AD-A158 820

AFWAL-TR-84-2065

200 TO 300 kVA
CONDITIONED POWER SYSTEM - DEVELOPMENT

WESTINGHOUSE ELECTRIC CORPORATION
ELECTRICAL SYSTEMS DIVISION
P.O. BOX 989
LIMA, OHIO 45802

MARCH 1985

DTIC

SEP 0 3 1985

E

FINAL REPORT FOR PERIOD SEPTEMBER 1982 TO MARCH 1984

AERO PROPULSION LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
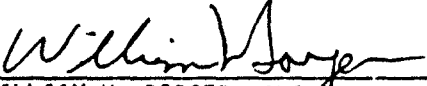AIR FORCE SYSTEMS COMMAND
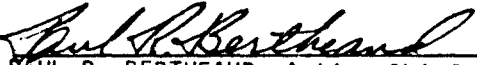
85 09 03 102

NOTICE

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture use, or sell any patented invention that may in any way be related thereto.

This report has been reviewed by the Office of Public Affairs (ASD/PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

WILLIAM U. BORGER, CHIEF
Power Conversion Project Office
Aerospace Power Division
Aero Propulsion Laboratory

FOR THE COMMANDER

PAUL R. BERTHEAUD, Acting Chief
Aerospace Power Division
Aero Propulsion Laboratory

"If your address has changed, if you wish to be removed from our mailing list, or if the addressee is no longer employed by your organization please notify AFWAL/POOC, W-PAFB, OH 45433 to help us maintain a current mailing list".

Copies of this report should not be returned unless return is required by security considerations, contractual obligations, or notice on a specific document.

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFWAL-TR-84-2065	2. GOVT ACCESSION NO. AD-A158820	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) 200 to 300 kVA Conditioned Power System - Development		5. TYPE OF REPORT & PERIOD COVERED Final Sept. 82 - March 84
		6. PERFORMING ORG. REPORT NUMBER 1383R
7. AUTHOR(s) W. E. Hyvarinen		8. CONTRACT OR GRANT NUMBER(s) F33615-82-C-2234
9. PERFORMING ORGANIZATION NAME AND ADDRESS Westinghouse Electric Corporation, ESD P.O. Box 989 Lima, OH 45802		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS P.E. 62203F 3145-29-68
11. CONTROLLING OFFICE NAME AND ADDRESS Aero Propulsion Laboratory (POO) Air Force Wright Aeronautical Lab, AFSC Wright Patterson AFB, OH 45433		12. REPORT DATE March 1985
		13. NUMBER OF PAGES 386
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION·DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release, distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Electrical Generator,
VSCF (Variable Speed Constant Frequency),
Large EW Systems,
Generic Power Technology,
Solid State Power Conditioning

System Control & Protection

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Future large AF electrical generator channels will be required to operate in parallel to supply single "large" loads. These channels will be required to use a minimum number of conversion stages to maintain the highest possible efficiency. The EW or other "large" loads will use power converted directly from the variable speed generator, and only that power required to be 400-Hz will be converted by the V.S.C.F. unit.
Redundancy for one generator out condition will be required. The protection and control of the parallel bus will require more sophistication and

DD FORM 1473   EDITION OF 1 NOV 65 IS OBSOLETE
1 JAN 73

20. complexity than the systems presently available.

Large rating generators, contactors, and distribution systems will require design effort and test.

This report covers a design study to meet the requirements of advanced high power EW systems for aircraft.

This report covers the design of a 540 kVA, six-phase generator which is spray oil cooled. The output ratings are 60 kVA at 53% speed, 120 kVA at 60% speed and 410 kVA above 83% speed. The generator maximum design speed is 15,000 rpm.

The 120-kVA, 400-Hz VSCF converter/inverter design is discussed along with the method of regulation required to meet the load speed characteristics of the generator and aircraft. The 13.2-k-vdc "large" power supply design is discussed. The method of regulation using the feedback to the generator control is unique to aircraft power systems.

Proposed mechanical designs of the generator, converter/inverter, high voltage unit and 28 vdc supply are included for size and weight estimates as well as the proposed package for a laboratory demonstration unit.

DEPARTMENT OF THE AIR FORCE
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES (AFSC)
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

REPLY TO
ATTN OF: POOA (Dr. W. Borger, (513) 255-6241)   12 September 1985

SUBJECT: Contract F33615-82-C-2234, Final Report AFWAL-TR-84-2065

TO: DTIC
Attention: DDAC, Mr. J. E. Cundiff
Cameron Station
Alexandria, VA 22304-6145

The subject final report (page 3-29) contains a "limited rights"

statement. I talked with the contractor on 12 September 1985 and we

mutually agreed that the statement is in error. Please remove this

statement on your copies and any copies requested from your

organization.

WILLIAM BORGER, Chief   cc: Westinghouse Electric Corp.
Power Conversion Project Office   Attn: Mr. D. Schmiedebusch
Aerospace Power Division   P.O. Box 989
Aero Propulsion Laboratory   Lima, OH 45802

FOREWORD

This final report was submitted by the Electrical Systems Division of the Westinghouse Electric Corporation under contract F33615-82-C-2234. The effort was sponsored by the Air Force Wright-Aeronautical Laboratory, Air Force Systems Command, Wright-Patterson AFB, Ohio with Dr. W. U. Borger, AFWAL-POOS-2, as Project Engineer. Donald W. Shireman of Westinghouse Electrical Systems Division was Program Manager, responsible for the overall effort.

This report covers work performed during the period September 1982 to March 1984 on Phase I. The final report for Phase I was submitted to AFWAL in March 1984.

The author gratefully acknowledges the contributions of J. Rosa, Westinghouse Research and Development Center; Leo Wilson and C. Carter, Westinghouse DESC Division; T. Lesster, R. Thing and J. Wilson, Westinghouse Oceanic Division; D. E. Baker, D. A. Fox, D. L. Stechschulte, L. L. Kessler, R. Sunderhaus, R. D. Jessee, J. L. McCabria, J. W. Ogden, and W. J. Shilling, Westinghouse Electrical Systems Division.

Accession For

NTIS GRA&I

DTIC TAB

Unannounced

Justification

By

Distribution /

Availability Codes

Avail and/or

Dist   Special

A-1

DTIC COPY INSPECTED 3

TABLE OF CONTENTS

PREVIOUS PAGE
IS BLANK

TABLE OF CONTENTS
(Continued)

TABLE OF CONTENTS
(Continued)

LIST OF FIGURES

LIST OF FIGURES
(Continued)

LIST OF FIGURES
(Continued)

LIST OF FIGURES
(Continued)

LIST OF FIGURES
(Continued)

LIST OF TABLES

1.0   INTRODUCTION

This report presents the results of the first phase of an Air Force program to design and develop a Hybrid High Power Aircraft Electric Power System. The requirements are reviewed, rationale for design approaches selected is given, and the initial design information is presented.

1.1   Contract Requirements

1.1.1   Objective

The objective of this program is to do the exploratory development effort to design one channel of a four-channel aerospace generator system configured to supply electrical power to advanced electronic warfare (EW) loads as well as power to the conventional 400-Hz loads.

The base configuration is defined in the Air Force Specification. It is the objective of the program to develop the system such that each type of power may be operated independent of the other and have a minimum interaction with the other sources of power. The configuration and the system requirements are reviewed below.

1.1.2   System Configuration

The system configuration is depicted in Figure 1.1.2-1. This shows the total aircraft electrical configuration in single line block diagram form. As can be seen from this figure, there are three types of power generated from the individual generator sources:

1. High Voltage dc (HVDC) (13.2 kv)
2. 115/200 Volts, 400 Hz ac
3. 28 Volt dc

Also, each of these three types of power are required to operate in parallel.
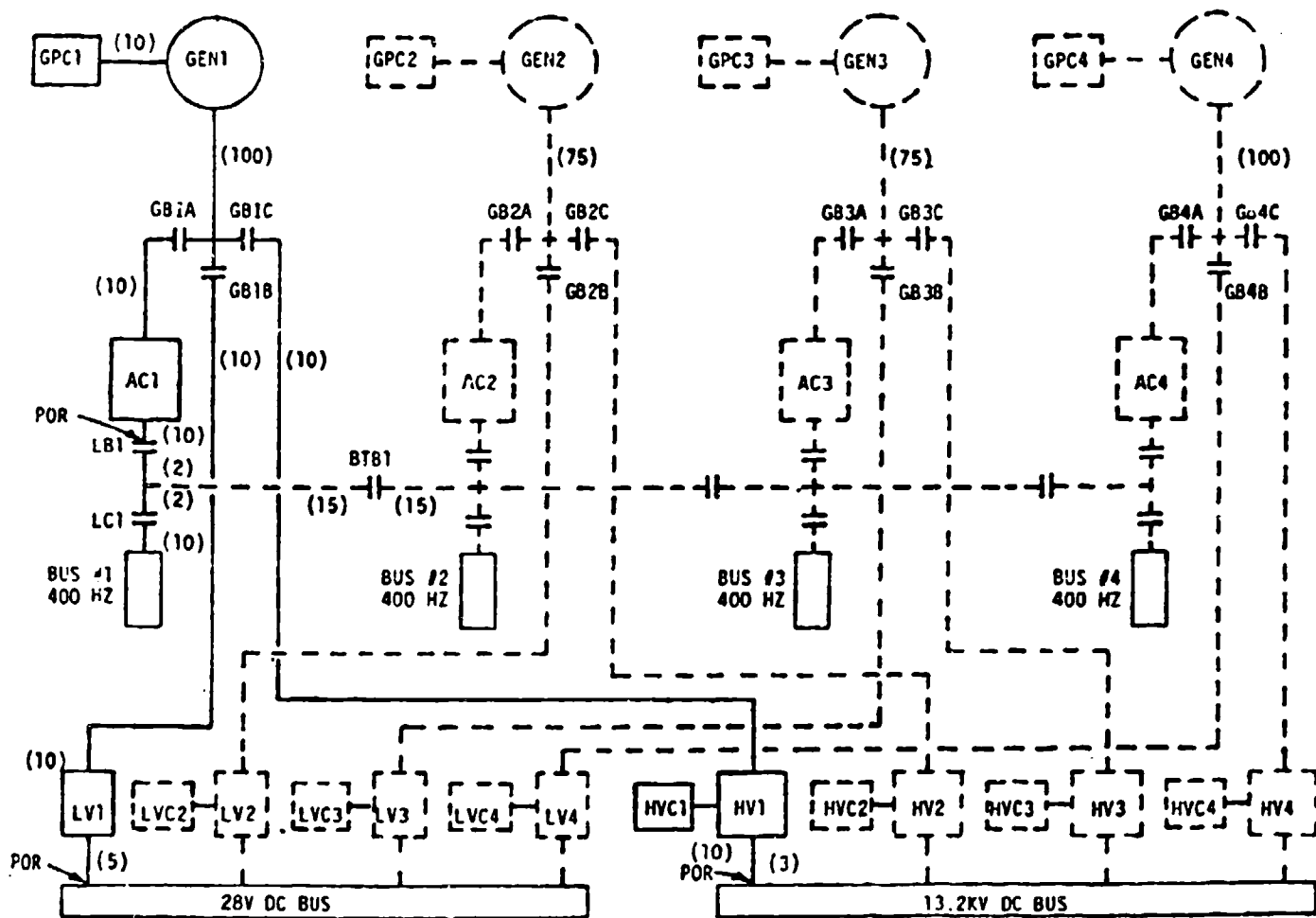
Figure 1.1.2-1

System Configuration

1.1.2   System Configuration (Continued)

The total load on each of these parallel systems is depicted in Figure
1.1.2-2. As each system must carry the load with one channel out, the
requirements for each channel are one-third of the total shown in Figure
1.1.2-2. A simplified block diagram of these requirements is shown in Figure
1.1.2-3.

1.1.3   Scope

The task is to design a single channel of the four-channel system with
consideration of the paralleling requirements; however, it is not necessary to
include the design of these circuits as part of the task.

The preliminary design task was to be approximately 50% complete for this
phase of the multiphase Air Force program.

1.2   Rationale for Design Selection

1.2.1   System Design

The load profile shown in Figure 1.1.2-2 shows that the largest power
requirements are associated with the 13.2kv dc power and that these
requirements are applicable only at the top of the speed range (83% to 110%).

The lightest load is that associate' with the 28v dc power system. Again,
this load is applied only in the top of the speed range. The 400-Hz system
power requirements cover the range of 53% speed to 110% speed.

The system interconnect single line diagram, Figure 1.2.1-1, depicts the
system components, the power flow paths, and the control interfaces.

The relative levels of load from each source and the generator speed at which
these loads are applied were taken into consideration in the design.
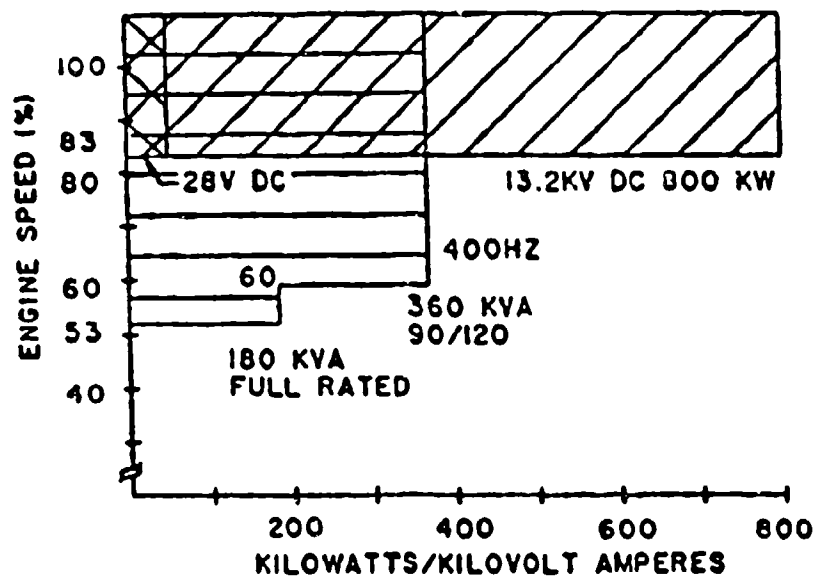
Figure 1.1.2-2

Load Profile
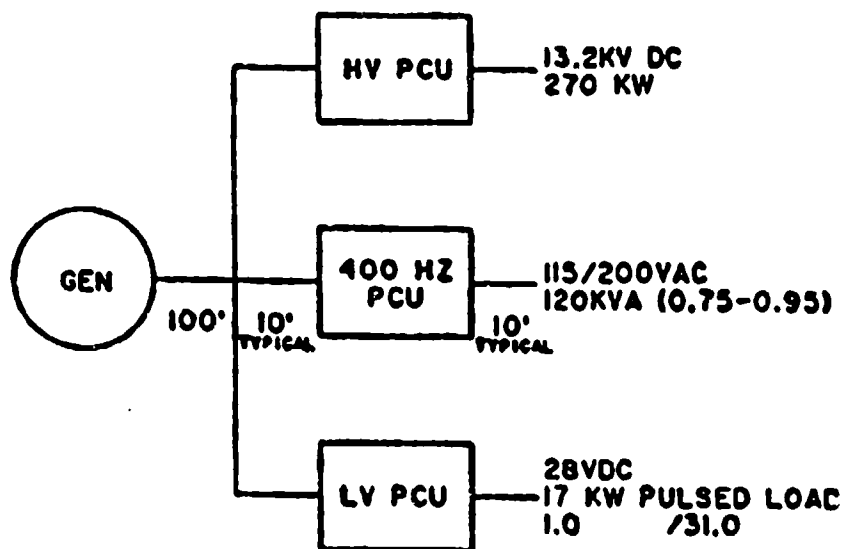
Figure 1.1.2-3
Block Diagram

1-5

1.2.1   System Design (Continued)

The primary concern of the overall system design is the electrical performance characteristics. Also, of concern is the system weight, efficiency, volume, cost, and reliability.

Based on these requirements, the following initial criteria were established for the system evaluation:

1. Six-phase generator (minimum filtering require.,ents)
2. High speed and high frequency
    a. Minimum generator weight
    b. Minimum filtering
    c. Maximum speed, ~25,000 rpm
    d. Minimum frequency, ~1,200 Hz
    e. Acceptable transmission losses
3. High transmission voltage
    a. Minimum transmission losses
    b. Generator corona considerations, ~250 v L-N Root Mean Square (RMS) nominal maximum
    c. Minimum voltage at 53 percent speed, less than 120 v RMS
4. Major impact of 13.2 kv, 270 kw output in determining overall system configuration and parameters.
5. 28 v dc output (4 percent system rating) addressed after 13 kv dc and 400-Hz outputs satisfied.

In nonlinear power conversion apparatus, maximizing the pulse frequency minimizes the filtering requirements. This makes it desirable to use a six-phase generator rather than a three-phase generator for the system. There is obviously a range of practical frequencies for optimum power conversion, limited at the upper end by losses in high power rectifiers, transformers, and power lines.

The generator output voltage should be the highest that is practical to minimize the system feeder weights and keep the electric power line voltage drop to a minimum. Thus, the limiting factor is the corona at the altitudes required for the application.
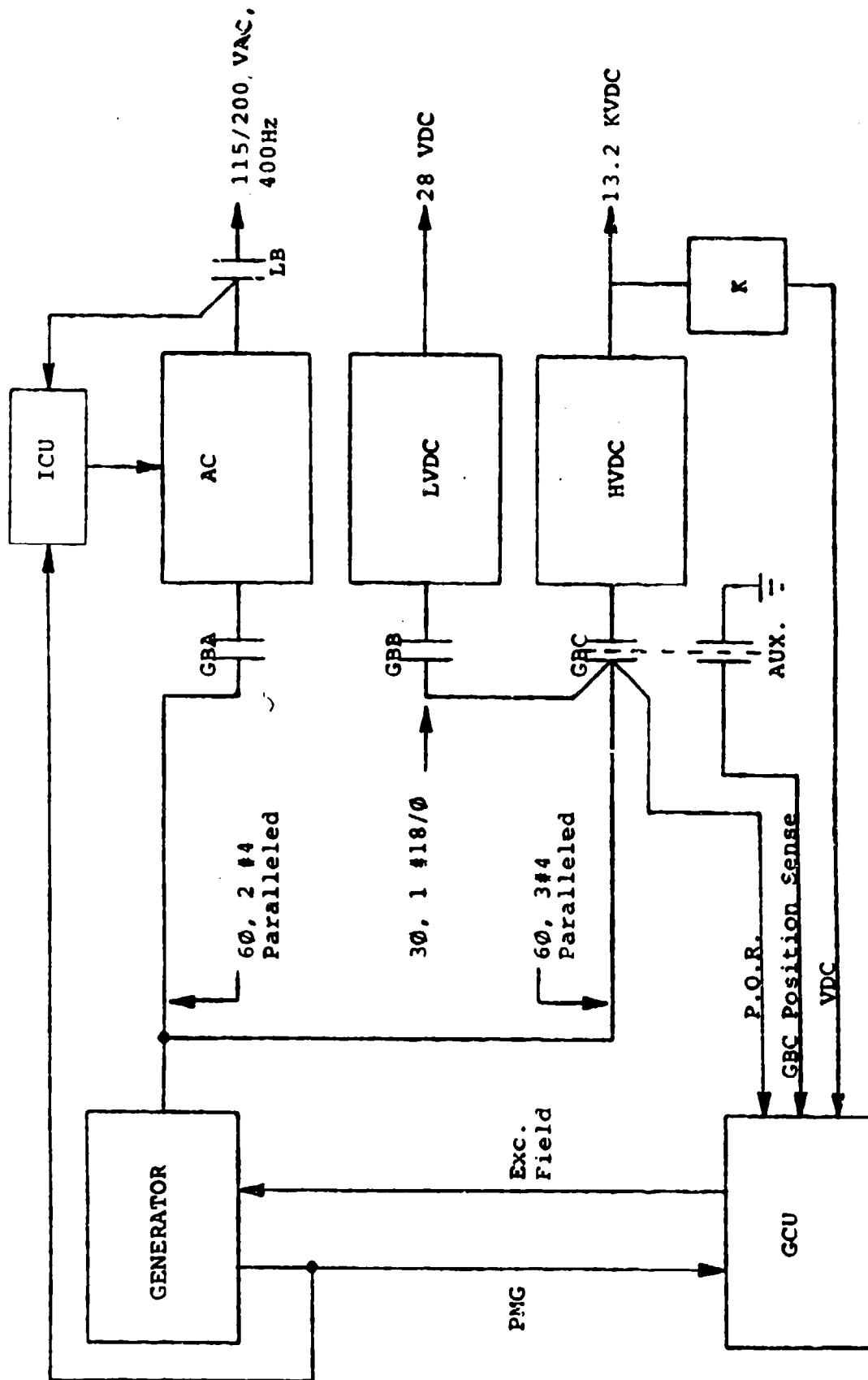
Figure 1.2.1-1
Single Line Diagram of Single
Channel System Interconnect

1.2.1   System Design   (Continued)

Based on the above, a six-phase generator was selected for the basic design, with a line-to-neutral voltage of 264 volts at the maximum speed. To provide maximum ripple frequencies for a rectifier type load, the generator output is further specified as consisting of two three-phase outputs, electrically isolated and separated from each other by 30°.

The high voltage dc power source imposes the greatest load on the generator system. Therefore, the control of this power source was of primary concern.

In selecting control options, steady-state voltage regulation (12 to 13.7 kv dc), current limiting at 1.2 per unit load, and load sharing when operating in parallel were operating conditions to consider.

Four control options were considered:

1. Voltage control and current limiting via generator field excitation control. Voltage would be sensed at the transformer input, thus depending on transformer voltage drop for required paralleling accuracy.

2. Voltage control and current limiting via generator field excitation control. Voltage would be sensed on the high voltage side, thus necessitating a load division circuit for parallel operation.

3. Voltage control and current limiting via reverse parallel connected thyristors.

4. Voltage control via field control, and current limiting via thyristor control.

The first and second options impose some constraints on the other power-conditioning subsystems, but as analysis showed, these options do not impose a severe burden on the design requirements for those systems. Overall, they have significant system appeal. As for the third option, a trade-off between

1.2.1   System Design   (Continued)

the primary and secondary would quickly show that it is preferable to put the phase-controlled arrangement on the primary side rather than on the high voltage side. The unfortunate aspect of this approach is that the primary electronics now have to be rated for the full system throughput and there is an additional filtering burden imposed on the secondary filter with this type of arrangement. Option 4 is a compromise where voltage control is used during normal operating modes via field control, maintaining the phase controlled rectifier in a full-on condition. This does not impose a severe requirement on the filtering and, if the load can tolerate it, phase control can be used just for current limiting. Unfortunately, the problem of the high rating required for the electronics portion of this process still exists.

Based on the above, options 3 and 4 were eliminated from further consideration. Option 1 has the advantage of not requiring a paralleling circuit. However, analysis shows that the High Voltage Direct Current (HVDC) system voltage regulation would not be met using this approach. Therefore, the design of the system is based on Option 2.

It must be kept in mind that the High Voltage Direct Current (HVDC) system is to operate only between the 83% to 110% speed conditions, while the 400-Hz system operates from 53% speed to 110% speed. Thus, when the generator speed is below the 83% speed, an alternate means of generator control is required.

A transfer means for point of regulation is therefore required if the HVDC output is sensed for excitation control when the HVDC is on. This has been accomplished. Between 53% and 83% speed, the generator output is sensed and controlled to approximately 140 volts line-to-neutral (L-N). This is the voltage level required of the 400-Hz AC conversion unit to satisfy its power requirements.

At the lower speed, the generator voltage support capabilities also are lower. The 400-Hz power conversion device is designed to provide the required power output at this lower voltage.

1.2.1   System Design   (Continued)

Two options were available for generator voltage control in the lower operating speed range. The first was to regulate to a constant generator output voltage, and the second was to provide a system with a constant voltage-over-frequency (V/F) characteristic.

Analysis showed that there is no advantage in going to a constant V/F characteristic, while there are two disadvantages; the controls are more complex with a constant V/F, and the system tends to be slightly less efficient.

Next, the 400-Hz system requirements were considered. The source voltage for the 400-Hz system has been established. At the lower speeds (53% to 83%) the voltage is constant at about 140 volts L-N, and at the higher speeds the voltage is predicated on the HVDC power supply requirements. This, then, requires that the 400-Hz power conversion device be self-regulating to maintain a regulated output with the variable voltage input.

There are two basic approaches that may be used for power conversion from a variable frequency, variable voltage to a constant frequency, constant voltage output:

1.   A cycloconverter type unit
2.   A dc-Link-type unit

Either unit would require means of regulation control.

Figure 1.2.1-2 is a rough diagram of the cycloconverter approach, showing the power stage repeated three times for each of the three output phases. It shows the complexity of this approach and shows some of its significant points, especially that with this scheme the neutral is run to the conversion unit to the generator. The second approach, the dc-Link inverter (Figure 1.2.1-3), has to have a neutral-forming transformer to provide the fourth wire; however, it does not require the neutral to be brought out from the
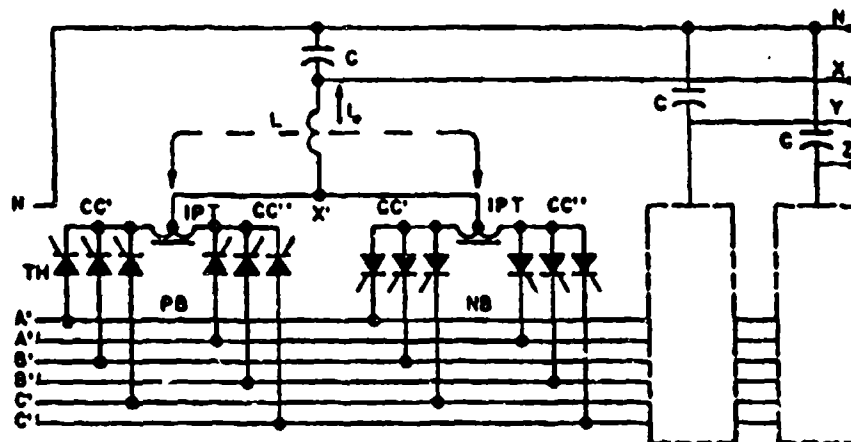
Output voltage quality and steady state and transient regulating accuracy depend to a large extent on the performance of a complex control circuit detecting critical timing of 36 thyristors and selection of six thyristor banks. Cycloconverter has a fixed ratio of net converter output current and input phase current (feeders and generator) of 0.666 and requires a generator neutral feeder cable rated for 33-1/3% nominal output current.

Figure 1.2.1-2

Cycloconverter Approach

1-11
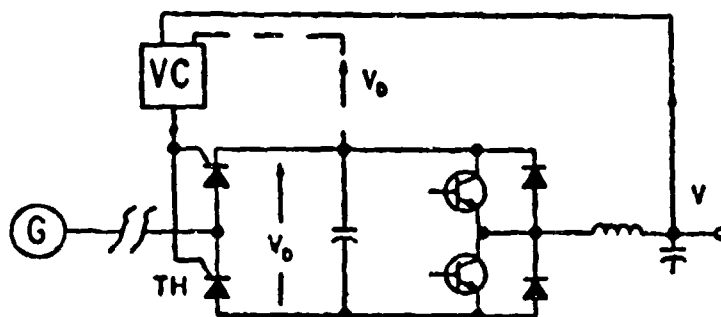
Using a fixed PWM digitally derived waveform pattern, the steady state and transient accuracy of the output voltages depend on the accuracy and speed of the link voltage control. A DC Link system has a ratio of 1.31 (real component of net inverter output current and DC Link current) and 0.41 (DC-Link current and input phase current) and requires a neutral forming transformer.

Figure 1.2.1-3

DC-Link Inverter Approach

1-12

1.2.1 System Design (Continued)

generator. The scheme that we recommend for operating the inverter stage is a fixed pattern controlling the bridge switches, such as transistors, that would then determine output frequency and distortion factors. Traditionally, voltage is controlled by regulating the link voltage via generator field control in this type of system. In this case, because of the choices already made on the 13-kv system, a preregulator stage is needed for the dc-Link system to compensate for the generator voltage variation over the speed range.

As can be seen from these diagrams, the power conversion goes through one stage for the cycloconverter and two stages for the dc-Link. The cycloconverter requires a total of 36 power switches (12 per output phase) and the dc-Link requires a total of 18 power switches (12 for the rectifier portion and 6 for the inverter).

Table 1.2.1-1 summarizes some of the critical differences between these two systems. The requirements imposed on the generator are less for the DC-Link type system. This results in a lower generator kVA requirement, as well as lower feeder weights from the generator to the converter. The neutral from the generator is not required for the dc-Link system; however, a neutral-forming transformer is needed. The weight advantage, even considering the neutral-forming transformer, favors the dc-Link type system.

Weight, however, is not the only consideration. First, the cycloconverter circulates reactive power through the feeder system and the generator. In contrast, the dc-Link system constrains the reactive current flow to the output stage of the inverter. That is significant. Second, under unbalanced conditions, an undesirable 800 Hz modulation effect is imposed on the generator terminals. The modulation is reflected into the 13-kv supply. The filter, for a 12-pulse output, is not designed for 800-Hz disturbances. That imposes a severe penalty on the filtering in the 13-kv supply and also creates a problem with the feeding of faults, where significant reactive power is circulated through 110 feet of feeder. Another constraint is maintaining minimum voltages on the generator output so that the supply can meet its other output requirements, such as the 28-v dc system.

1-13

Table 1.2.1-1 - 400 Hz Conversion Options

Load Condition	Cycloconverter		DC-Link	
	Steady State	Sh. Ckt.	Steady State	Sh. Ckt.
Load KVA	120	N/A	120	N/A
Load Power Factor	1	N/A	1	N/A
Load Current, Amp	348	N/A	348	N/A
Filter Current, Amp	174	~0	162	~0
Converter Output, Amp	389	1,044	384	1,044
DC-Link Current, Amp	N/A	N/A	456	~0
Input Phase Current, Amp	220	591	186	~0
Neutral Current at 1/3 Load				
Unbalance, Amp	116		116	

1.2.1 System Design (Continued)

If all of these constraints are taken into consideration for this particular application, a dc-Link system offers some significant advantages. The input stage does have additional complexity: it is not a rectifier; it now becomes a phase-controlled bridge; it requires some additional filtering on the link. However, on an overall system basis, considering weight, reliability, and efficiency, the trade-offs work in favor of the dc-Link system. Now that this has been determined, the control strategies that are applicable can be reviewed. Some of these have almost been discounted, but are included for the sake of completeness.

One option is to use field control on the generator. That is a viable option and is the simplest. The same statements hold true here as for the 13-kv system. However, choosing field control for the 13-kv system implies a separate generator to feed the dc-Link system. In the ground rules established by the application requirements, there is a specific requirement for a single generator, meaning a single, physical generator, not necessarily a single generator designed with that physical envelope.

A second option for voltage control is the use of gate-controlled thyristors. The input stage is a phase-controlled bridge. When considering interactions between the systems, the phase-controlled front end provides a one-way buffer between the 13-kv system and the 400 Hz system. There is also the question of transient response. The faster response time of Option 2 and its effect on transient response at the output of the 400-Hz system more than compensates for the increased complexity. Option 2 also provides buffering of the 400-Hz output due to sudden load changes in the 13-kv output. Although there is some interaction between the 13-kv and 400-Hz outputs, the controlled rectifier helps to minimize these effects.

It should be pointed out here, that the design of the generator is predicated largely on the ripple and the resultant filtering requirements on the 13-kv system. This necessitates use of a generator that has two sets of three-phase windings, electrically 30° apart. This generator design does not provide the voltages to a cycloconverter as required (six-phase generator with 60° between phases).

1-15

1.2.1   System Design   (Continued)

The preceding paragraphs have addressed feeders from the aspect of the
interaction between the 400-Hz system and the HVDC system.   To minimize the
interaction of these supplies, dedicated feeders could be used for each supply
from the generator.   However, there are other factors that need to be
considered prior to making a final selection.   These factors are:

    1.   Continuous current rating
    2.   Skin effect impact due to high generator frequencies
    3.   Weight of single conductors versus paralleled conductors per phase
          for the current levels required

The power requirements of the generator for the 13-kv dc system and the 400-Hz
system as a function of speed (in %) were tabulated.   These tabulations are
presented in Table 1.2.1-2. which provides the information necessary for
evaluation of feeder requirements (the 28-v dc power requirements have a
negligible impact on feeder selection).

From the viewpoint of the conversion equipment, it is desirable to have as
much isolation between the 13-kv and 400-Hz systems as practical. With a
common generator, the use of dedicated feeders for each source provides the
maximum isolation.   The question then becomes a matter of penalty, if any,
associated with providing dedicated feeders.

From Table 1.2.1-2 it is seen that the maximum continuous current requirement
is 360 amperes per phase from the generator.   For the preliminary analysis,
IEEE Std 128-1976 was used for reference.

Table II-1 of this standard shows that one 4/0 size copper conductor can carry
380 amperes as a single wire in free air.   Paralleling conductors require two
number two, three number four, four number six, or five number eight
conductors to carry this same current.   Finished wire weight for the
conductors are as follows:

Table 1.2.1-2 - Generator Summary

Load	Full	5 Min O.L.	5 Sec O.L.	Full	5 Min O.L.	5 Sec O.L.
RPM	53%	53%	53%	60%	60%	60%
I_{HVDC}		0	0	0	0	0
$I_{400\ Hz}$	92 ∠-31 (60 KVA)	104 ∠-31 (75 KVA)	138 ∠-31 (90 KVA)	124 ∠-31 (120 KVA)	207 ∠-31 (135 KVA)	276 ∠-31 (180 KVA)
$I_{TOTAL\ GEN}$	92 ∠-31	104 ∠-31	138 ∠-31	184 ∠-31	207 ∠-31	276 ∠-31
$V_{GEN\ L-N}$	143	144	144	146	147	149
KW	68	77	102	138	156	212
KVA	79	90	119	161	183	247
Pf	.86	.85	.85	.86	.85	.86

Load	Full	5 Min O.L.	5 Sec O.L.	Full	5 Min O.L.	5 Sec O.L.
RPM	83% +	83% +	83% +	83% -	83% -	83% -
I_{HVDC}	207 ∠-18 (270 KW)	207 ∠-18 (270 KW)	207 ∠-18 (270 KW)	0	0	0
$I_{400\ Hz}$	184 ∠-62 (120 KVA)	207 ∠-62 (135 KVA)	276 ∠-62 (180 KVA)	184 ∠-31 (120 KVA	207 ∠-31 (135 KVA)	276 ∠-31 (180 KVA)
$I_{TOTAL\ GEN}$	360 ∠-38	382 ∠-40	447 ∠-43	184 ∠-31	207 ∠-31	276 ∠-31
$V_{GEN\ L-N}$	245	245	245	148	149	152
KW	418	430	481	140	159	217
KVA	530	562	657	163	185	252
Pf	.79	.77	.73	.86	.86	.86

Table 1.2.1-2 - Generator Summary
(Continued)

Load	Full	5 Min O.L.	5 Sec O.L.	Full	5 Min O.L.	5 Sec O L.
RPM	110%	110%	110%			
I_{HVDC}	207 $\underline{\|-18}$	207 $\underline{\|-18}$	207 $\underline{\|-18}$			
$I_{400\ Hz}$	184 $\underline{\|-12}$	207 $\underline{\|-62}$	276 $\underline{\|-62}$			
$I_{TOTAL\ GEN}$	361 $\underline{\|-38}$	382 $\underline{\|-40}$	447 $\underline{\|-43}$			
$V_{GEN\ L-N}$	245	245	245			
KW	418	430	481			
KVA	531	561	657			
Pf	.79	.77	.73			

1.2.1   System Design   (Continued)

Conductor(s)	Weight (lbs per ft.)
One single, 4/0	0.820
Two number two	0.560
Three number four	0.528
Four number six	0.460
Five number eight	0.382

This decreasing weight with increasing number of conductors illustrates how weight of feeders is reduced by use of parallel conductors.

Another factor to consider in selecting the feeder configuration, especially with the high frequency of the generator (1204 to 2500 Hz), is the voltage drop of the feeders. Associated with this are two factors: conductor skin effect and the reactance of the lines.

Skin effect is a function of two parameters: the resistance per unit length of the conductor and the frequency of operation. Calculations were made for conductor sizes ranging from a size eight conductor to a 1/0 conductor. Skin effect at 2500 Hz (worst case on the conductor effective resistance) is negligible (factor of 1.05) for the smallest size wire, and an appreciable value for the 1/0 conductor (factor of 1.7). The results of the analysis are presented in Table 1.2.1-3. This table also presents voltage drops for the conductor for rated current (based on conductor rating).

Based on the analysis on skin effect, the decision was made to proceed with no conductors of physical size greater than a number four. For the preliminary design, it was therefore concluded that two number four conductors per phase would be used for the 400-Hz source and three number four conductors per phase would be used for the HVDC source.

Table 1.2.1-3 - Skin Effect at 2500 Hz

Wire Size	Rdc* (Ω/100 ft.)	mr **	R2500/Rdc	R2500 (Ω/100 ft.)	*** Icap	X2500 (Ω/100 ft.)	Vdrop**** at ICAP (V/100 ft.)
#8	.0700	1.654	1.05	.0735	46	.1412	7.32
#6	.0436	2.096	1.10	.04796	60	.1381	8.77
#4	.0274	2.643	1.18	.0323	80	.1325	10.9
#2	.0179	3.271	1.40	.02506	100	.1288	13.1
AN-0	.0114	4.098	1.70	.0194	150	.1275	19.3

*   At 20°C

**   mr = .036 $\sqrt{\mu rf/Ro}$.   See "Elements of Power System Analysis" by W. D. Stevenson for futher explanation.

***   Conductor capacity based on Table II-1 of IEEE Std 128-1976 IEEE Guide for Aircraft Electric Systems.   This does not take skin effect into consideration.

**** Voltage drop was calculated based on current times impedance. Differences in voltages would be less.

1.2.1   System Design   (Continued)

Voltage drops were calculated for these feeder configurations for both the 400-Hz and HVDC supply lines and are shown in Tables 1.2.1-4 and 1.2.1-5, respectively.

Minimum weight, low loss feeder lines are thus implemented using paralleled conductors. This is accomplished with an approach that provides for minimum interaction between the HVDC and the 400 Hz power supplies, as well as low line drops from the source to the conversion equipment.

The 28 volt dc system represents only a small portion of the generator load. Initial evaluation indicates that the best approach to this design is to use the energy storage technique to keep size and weight to a minimum.

The average power required per channel is less than 600 watts. Based on this level of power, the input power will be from only one set of 3-phase windings (instead of two sets) and separate feeders will not be run from the generator.

1.2.2   Generator Control Unit and Generator

1.2.2.1   Generator Control Unit

The Generator Control Unit (GCU) is designed to function as a working breadboard, that is, it must be reliable, yet easily modified and tested. Many funtions in the GCU, while not complex, are unique to this system, and may need modifications. For this reason, the GCU is designed using conventional analog circuits partitioned onto six, plug-in printed wiring boards.

Circuits are designed to be as modular as possible, that is, with little or no interaction between different factors so that performance of each circuit can be easily monitored and modified. The GCU is packaged in a roomy, fabricated sheet metal enclosure allowing easy access to all parts while the unit is operating.

Table 1.2.1-4 - Voltage Drop to 400 Hz Converter
Two Parallel #/ Gauge Conductors 100 Feet Long

Generator Frequency (Hz)	400 Hz Load (KVA)	Current to Converter (A)	Voltage (V) Drop	
			Line	Generator Converter
2500	120 Cont.	184 |-62	12.55	12.17
2500	135 5 min.	207 |-62	14.12	13.69
2500	180 5 sec.	276 |-62	18.82	18.24
1886	120 Cont.	184 |-62	9.64	9.46
1886	135 5 min.	207 |-62	10.85	10.65
1886	180 5 sec.	276 |-62	14.46	14.19
1886	120 Cont.	184 |-31	9.64	7.05
1886	135 5 min.	207 |-31	10.85	7.92
1886	180 5 sec.	276 |-31	14.46	10.47
1364	120 Cont.	184 |-31	7.19	5.68
1364	135 5 min.	207 |-31	8.09	6.38
1364	180 5 sec.	276 |-31	10.80	8.48
1205	60 Cont.	92 |-31	3.24	2.66
1205	67.5 5 min.	104 |-31	3.66	3.00
1205	90 5 sec.	138 |-31	4.86	3.98

Table 1.2.1-5 - Voltage Drop to High Voltage dc Power Supply
Three Parallel #4 Gauge Conductors 100 Feet Long

Generator Frequency (Hz)	HVDC Load (KW)	Current to HVDC Pwr. Sup. (A)		Voltage (V) Drop	
				Line	Generator Pwr. Sup.
2500	270	207	~18	9.44	4.94
1886	270	207	~18	7.22	4.11

1.2.2.2   Generator

1.2.2.2.1   Electrical Rationale

Although the mechanical design is unique, the electrical design is a conventional
salient pole, brushless generator design.

This conventional design (with the main machine having rotating salient poles)
has been proven over time to be an optimum type design. The design is "optimum"
with regard to weight, size, and electrical performance. In other type designs
(Induction, Lundell, Homopolar, Beckey-Robinson, etc.), flux paths are long.
Flux cannot be contained or isolated. When paths are long, leakage flux becomes
a problem, which leads to weight and performance penalties. Also, steel is
required to carry flux. Long flux paths then result in weight penalties.

Nonconventional machines do have certain advantages that can be utilized in
unique applications, but in general, the problems outweigh the advantages so that
these type generators remain in a nonconventional category.

Permanent magnet salient pole generators tend to have most of the inherent
advantages of conventional wound rotor salient pole machines. However, PM
generators have voltage regulation problems and high iron losses at high speeds.

Unique Design

For mechanical reasons it is desirable to have a short machine. To accomplish
this a unique design technique was used in which the main machine is designed
with a hollow shaft large enough to tuck the exciter and PM generator inside the
hollow shaft (see Figure 1.2.2.2-1) . This has a double effect in reducing
machine length: (1) The large diameter of the main machine inherently gives a
short design; and (2) the exciter and PM generator no longer have an effect on
length.

1-24

SECTION B-B

SECTION A-A

Figure 1.2.2.2-1
Generator Layout

1013

CTION A-A

SECTION C-C
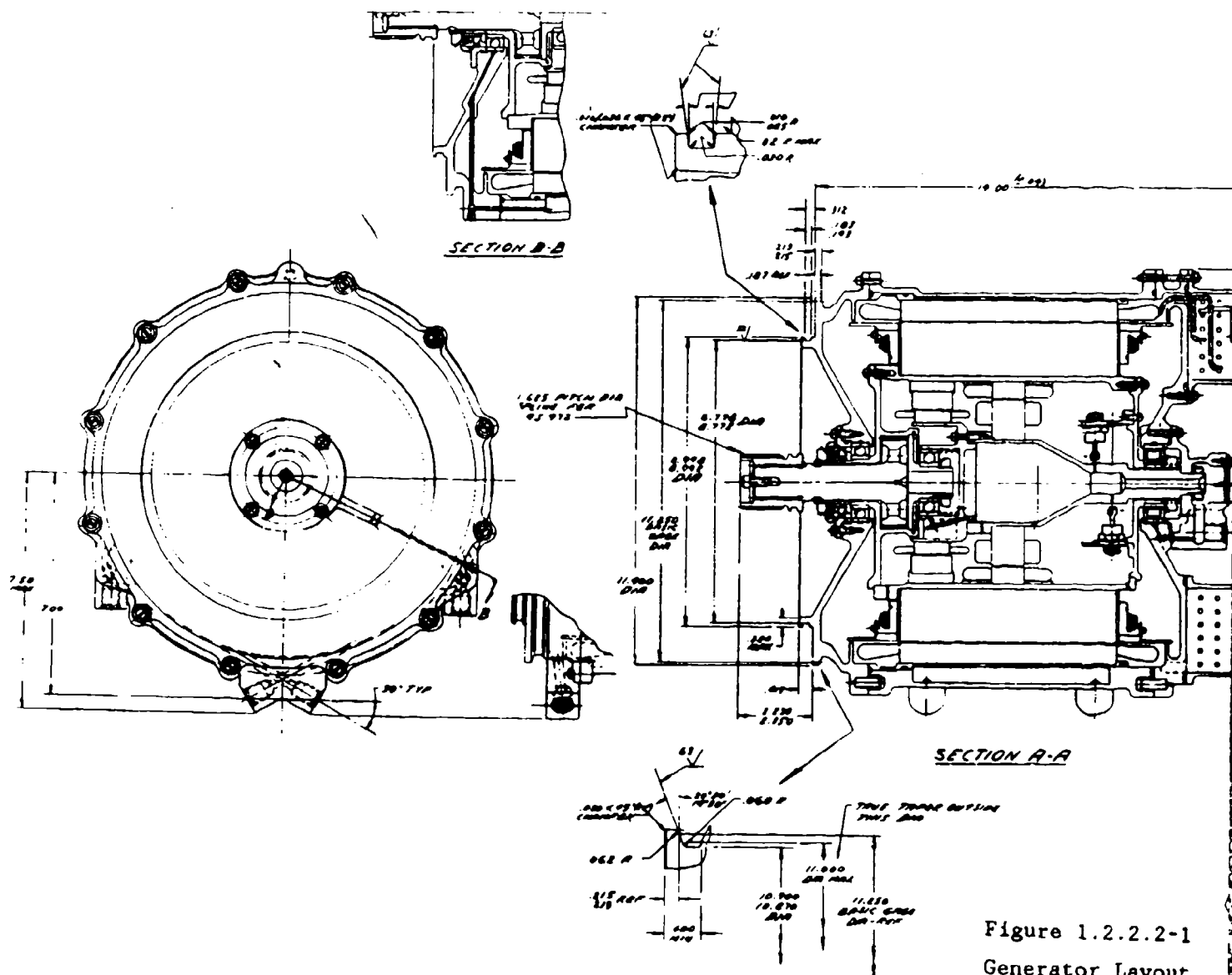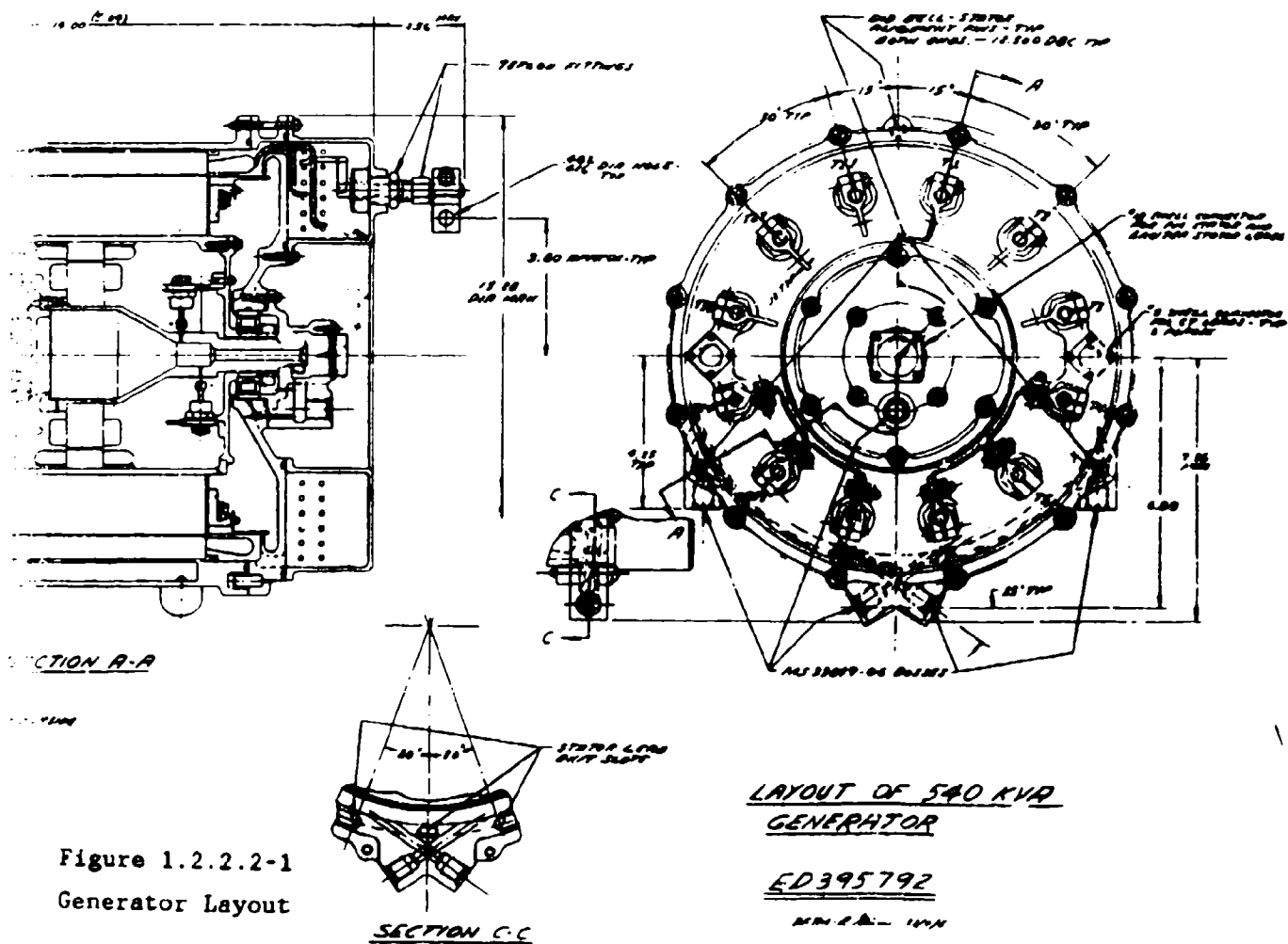
Figure 1.2.2.2-1
Generator Layout

LAYOUT OF 540 KVA
GENERATOR

ED395792

1-25

1.2.2.2.1   Electrical Rationale   (Continued)

Poles

It is desirable to have a relatively large number of poles for two reasons:
(1) the larger the number of poles, the easier it is to wedge the rotor
winding to contain the winding mechanically; and (2) the more poles, the
higher the frequency. From an electrical system consideration the higher
frequency has advantages; e.g. filtering rectified output power.

On the other hand, an excessive number of poles can cause excessive leakage
flux between poles. A design of 20 poles was established which gives a
frequency range of 1,205 to 2500 Hz over a speed range of 7227 to 15,000 rpm.

Speed

The fundamental requirement for generating voltage is the cutting of lines of
flux-- the faster the cutting or the more the flux, the higher the voltage.
Stated another way, the higher the rotor peripheral speed of a generator, the
less the weight of the generator. The top rated speed of the subject
generator is 15,000 rpm. It has a rotor diameter of 10 inches, which then
gives a rotor peripheral speed of 654 feet per second. As rotor peripheral
speeds go up, mechanical problems become severe. The 654 feet per second is
representative of the present state of the art. (For example, this compares
to 585 feet per second for the F-20 generator).

Rated Voltage and Corona

Machine size is a function of kVA rating. It is usually desirable to use a
high rated voltage (to keep system transmission wire weight down), but voltage
is limited by corona problems. Standard aircraft rated voltage is 120/208.
In the subject design, the internal generator cavity will be pressurized to 7
psia minimum which will allow a rated voltage of 245/425 volts.

1.2.2.2.1   Electrical Rationale   (Continued)

Six Phases

The generator is a six-phase machine. This is accomplished using two isolated three-phase windings displaced 30°. The six phases are a system requirement (based on converter requirements, which are discussed in another section).

Reactances

From a system standpoint it is usually desirable to have low reactances in the generator. However, low reactance designs are usually heavy. The optimum lightweight design usually occurs when the machine reactances are the maximum that can be tolerated by the system. The desired generator reactance, then, is somewhat judgmental. For this reason, it may be useful to compare reactances of the subject machines with other generators. A comparison is shown below:

		X_d(%)*	X''_d(%)*
New	540 kVA (ED395792)	165	20.8
Std	500 kVA (977J016-4)	263	15.7
F-111	62.5 kVA (976J404)	138	9.3
F-20	40 kVA (977J311)	123	16.0

* Note: X_d is the synchronous reactance at maximum rpm. X''_d is subtransient reactance.

Wire Size

The choice of wire size for the various generator windings influences: losses, efficiency, temperatures, voltage transients, and machine constants.

1.2.2.2.1   Electrical Rationale   (Continued)

In the main AC winding, the high frequency of the current can cause an
excessive AC resistance (skin effect) unless the wire strands are small.   In
the subject design, wire strands are .064.   This gives a calculated eddy
current factor (AC resistance divided by DC resistances) of 1.27 at 11,319 rpm
and 1.48 at 15,000 rpm.   This factor has been considered in loss calculations.

Winding losses affect winding temperatures.   Thermal calculations are complex,
but a comparison of wire current densities can be helpful and are shown below:

	New Design	E-4B	F-20
Rated kVA	540	150	40
Cooling (Oil)	Spray & Conduction	Spray	Spray
Main Stack	6.9 in.	3.25 in.	2.0 in.
	Amp/in^2	Amp/in^2	Amp/in^2
Main AC Winding	14,067	14,900	14,800
Main Field	18,084	14,500	21,200

"Sew-Thru" Winding

A new winding technique has been developed at Lima Westinghouse known as
"sew-thru" winding.   In this type winding, the wire is sewn through the slot
instead of inserted from the stator bore.   Such a winding is continuous with
few braze joints.   It is impossible for wires to fall in the air gap during
operation.   The "closed" slot is also conducive to flux flow through the air
gap.   The winding technique is applicable to automatic winding.   In summary
then, the new technique provides good electrical design, highly reliable, at
low cost.

"Sew-Thru" Winding   (Continued)

At this time, development of this winding is based on a one-conductor wide
slot. In the power conditioning generator, a one conductor wide slot requires
an excessive number of slots; thus a two-conductor wide slot will be
required. This development entails reasonable effort.

Winding and Waveform

Good waveform in generators, especially under load, is usually accomplished by
using a winding that uses a large number of slots with a chorded winding. (A
chorded winding is one in which the coil spans a number of slots less than the
number of slots per pole.) However, such type windings require extra magnetic
steel. In the power conditioning generator, the winding is "fully pitched" so
that there are no weight penalties. The 3rd harmonic (space) is eliminated by
using line-to-line voltages. The 5th and 7th harmonics calculate to be 4
percent and 2 percent respectively, at no load. This is accomplished by
choosing a pole head width to give good flux waveform. Under load, though,
the flux gets distorted which affects the 5th and 7th harmonics. Calculations
of waveform under load are complex, but system consideration indicates that
exceptionally good waveform under load is not required.

Magnetic Steels

The poles of the main machine are highly stressed mechanically. (Stress
analysis is covered in another portion of this report.) A steel developed by
Westinghouse, Hiperco 50, will be used for the main poles. This steel has
very good magnetic properties and has tensile strengths of 100,000 psi and
higher (with special annealing).

1-29

Magnetic Steels   (Continued)

The main stator punching will be Hiperco 27, 0.006 inch thick. Hiperco 50 has better magnetic qualities than Hiperco 27; however, the width of steel required for the stator (~12 inches) is not available for Hiperco 50 in the market at this time. (The width requirement is based on a one-piece punching. Such punchings are standard in the aircraft industry to support high reliability.) The thin punching keeps iron losses to a minimum.

Exciter

The exciter design is based on the F-20 main generator design with the primary difference being stack length and pole winding. The design, however, is utilized in a significantly different mechanical mode. In the F-20 application, the AC winding structure was stationary while the pole structure rotated. In this new application, the AC winding structure rotates while the poles are stationary. This is a new concept. The mechanical implications and considerations are discussed.

PM Generator

The PM generator (PMG) provides power for control functions and generator excitation. The high coercive force permanent magnets are samarium cobalt The PMG design is based on the F-20 PMG; however, because it is mounted inside the shaft, it was necessary to turn the design "inside-out". See Figure 1.2.2.2-2. Thus the AC winding structure is inside the pole structure. The pole structure, mounted inside the shaft, rotates with the shaft. The basic electrical design has been proven in F-20, AV-8B, and F-18 aircraft applications.

Rotor Mechanical Design

The rotor lamination is made of a high permeability and high strength iron-cobalt electrical sheet steel. The thickness is 0.006 inch. Finite element (FE) program has been employed to analyze and optimize the rotor

Figure 1.2.2.2-2
PMG Design

1-31

PM Generator   (Continued)

lamination designs. Attention is focused on weight reduction and stress
concentration of critical areas under the overspeed condition.

A FE model of a typical twelve-pole lamination is shown in Figure
1.2.2.2.2-1. Only a symmetrical sector of 15° with proper boundary condition
is analyzed. Thin shell elements (eight nodes each) of the SUPERB (an FE code
of structural Dynamics Research Company) are used for the model. Figure
1.2.2.2.2-1 shows a right angle applied to the root corner of the pole.
During design optimization, the radius of the corner is increased until a
satisfactory margin of safety, from the standpoint of fatigue strength, is
obtained.

The design history, along with the FE analyses, is described in the following
paragraphs.

Original Rotor Designs

An overspeed of 25,000 rpm is applied to original rotor design analyses. A
summary of the original rotor design analyses for the Conditioned Power System
is listed in Table 1.2.2.2.2-1.

Designs for Winding of 0.091 Inch Wires

Twenty-two turns of 0.091 inch (or 0.096 inch insulated) diameter wires have
first been proposed for a rotor of 6 inch OD. A gap of 0.788 inch between the
punching yoke and the aluminum wedge is required to accommodate a column of
eight turns of wires plus two layers of insulation (0.010 inch thick each).
Generally, the thickness of the yoke is maintained at about 0.043 inch. The
ID of the punchings is 2.650 inch for both Designs 1 and 2.

Design 1 (R = 0.040 Inch)

Figure 1.2.2.2.2-2 shows the FE model where a radius of 0.040 inch is applied to the corner around the roots of each pole. The deformed geometry at 25,000 rpm is also shown. Figure 1.2.2.2.2-3 shows the maximum stress at the corner is 141,980 psi, which is greater than the yielding of material (H-50). The yielding of material is 120,000 psi.

Design 2 (R = 0.060 Inch)

Figure 1.2.2.2.2-4 shows the only change is that the radius of the corner, is 0.060 inch instead of 0.040 inch for Design 1. Figure 1.2.2.2.2-5 shows the maximum stress at the corner at 25,000 rpm becomes 127,760 psi, which is still greater than the yielding (120,000 psi). A reduction of 10% in the stress is achieved for Design 2 versus Design 1.

Designs for Winding of 0.072 Inch Wires

Smaller wires (0.072 inch, or 0.076 inch insulated) are secondly proposed for the 22 turn winding. A gap of 0.552 inch between the yoke and the magnesium wedge is required to accommodate a column of seven turns of the wires plus two layers of insulation. The thickness of the yoke is maintained at about 0.450 inch. The OD of the punching is the same as Designs 1 and 2. The ID of the punching becomes 3.176 inch for the rest of the designs.

Design 3 (R = .040 Inch)

Figure 1.2.2.2.2-6 shows the main dimension and a radius of 0.040 inch applied to the corner around the pole root. The deformed geometry at 25,000 rpm is also shown. Figure 1.2.2.2.2-7 shows the maximum stress at the corner is 129,690 psi, which is still beyond the yielding.

Design 4 (R = 0.048 Inch, θ = 30°)

Figure 1.2.2.2.2-8 shows the change around the corner. Essentially, it is to split the stress concentration into two radii (R = 0.048") around the root of each pole; as the design of the F-20 rotor. The angle θ is 30° between the horizon and the straight portion which links the radii. Figure 1.2.2.2.2-9 shows the maximum stress of 98,920 psi at 25,000 rpm happens at the lower right radius. The stress is now less than the yielding.

Design 5 (R_=0.048 Inch, θ = 20°)

Figure 1.2.2.2.2-10 shows the only change is made in the angle. The angle is 20° instead of 30°. The maximum stress of 100,900 psi moves to the upper-left radius (Figure 1.2.2.2.2-11).

Design 6 (R = 0.048 Inch, θ = 25°)

Figure 1.2.2.2.2-12 shows an angle, θ = 25°, between 20° and 30°, is selected. Hopefully the stress concentration will be evenly split at both radii. Relatively even stress distribution is achieved by θ = 25°. Figure 1.2.2.2.2-13 shows the maximum stress at 25,000 rpm becomes 92,880 psi at the lower-right radius. The stress at the upper-left radius is 91,440 psi. Both values are closed.

Conclusion

Design 6 provides the best results, with the margin of safety about 21.8% based upon the ratio of fatigue strength to equivalent cyclic stress. The equivalent cyclic stress is converted from a stress cycle (0 to the maximum principal stress at the corner of the pole root). Design 6 is originally suggested for the conditioned power system.

Current Rotor Designs

A novel generator design concept has emerged for the conditioned power system since the proposal. This involves current rotor design changes. The overspeed is reduced to 15,000 rpm for current rotor design analysis. A summary of the current rotor design analyses for the conditioned power system is listed in Table 1.2.2.2.2-1. The details are described in the following paragraphs.

Design 7 (R = 0.040 Inch)

The inside-out rotor concept involves a larger rotor lamination than previous designs. This is required to accommodate the PMG and the exciter inside the rotating shaft. The OD of the rotor lamination is 10.0 inches and the ID is 6.65 inches (Figure 1.2.2.2.2-14). The thickness of the yoke is 0.45 inch. Twenty-one turns of C.091 inch diameter wires are simulated by square cross-section elements with proper boundry condition to maintain the movement to the right during rotating. An aluminum wedge is used.

Figure 1.2.2.2.2-14 also shows the distorted geometry at 15,000 rpm. At this speed, the maximum shear at the corner of the pole root is 159,000 psi, which is greater than the yielding (Figure 1.2.2.2.2-15).

Design 8 (R = 0.040 Inch)

Twenty-two turn wires are rearranged into four columns (Figure 1.2.2.2.2-16). This makes the yoke of the punching thicker (0.75 versus 0.45 inch).

Figure 1.2.2.2.2-17 also shows the distorted geometry at 15,000 rpm. Figure 1.2.2.2.2-17 shows the maximum stress at the corner becomes 95,860 psi, which is less than the yielding.

Design 9 (R = 0.049 and θ = 30°)

To save weight, design 9 splits the stress concentration into two radii (R = 0.049 inch) around the pole root. A straight portion with θ = 30° from horizon connects two radii (Figures 1.2.2.2.2-18 and 1.2.2.2.2-19). The thickness of yoke becomes 0.675 inch. The reduction in yoke thickness is compensated by the increase in the aluminum wedge thickness.

Figure 1.2.2.2.2-19 also shows the distorted geometry at 15,000 rpm. Figure 1.2.2.2.2-19 shows the maximum stress at the corner is 95,750 psi.

Conclusion of the Current Rotor Designs

Results of the three current designs are summarized in Table 1.2.2.2.2-1 Design 9 provides the best margin of safety (18.1%). Moreover, the results are compared with those of AV-8B and F-20 designs. Design 9 is the best. Therefore, Design 9 is suggested for the conditioned power system.

TABLE 1.2.2.2-1 - Summary of Rotor Designs for
the Conditioned Power System (CPS) versus AV-8B and F-20

ROTOR DESIGN	I.D. OF YOKE (IN)	CHARACTERISTIC RADIAL LENGTH OF YOKE (IN)	AVERAGE YOKE STRESS		POLE ROOT RADIUS (IN)	FLAT		CORNER STRESS		EQUIVALENT CYCLIC STRESS (1) (KSI)	MARGIN OF SAFETY (2) (%)
			IN VON MISES (KSI)	IN MAX PRINCIPAL (KSI)		LENGTH (IN)	ANGLE (DEGREE)	IN VON MISES (KSI)	IN MAX PRINCIPAL (KSI)		
Design 1	2.650	.430	72.0	73.6	.040	--	--	135.8	141.4	±100.0	- 20.0
Design 2	2.650	.430	70.9	72.9	.040	--	--	124.5	127.1	± 89.9	- 11.0
Design 3	3.176	.450	62.8	62.3	.040	--	--	127.3	129.6	± 91.6	- 12.7
Design 4	3.176	.450	60.7	61.4	.048	.076	30	93.5	98.3	± 69.5	15.1
Design 5	3.176	.450	60.9	61.4	.048	.076	20	97.7	100.9	± 71.3	12.1
Design 6	3.175	.450	60.8	61.4	.048	.076	25	88.8	92.9	± 65.7	21.8
Design 7	6.650	.450	77.0	80.0	.040	--	--	153.1	159.1	±112.5	- 28.9
Design 8	6.650	.750	59.1	60.3	.040	--	--	88.9	95.9	± 67.8	18.0
Design 9	6.650	.675	63.5	64.5	.049	.076	30	91.9	95.8	± 67.7	18.1
AV-8B	2.650	.415	46.4	47.0	.040	--	--	96.6	101.1	± 71.5	11.9
F-20	3.000	.413	53.0	53.3	.040	.030	20	93.6	96.8	± 68.4	17.0

NOTES: (1) Based upon the corner stress in Max. principal

(2) Margin of Safety = $\dfrac{\text{Fatigue Limit (80KSI)}}{\text{Equivalent Cyclic Stress}} - 1$
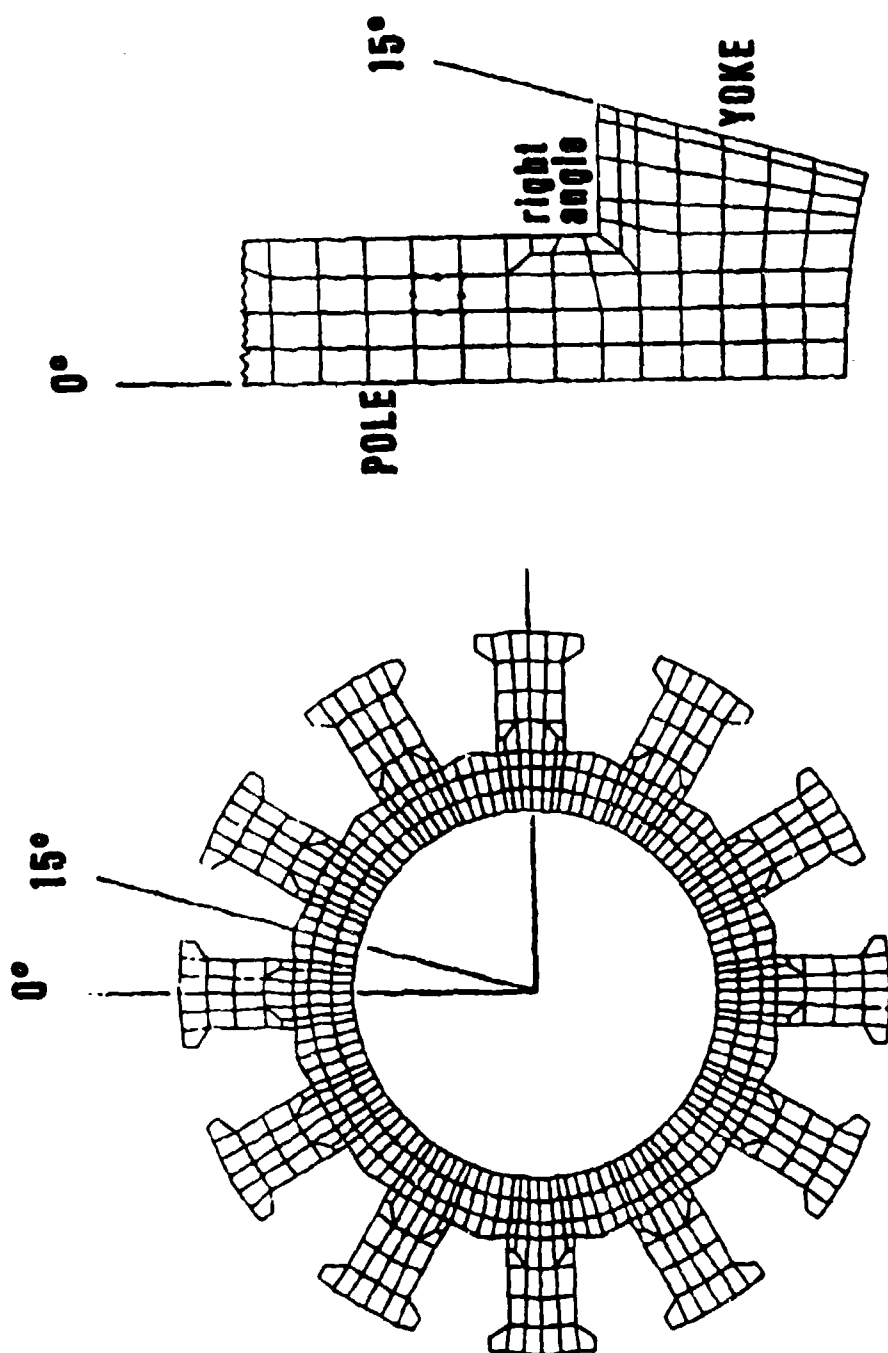
Figure 1.2.2.2.2-1

Twelve Pole Lamination

0.0035″

0.0050″

O.D.= 6″

0.788″
8 × .096
2 × .010

W = 25,000 rpm

R = 0.060

0.0031″

I.D. = 2.650″

CONDITION POWER SYSTEM ROTOR
SUPERB POST PLOT NO. 1
DISTORTED GEOMETRY   82/05/27   10.33.48

Figure 1.2.2.2.2-2

Design 1

ω = 25,000 rpm

141,977 psi

SUPERB POST PLOT NO. 3

CONTOUR INTERVAL = 17000.00

CONTOUR CONTOUR
NUMBER   LEVEL
1   -34000.0
2   -17000.0
3   .0000000
4   17000.00
5   34000.00
6   51000.00
7   68000.00
8   85000.00
9   102000.0
10   119000.0
11   136000.0

CONDITION POWER SYSTEM 83°CR
SUPERB POST PLOT NO. 3   82/05/27   10.23.49
MAX PRINCIPAL STRESS

Figure 1.2.2.2.2-3
Design 1 (R = 0.040")
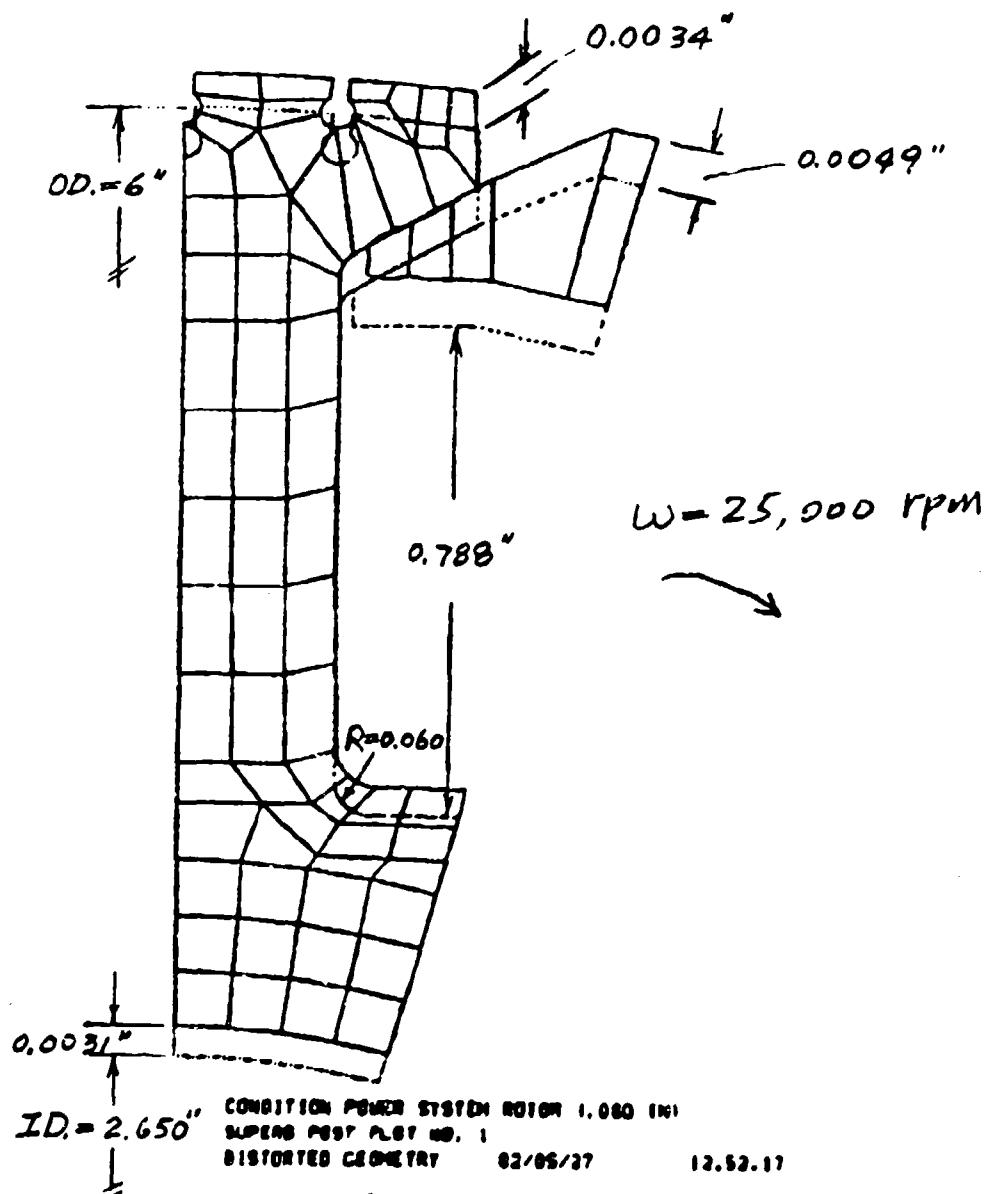
Figure 1.2.2.2.2-4

Design 2
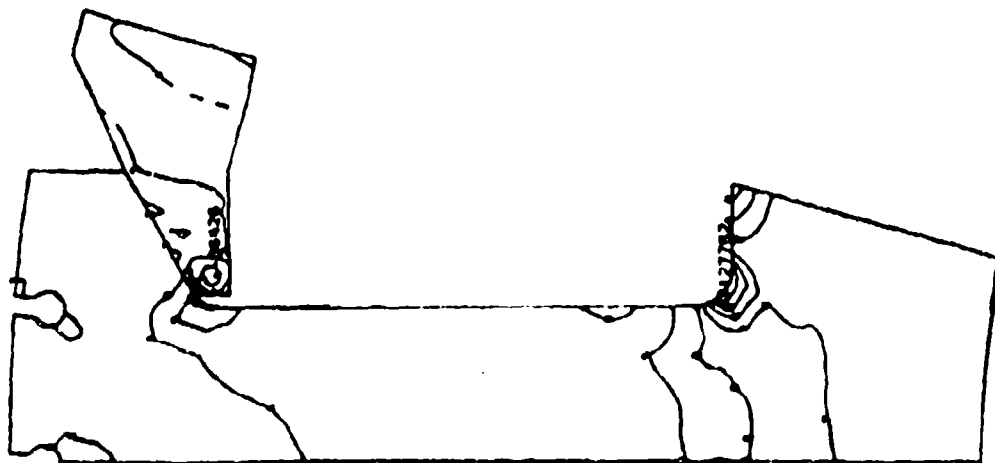
ω = 25,000 rpm

127,760 psi

SUPERB POST PLOT NO. 3

CONTOUR INTERVAL - 16000.00

| CONTOUR | CONTOUR |
NUMBER	LEVEL
1	-32000.0
2	-16000.0
3	.0000000
4	1600.00
5	32000.00
6	48000.00
7	64000.00
8	80000.00
9	96000.00
10	112000.0
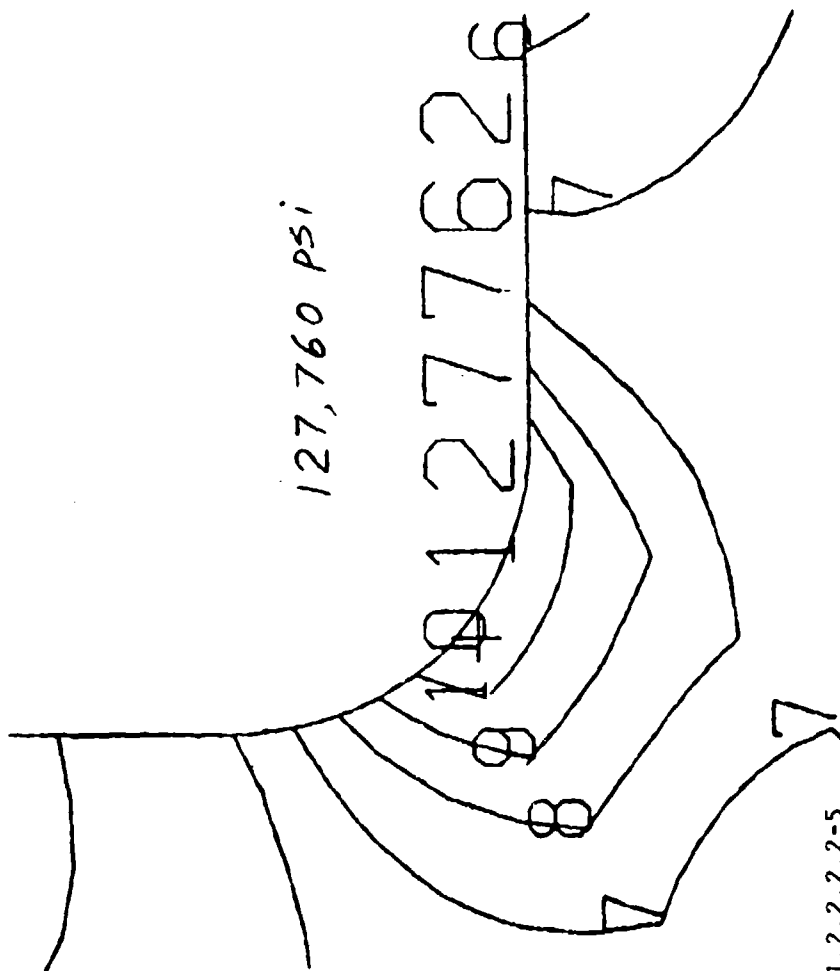
CONDITION POWER SYSTEM ROTOR (.060 IN)
SUPERB POST PLOT NO. 3
MAX PRINCIPAL STRESS 82/05/27   12.52.17

Figure 1.2.2.2.2-5

Design 2 (R - 0.060 Inch)
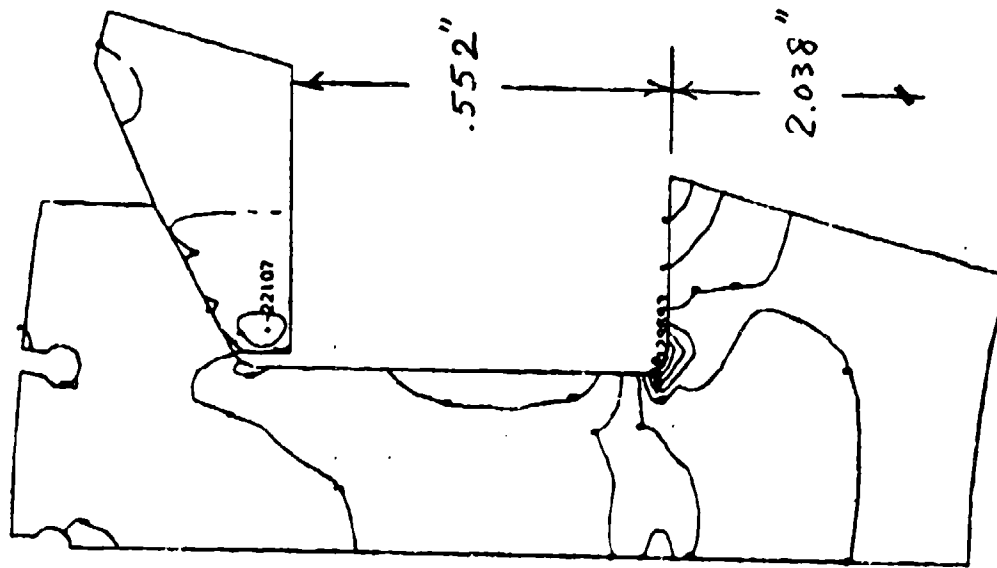
1-42

ω = 25,000 rpm

0.0033"

OD. = 6"

.0043"

.552"

7 × .076" Dia.
2 × .010 Ins.

R = .040"

2.038"

.0032"

ID. = 3.176"   CONDITION POWER SYSTEM ROTOR 1 1.000 INI
SUPERB POST PLOT NO. 1
DISTORTED GEOMETRY   02/05/28   16.58.33

Figure 1.2.2.2.2-6

Design 3

1-43

129,690 psi

ω = 25,000 rpm

SUPERB POST PLOT NO. 3

CONTOUR INTERVAL = 15000.00

CONTOUR CONTOUR
NUMBER LEVEL
1   -15000.0
2   .0000000
3   15000.00
4   30000.00
5   45000.00
6   60000.00
7   75000.00
8   90000.00
9   105000.0
10 120000.0

.552"

2.038"

CONDITION POWER SYSTEM ROTOR 1 1.DWG IN1
SUPERB POST PLOT NO. 3
MAX PRINCIPAL STRESS 82/05/28   14.56.23
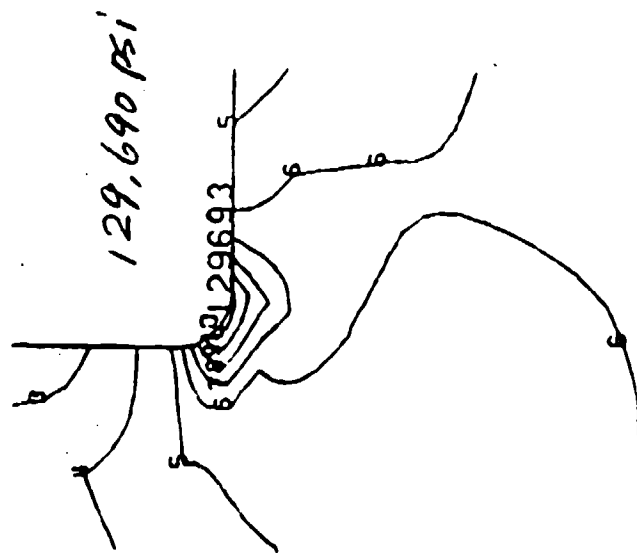
Figure 1.2.2.2.2-7

Design 3 (R = 0.040 Inch)
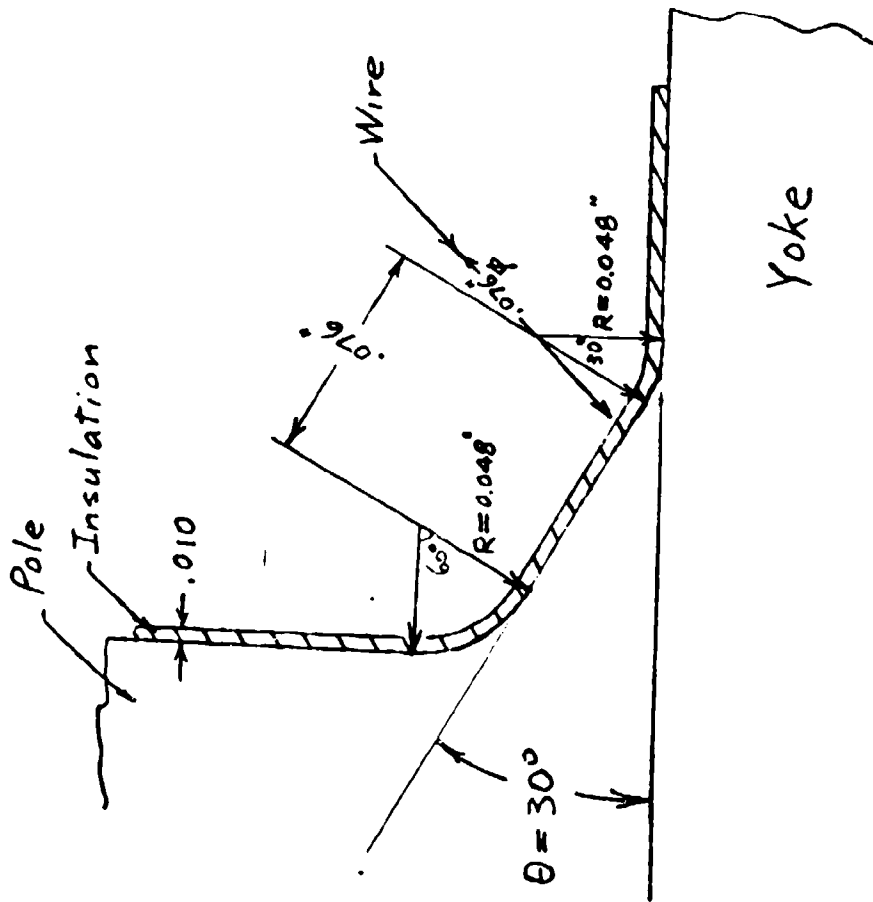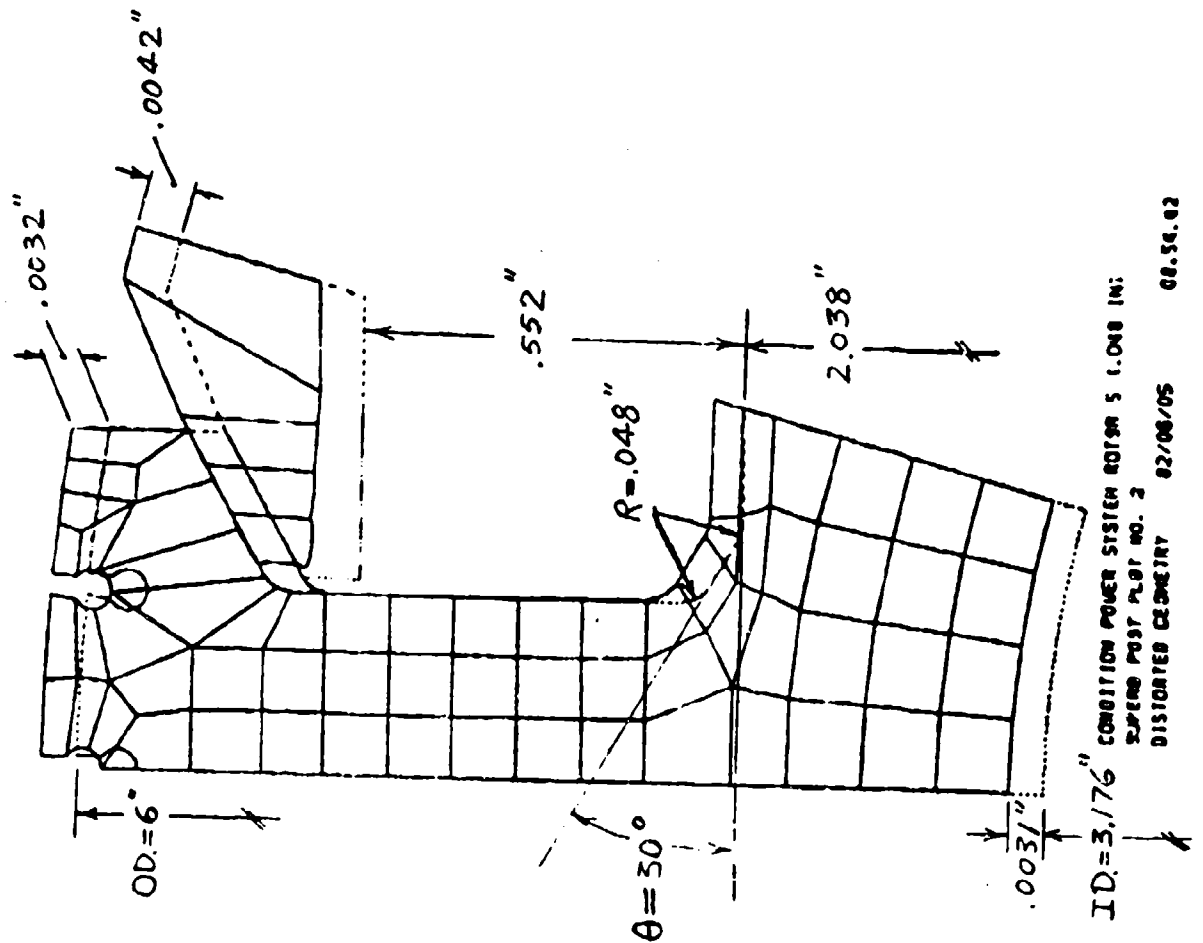
Figure 1.2.2.2.2-8
Design 4
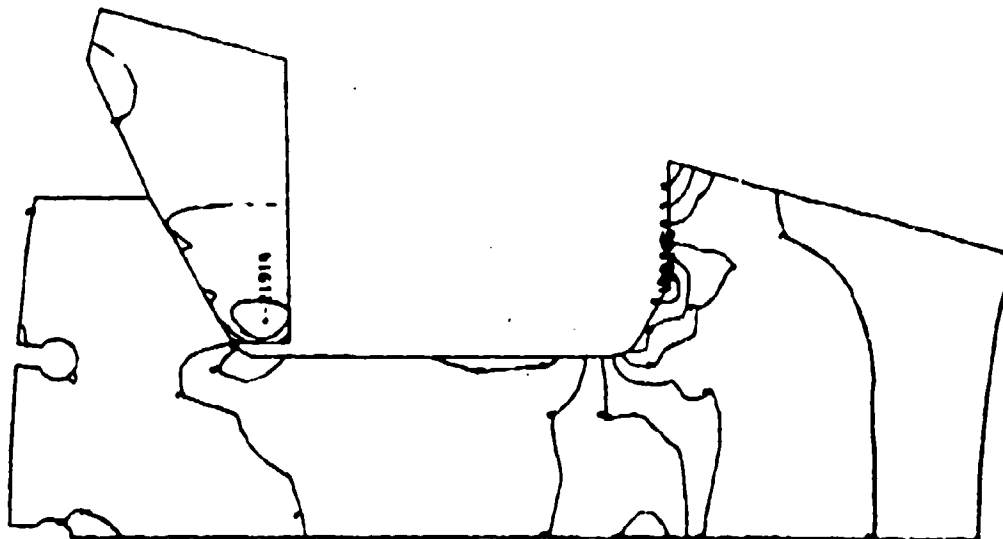
Figure 1.2.2.2.2-9

Design 4 (R = 0.048 Inch, θ = 30°)
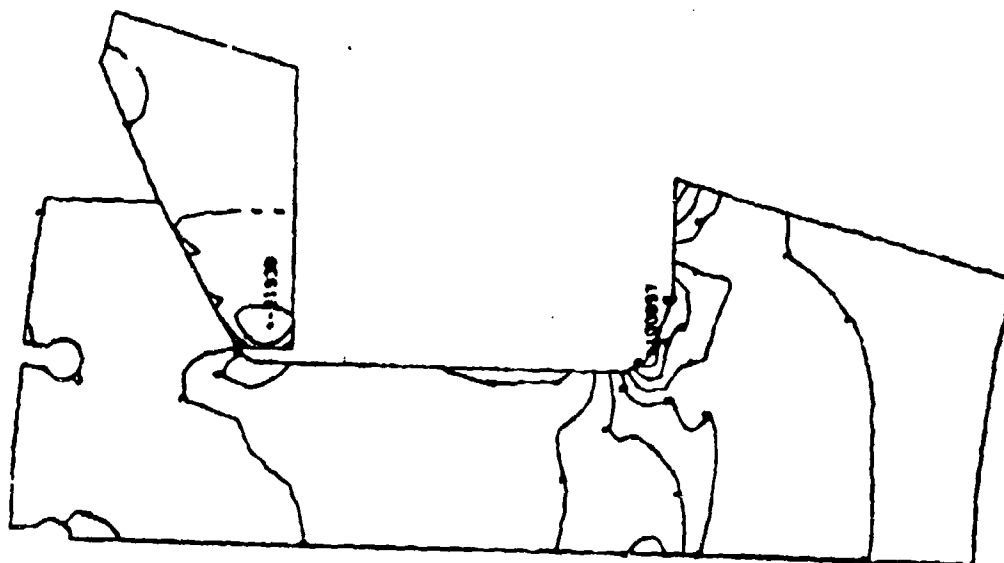
$\omega = 25,000$ rpm

OD.=6"

.0052"

.0042"

.552"

$\theta = 20°$

R=.048"

2.038"

.0031"

ID.=3.176"

CONDITION POWER SYSTEM ROTOR & 1.040 INI
SUPERB POST PLOT NO. 1
DISTORTED GEOMETRY   02/06/02   12.43.40

Figure 1.2.2.2.2-10

Design 5

$\omega = 25,000 \; rpm$

SUPER POST PLOT NO. 3

CONTOUR INTERVAL = 12000.00

CONTOUR NUMBER	CONTOUR LEVEL
1	-12000.0
2	.000000
3	12000.00
4	24000.00
5	36000.00
6	48000.00
7	60000.00
8	72000.00
9	84000.00
10	96000.00

100,900 psi

87,100 psi

CONDITION POWER SYSTEM ROTOR W 1.048 IN
SUPER POST PLOT NO. 3
MAX PRINCIPAL STRESS   02/05/82   12.40.40
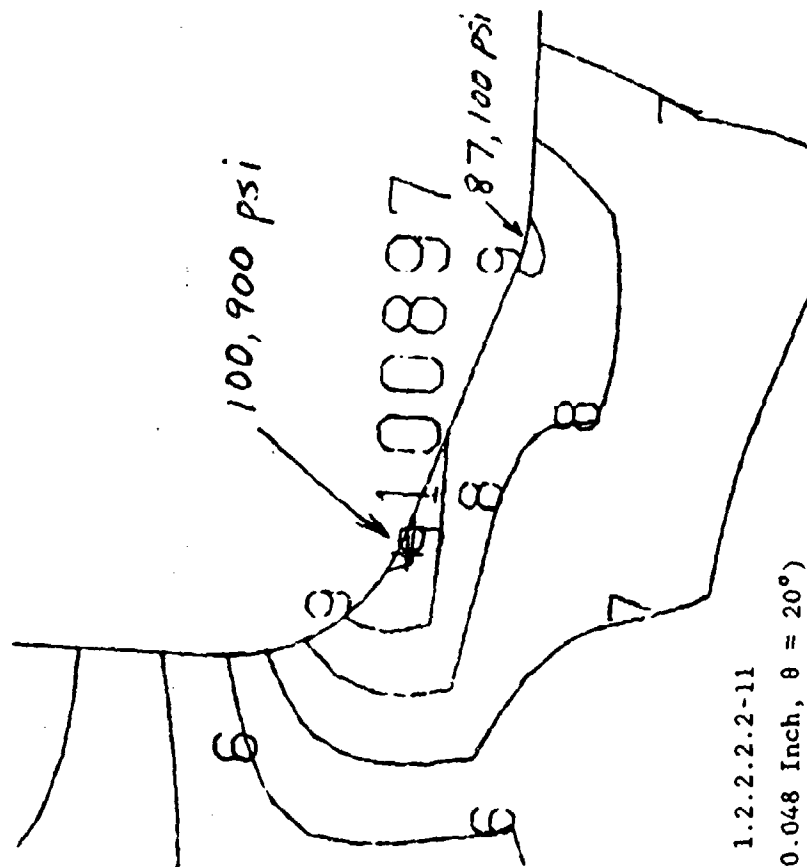
Figure 1.2.2.2-11
Design 5 (R = 0.048 Inch, θ = 20°)

1-48
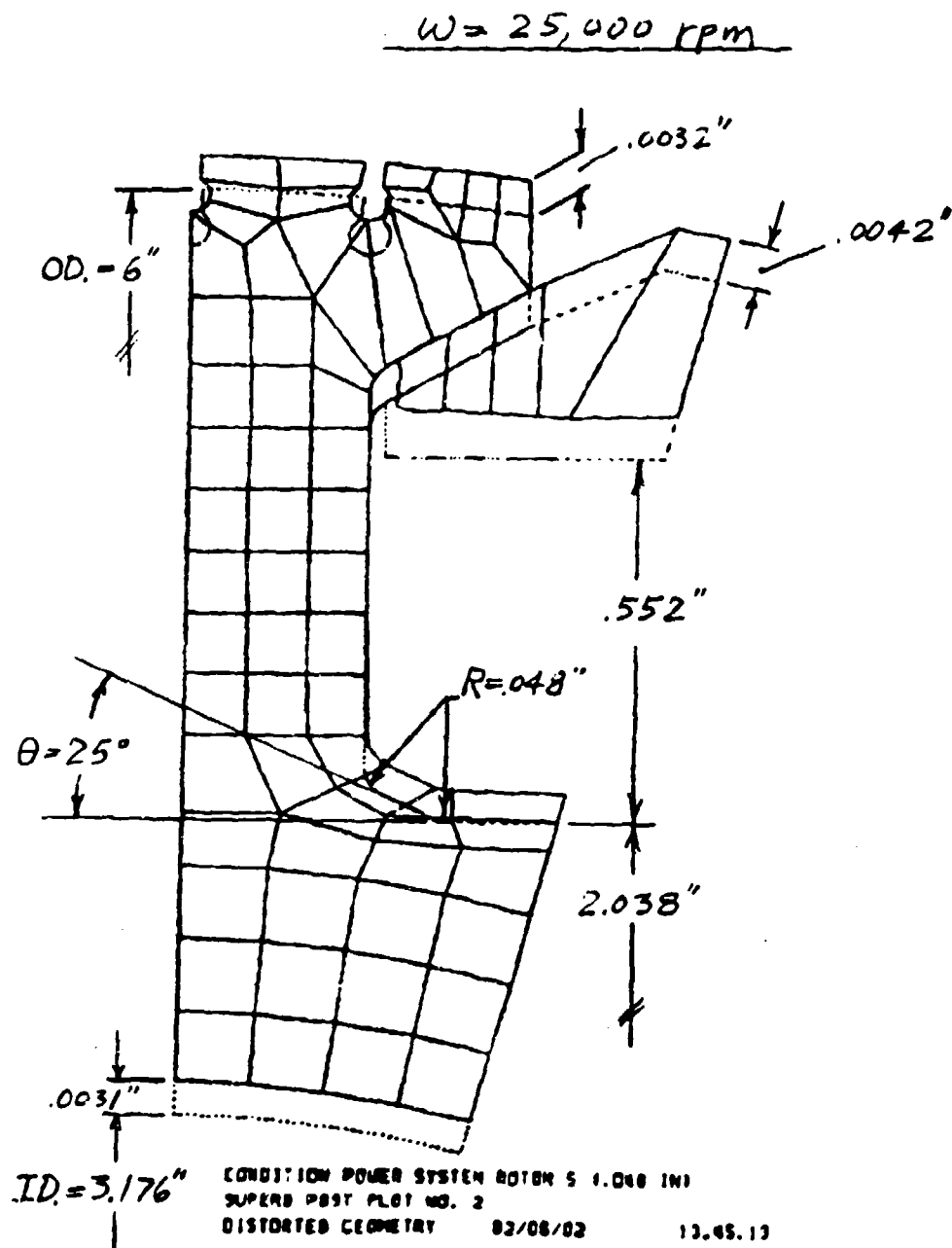
$W = 25,000$ rpm

Figure 1.2.2.2.2-12

Design 6
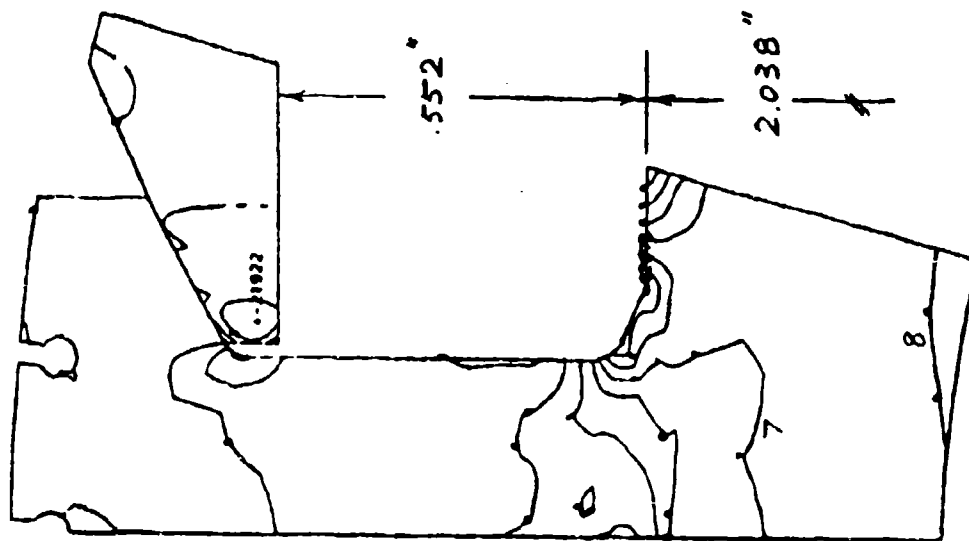
$\omega = 25,000$ rpm

SUPERB POST PLOT NO. 6

CONTOUR INTERVAL - 11000.00

CONTOUR NUMBER	CONTOUR LEVEL
1	-11000.0
2	.000000
3	11000.00
4	22000.00
5	33000.00
6	44000.00
7	55000.00
8	66000.00
9	77000.00
10	88000.00

92,680 psi

91,440 psi

.552"

2.038"

CONDITION POWER SYSTEM ROTOR S 1.048 INI
SUPERB POST PLOT NO. 4   82/08/83   13.05.13
MAX PRINCIPAL STRESS
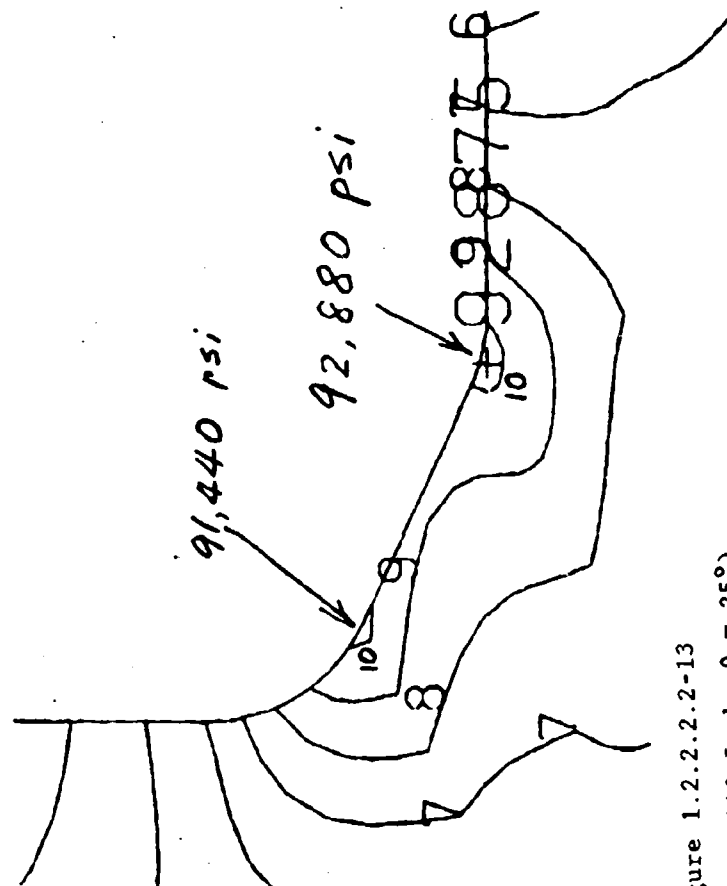
Figure 1.2.2.2.2-13
Design 6 (R = .048 Inch, θ = 25°)

1-50

AF 300 KVA ROTOR
(Design 7)
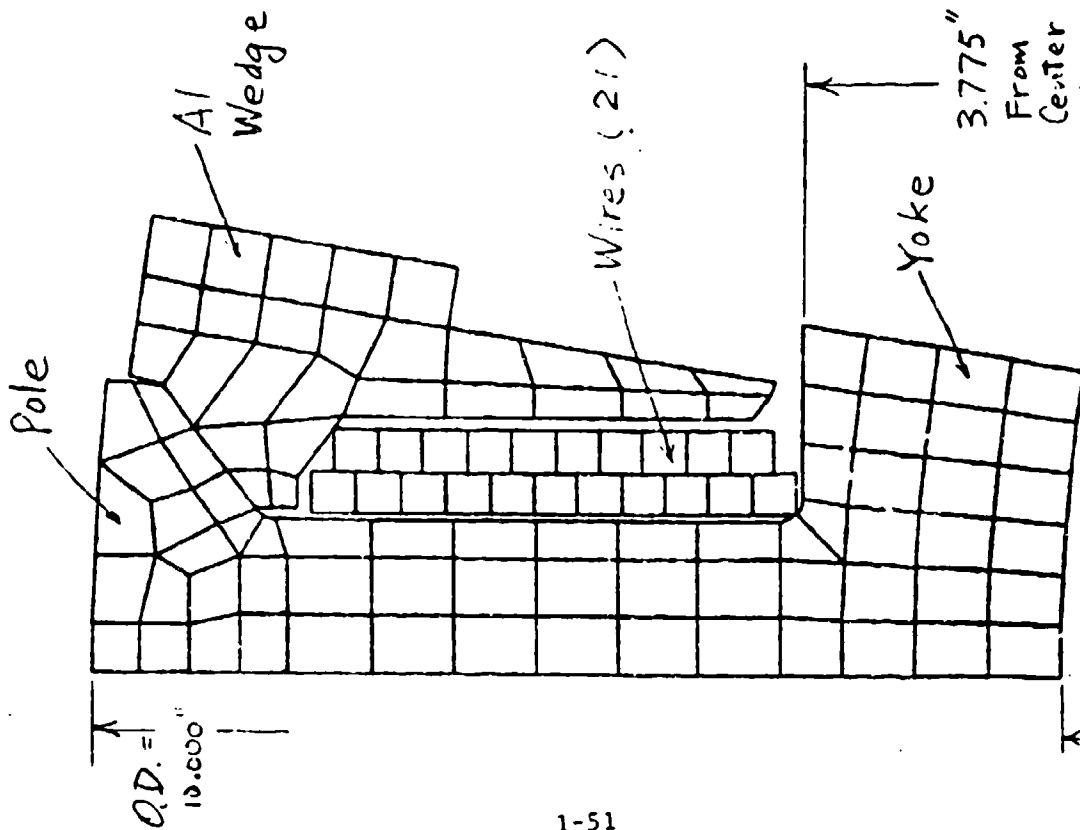
$\omega = 15,000$ RPM
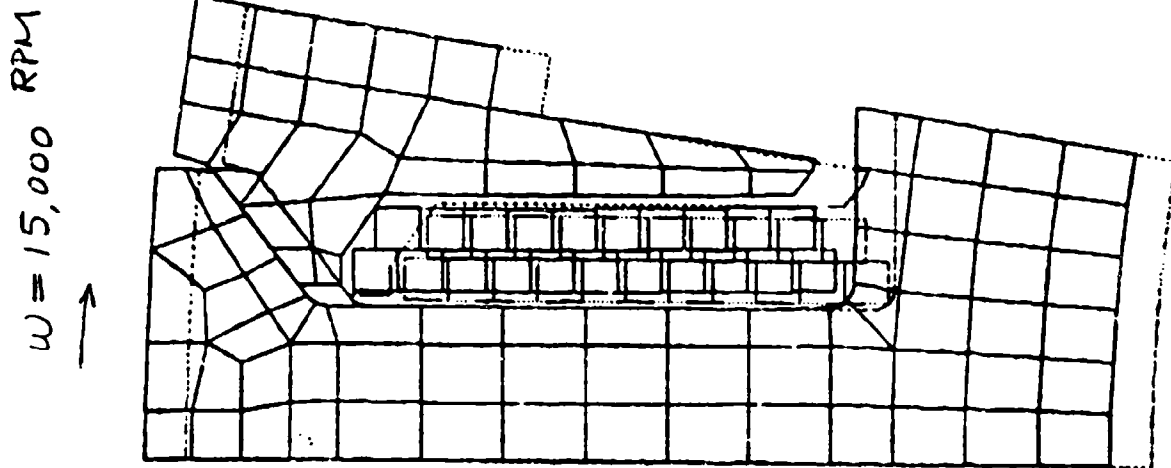
Pole

Al Wedge

Wires (2!)

Yoke

3.775" From Center Line

O.D.= 10.000"

I.D.= 6.050"

RF CONDITIONED SYSTEM ROTOR ASSEMBLY
SUPER POST PLOT NO. 1
DISTORTED GEOMETRY   83/03/28   10.02.28

RF CONDITIONED SYSTEM ROTOR ASSEMBLY
PLOT NO. 1

Figure 1.2.2.2-14
Design 7
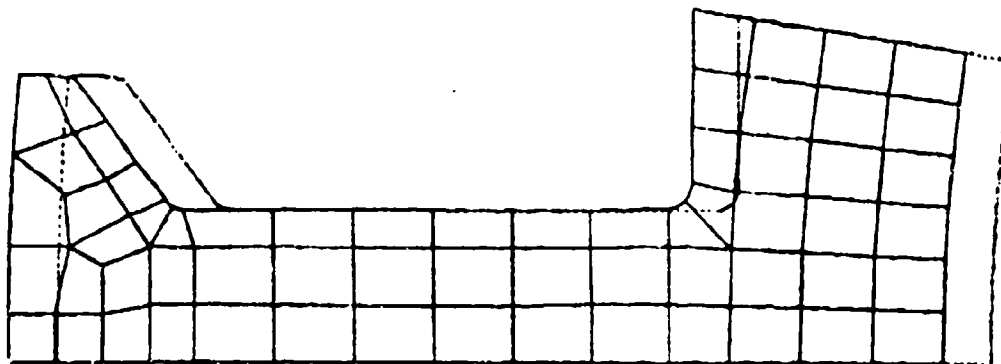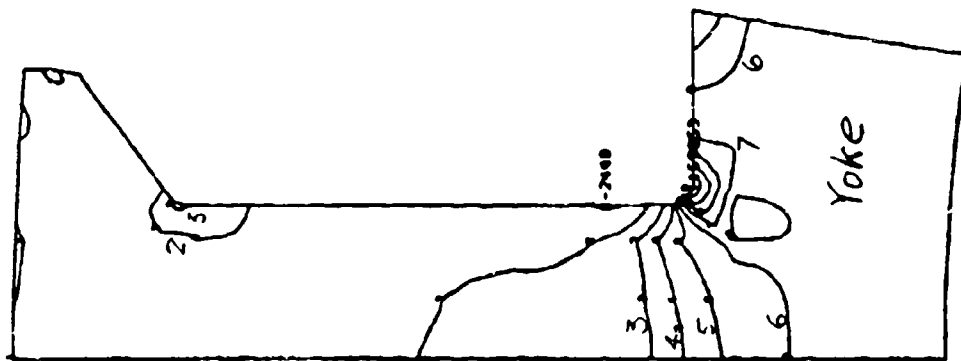
SUPER POST PLOT NO. 7

CONTOUR INTERVAL = 16000.00

CONTOUR CONTOUR
NUMBER LEVEL
1 .000000
2 16000.00
3 32000.00
4 48000.00
5 64000.00
6 80000.00
7 96000.00
8 112000.0
9 128000.0
10 144000.0

Yoke

AF CONDITIONED SYSTEM ROTOR ASSEMBLY
SUPER POST PLOT NO. 7
MAX PRINCIPAL STRESS   83/03/28

Figure 1.2.2.2-15

Design 7

$\omega = 15,000$ RPM

GF CONDITIONED SYSTEM ROTOR ASSEMBLY
SUPER POST PLOT NO. 5
DISTORTED GEOMETRY   83/03/28

AF 300 KVA ROTOR

(Design 8)

ω = 15,000 RPM

Figure 1.2.2.2.2-16
Design 8

1-53

SUPERB POST PLOT NO. 7

CONTOUR INTERVAL = 10000.00

CONTOUR CONTOUR
NUMBER LEVEL
1   -10000.0
2   .000000
3   10000.00
4   20000.00
5   30000.00
6   40000.00
7   50000.00
8   60000.00
9   70000.00
10   80000.00
11   90000.00

95,863 PSI

RF CONDITIONED SYSTEM ROTOR ASSEMBLY 2
SUPERB POST PLOT NO. 7
MAX PRINCIPAL STRESS   83/03/71

YOKE

ω = 15,000 RPM

.0066"

.0063"

RF CONDITIONED SYSTEM ROTOR ASSEMBLY 2
SUPERB POST PLOT NO. 5
DISTORTED GEOMETRY   83/03/71

Figure 1.2.2.2.2-17

Design 8

1-54

AF 500 KVA ROTOR

(Design 9)

Pole

Al Wedge

Wires (21)

4.000" From Center-Line

Yoke

ω = 15,000 RPM

O.D. = 10.000"

I.D. = 6.650"

Figure 1.2.2.2.2-18

Design 9

1-55

SUPERB POST PLOT NO. 7

CONTOUR INTERVAL = 10000.00

CONTOUR CONTOUR
NUMBER LEVEL
  1   -1000.0
  2   .000000
  3   10000.00
  4   20000.00
  5   30000.00
  6   40000.00
  7   50000.00
  8   60000.00
  9   70000.00
 10   80000.00
 11   90000.00

95,753 PSI

95,753 PSI

9510 57 53

7 8

NF CONDITIONED SYSTEM ROTOR ASS
SUPERB POST PLOT NO. 7
MAX PRINCIPAL STRESS   01/28/04

Figure 1.2.2.2.2-19
Design 9

ω = 15,000 RPM

.0069"

R = .045"

R = .045"

3.0°

.0900"

NF CONDITIONED SYSTEM ROTOR ASSEM
SUPERB POST PLOT NO. 5
DISTORTED GEOMETRY   03/04/04
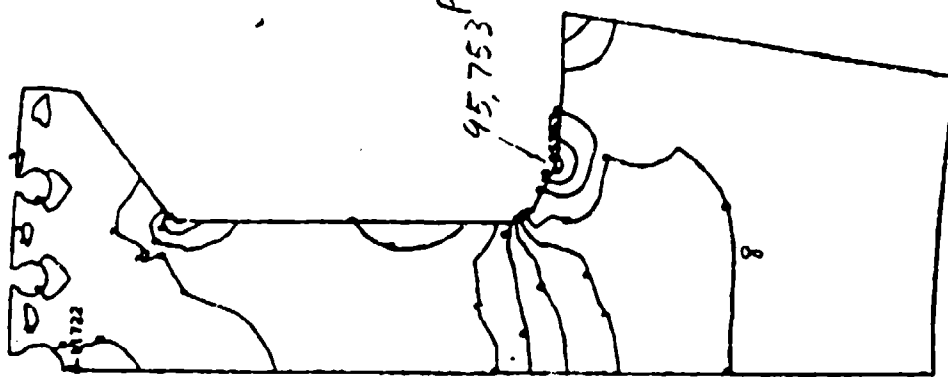
1.2.2.2.3   Thermal Rationale

For cooling considerations, it is desirable to have a short machine with a
short rotating field winding and a large number of poles. A long field
winding requires cooling passages and heat conduction paths within the array
of electrical conductors within the field winding. These provisions require
significant space, which reduces the space available for electrical turns
around each pole. In addition, a higher current density with higher losses
results when cooling passages and heat shunts are placed within the winding.
These complications are avoided if the field winding is kept short. In this
situation, most of the loss within the winding is conducted along the copper
wire to the ends of the winding. The remainder of the losses are conducted
axially along the wedges between the pole heads and radially through the steel
core. Cooling the winding is accomplished by spraying oil on the ends of the
winding and onto the ends of the wedges. This oil passes along the bore of
the hollow shaft before it is discharged onto the windings. Thus, it also
provides a heat sink for the losses conducted radially through the steel
core. The 20-pole machine shown in Figure 1.2.2.2.2-20 uses aluminum wedges
for containment of the windings, since the space between the pole heads is
0.528 inches (see Figure 1.2.2.2.2-21 and the bending stress and deflection
within the wedges is very low. These wedges provide conductive paths from the
center to the ends of the winding. A thermal analysis of the 6.9 inch long
field winding is shown in figures 1.2.2.2.2-22 and 1.2.2.2.2-23 indicates the
following:

Heat Conduction Paths for Field Winding Losses	Percent Loss
Radially through steel into the hollow shaft	28.8
Axially through wedges	25.1
Axially through copper conductors	
to the ends of the winding	46.1
Total	100.0

It can be noted from above that 71.2 percent of the field winding losses can
be removed by spraying oil on the ends of the winding.

1-57
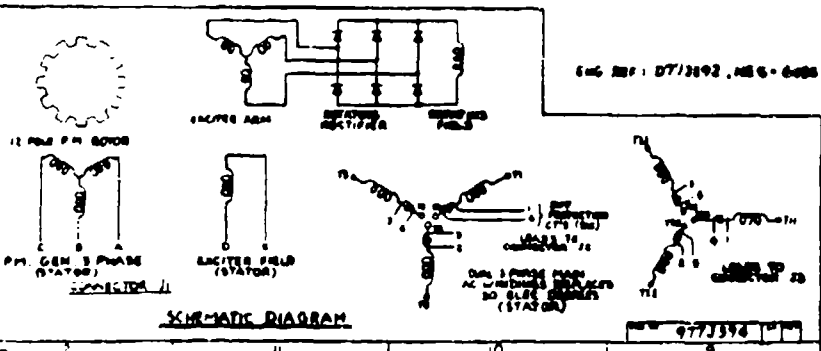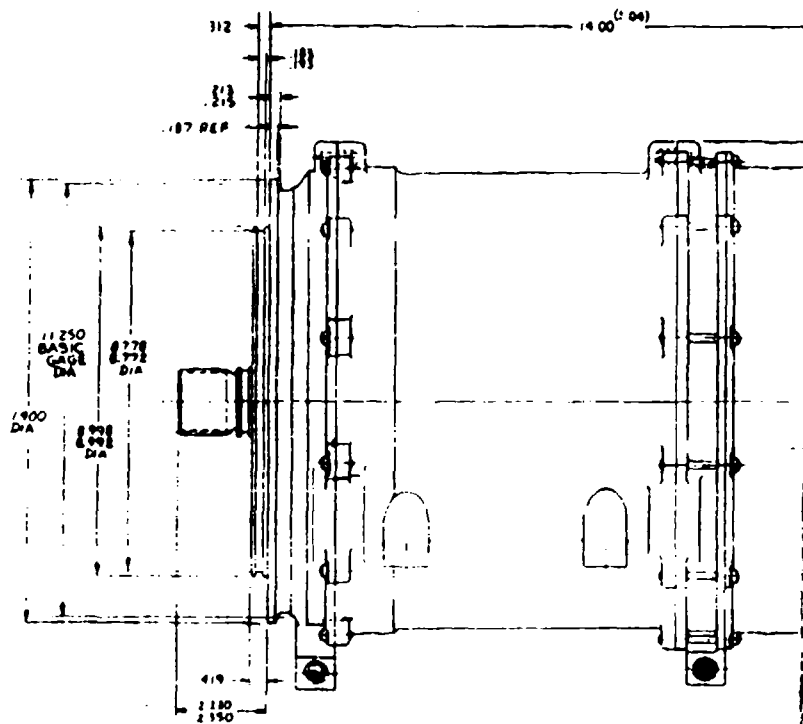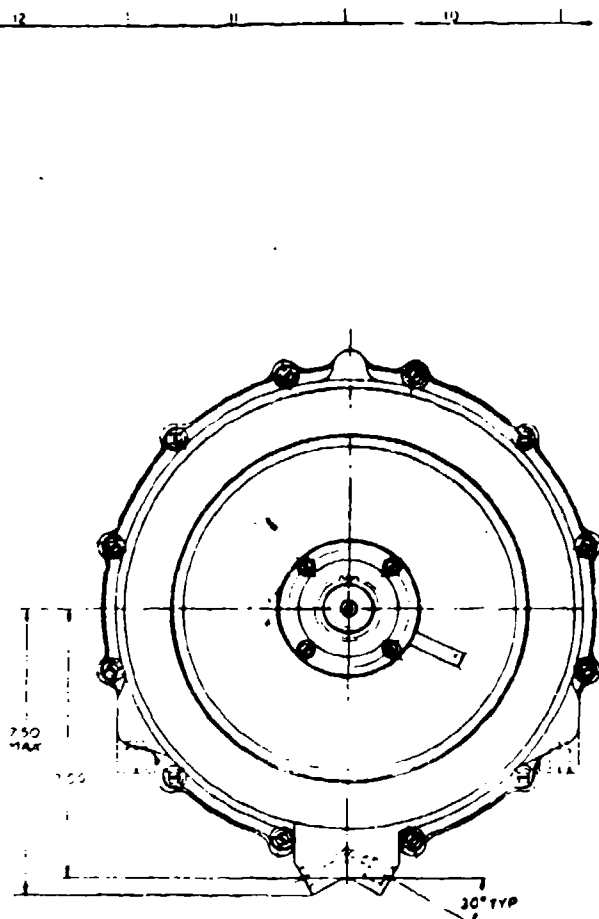
GENERATOR CHARACTERISTICS

AC BRUSHLESS GENERATOR, SPRAY/CONDUCTION OIL COOLED
DUAL 3 PHASE WINDINGS - 30° DISPLACED
1209/2500 Hz, OVERSPEED : 16500 RPM

SCHEMATIC DIAGRAM

30° TYP

PM GEN CONT RATING WHEN 3 Ø F.W. RECTIFIER (TYPICAL)

RPM	VOLTS DC	AMPS
	17 R DC	DC
7.227	57	30
15,000	116	30
15,000	155	0

INSTALLATION DRAWING FOR 977J393-1

OUTLINE

Figure 1.2.2.2.2-20
Twenty Pole Machine

1-58
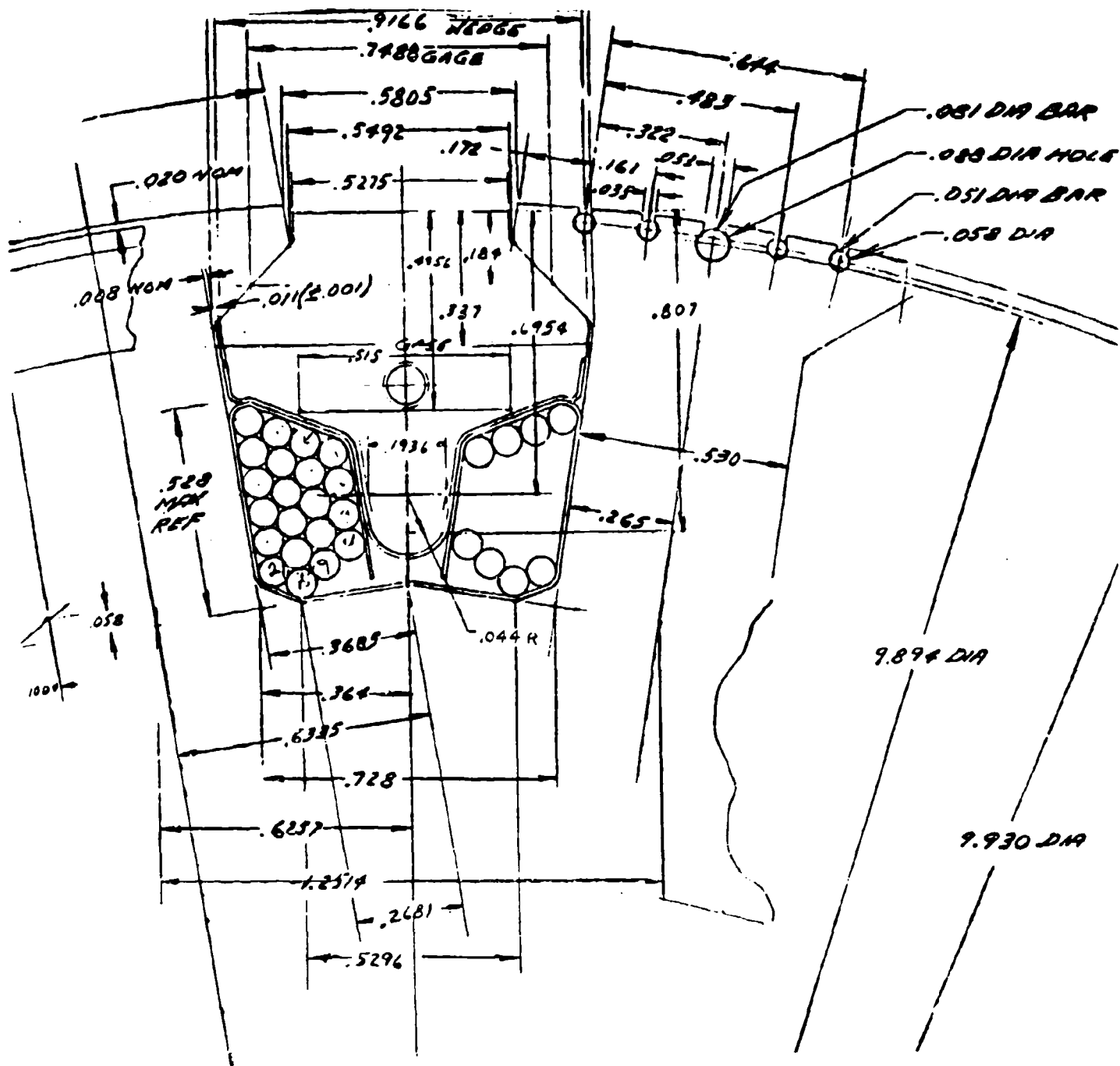
Figure 1.2.2.2.2-21

Pole Configuration, Twenty Pole Design

1-59
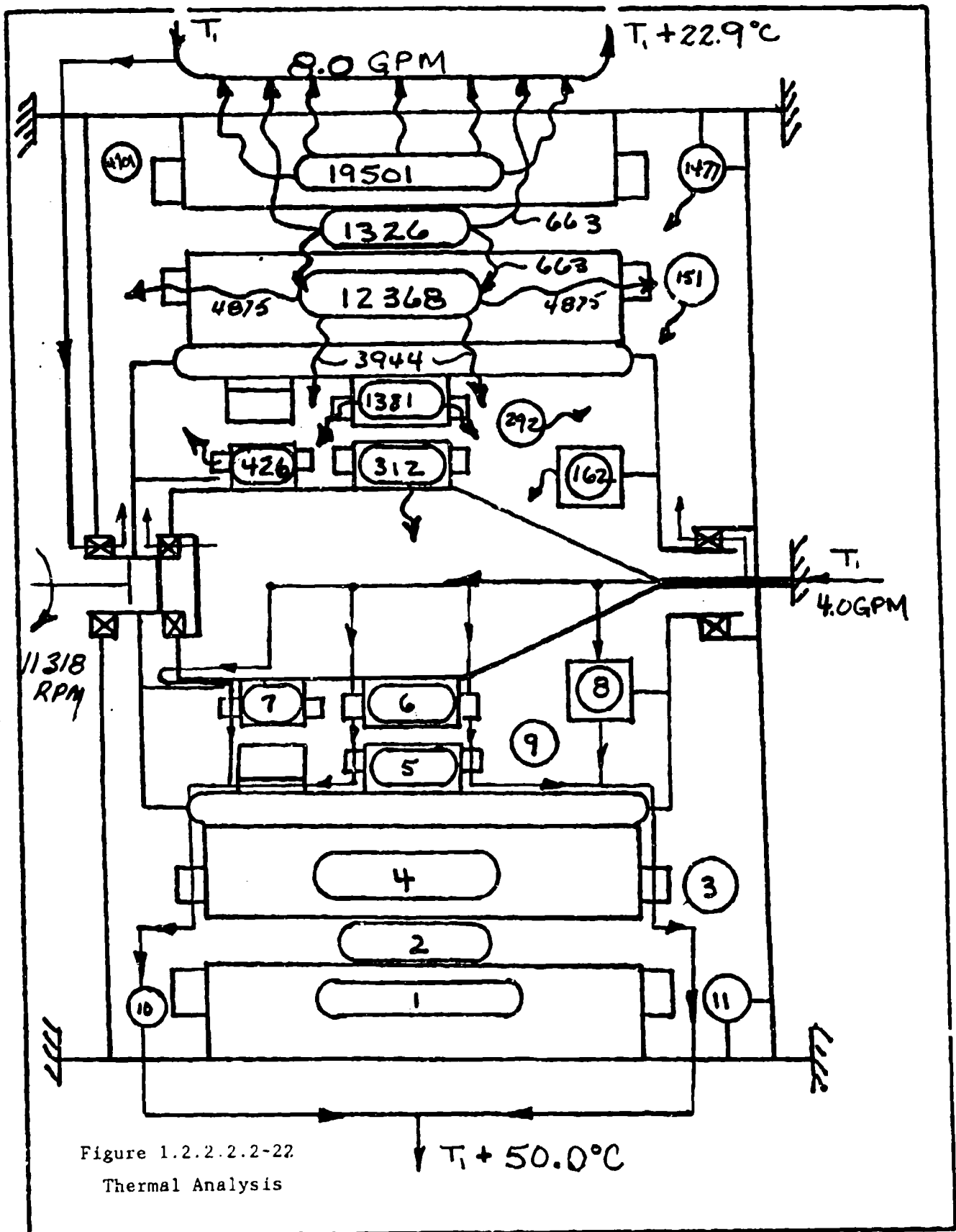
Figure 1.2.2.2.2-22
Thermal Analysis
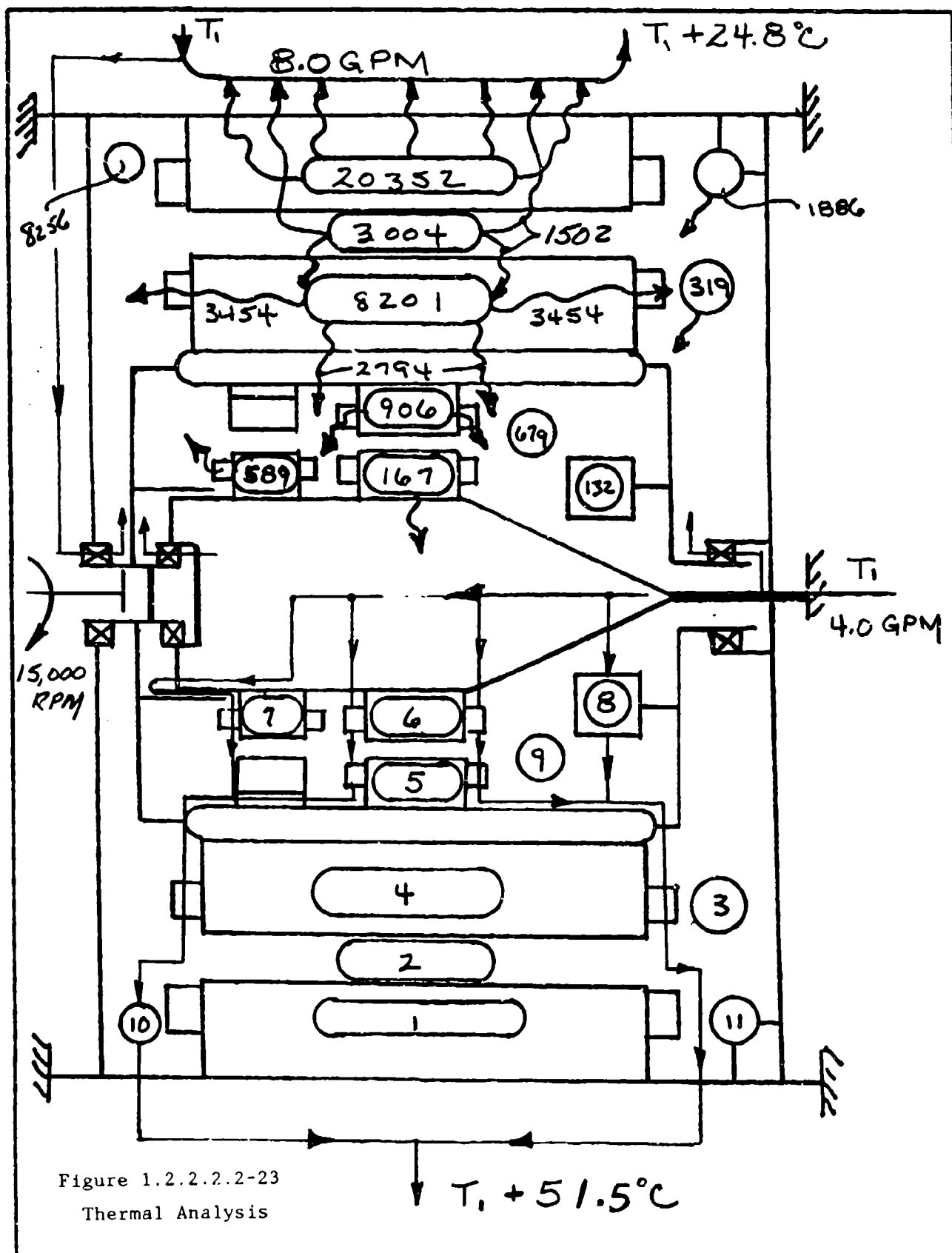
Figure 1.2.2.2.2-23
Thermal Analysis

1.2.2.2.3   Thermal Rationale   (Continued)

The remaining 28.8 percent of the field winding losses is conducted into the
hollow shaft that contains the permanent magnet generator, the exciter
generator, and the rotating rectifier assembly. The oil path for cooling
these components is illustrated in Figure 1.2.2.2.2-24. Nozzles on the
stationary central shaft are used to spray oil onto the rotating rectifier
assembly, the armature winding for the exciter generator. The stationary
winding for the permanent magnet generator is cooled by oil discharged from a
rotating sleeve under one end of the winding. After the oil passes around the
components within the hollow shaft, the coolant circuit splits and one-half of
the oil is sprayed onto the rotor windings to provide the major source of
rotor cooling. Oil leaving the rotor is collected in scrolls, which direct
the oil into a discharge port on each end of the unit.

The main generator stator is cooled by conduction of copper losses into the
stator iron and then with iron losses through the back iron and an aluminum
sleeve to the cooling oil. One-half of the windage loss in the rotor-stator
air gap is assumed to be conducted through the stator iron and into the stator
coolant.

1.2.3   400 Hertz AC

The 400-Hz-AC system converts the variable frequency, variable voltage input
from the generator to constant voltage, constant frequency 400 Hz power.

This is accomplished by converting the generator power to DC power, which is
then fed to a three-phase inverter that provides the constant frequency output.

As the inverter is controlled to a programmed waveform, the inverter output
voltage is proportional to the DC-link voltage. This, then predicates use of
a preregulator of the DC-link voltage to maintain a regulated output of the
400 Hz system.
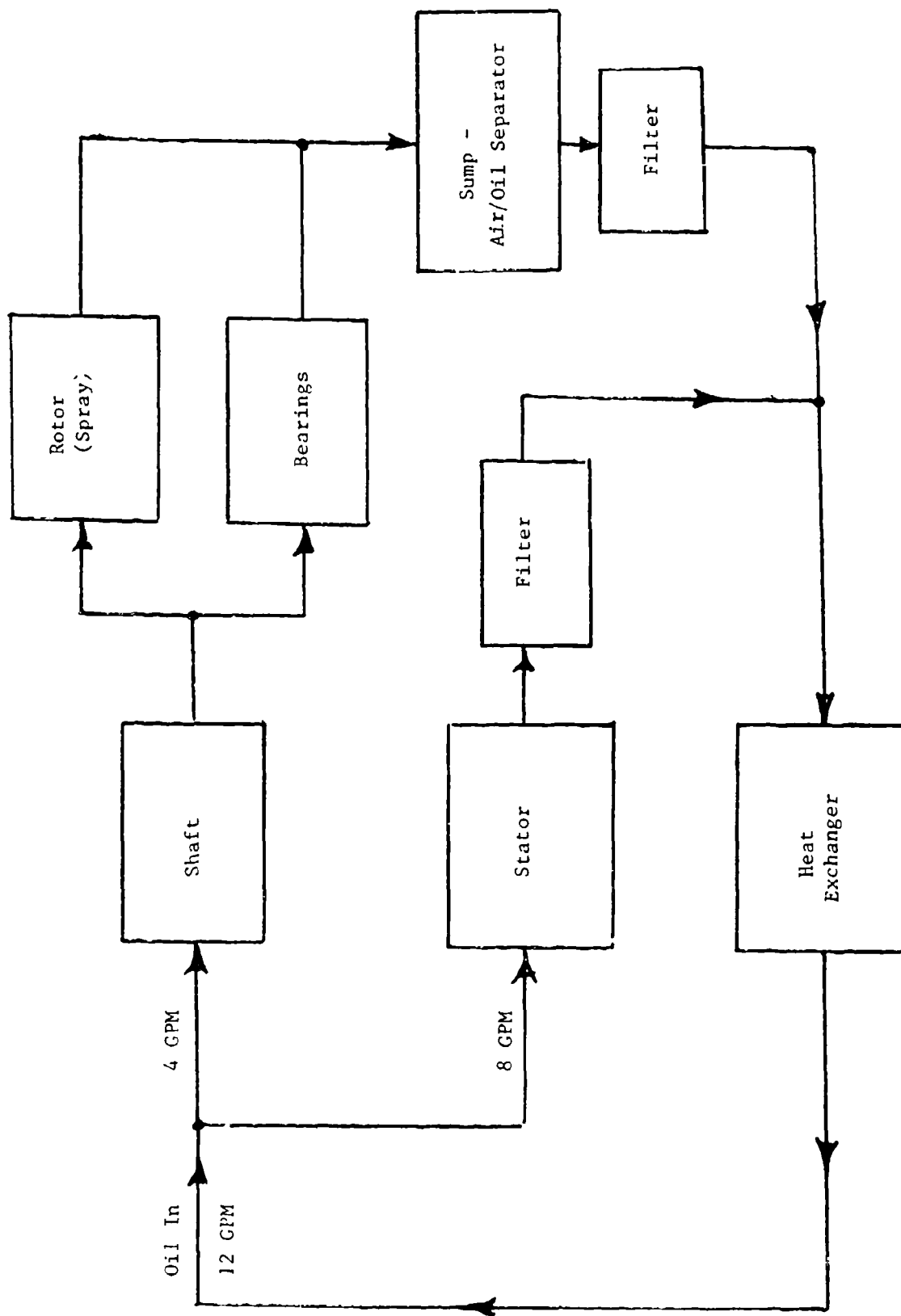
Figure 1.2.2.2.2-24
Generator Oil Cooling Path

1.2.3   400 Hertz AC (Continued)

The simplified block diagram of Figure 1.2.3-1 illustrates the basic
configuration of the system. The output voltage is sensed, compared to a
reference, and the error signal is then processed through the pre-regulator,
which controls the controlled-rectifier bridge. This bridge is controlled to
maintain the output voltage constant, varying the DC-Link output voltage to
correct for the voltage drops in the inverter and filter as a function of load.

The following paragraphs discuss these elements in further detail.

1.2.3.1   Preregulator

In the Westinghouse DC-Link VSCF systems, the 400 Hz output voltage is
generated by a "fixed pattern" pulse width modulated inverter. With fixed
pattern, the output voltage level control is not provided through the inverter
power circuit. The output voltage level of the inverter is controlled by
adjusting its DC-Link input voltage level. Regulation may be accomplished by
controlling either the generator voltage level via a "conventional" generator
regulator in response to feedback from the inverter 400-Hz output, or the
output DC voltage of a preregulator between the generator and the inverter.

The generator output voltage level cannot be field controlled to establish the
correct link voltage because multiple systems are connected to this generator
output. Therefore, a preregulator is used between the generator and the
inverter to establish the correct link voltage. A link voltage demand signal
from the inverter controls the preregulator output.

The preregulator must accommodate an almost two-to-one variation in generator
voltage. It also must compensate for a 25% voltage drop across the link
filter, which is a function of load current magnitude and power factor.
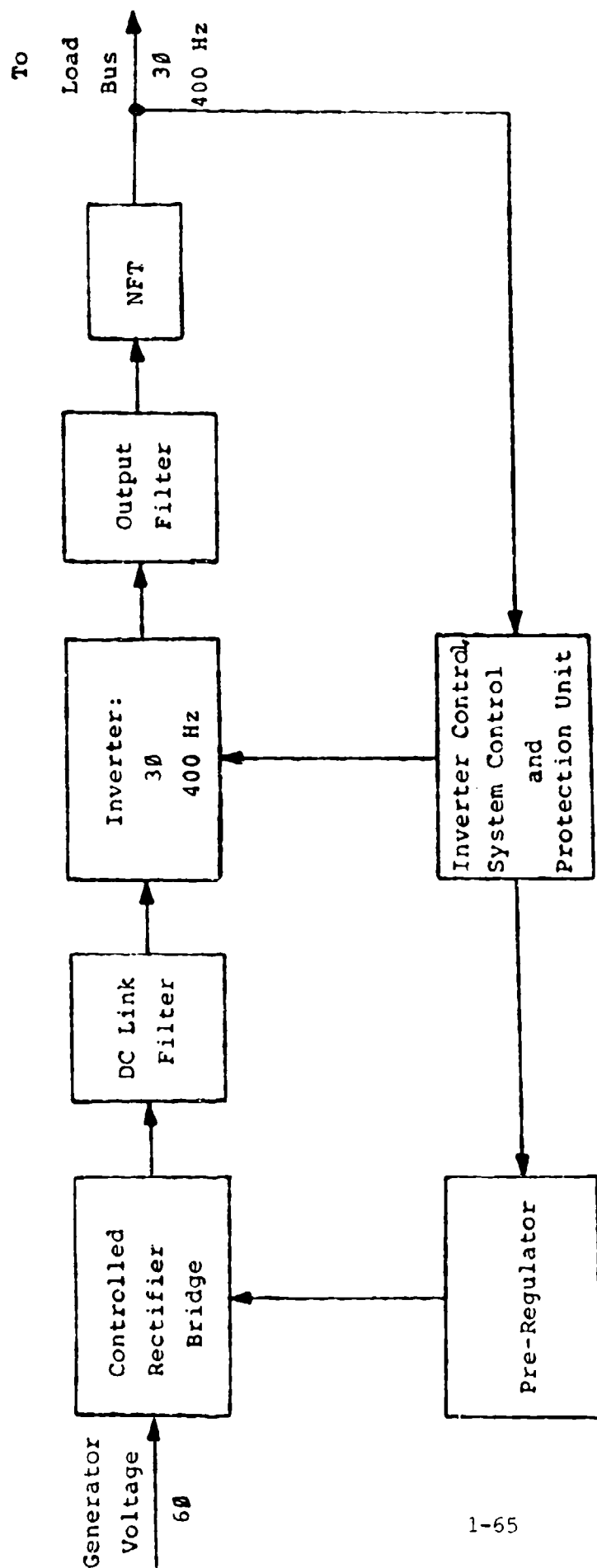
Figure 1.2.3-1

Block Diagram for 400 Hz AC Electrical System

1.2.3.1   Preregulator   (continued)

The preregulator design requirements are as follows:

1.   Input Voltage Range: 140 to 260 RMS L-N
2.   Input Configuration: Six-Phase (Two Three-Phase Sets Staggered 30°)
3.   Input Frequency: 1,208 Hz to 2,500 Hz
4.   Output Voltage: Controllable from 250 VDC to 315 VDC
5.   Output Ripple: 1% P-P (Goal)
6.   Filter: Compatible with Existing 600 μF Link Capacitor
7.   Response Time: Open Loop Approximately .25 Millisecond

The preregulator is designed to provide this performance as well as the
voltage control necessary for paralleling of the 400 Hz channels. Of the
available techniques, the controlled rectifier appeared the best suited to the
application. It serves the double function of rectifying the generator AC
voltage to DC for the DC-Link inverter and controlling the level of DC voltage
into the inverter independently of the generator voltage level. Other DC type
preregulator concepts were considered such as:

1.   rectifier plus transistor buck regulator;
2.   rectifier plus SCR buck regulator;
3.   rectifier plus transistor boost; and
4.   rectifier plus SCR boost regulator.

The SCR regulators have the disadvantage of requiring bulky complex
commutation circuits and are not weight or cost competitive. The transistor
regulators require a device, preferably a single device, capable of switching
up to 180 KVA of power and such devices are not yet available.

The major components of the preregulator are shown in Figure 1.2.3.1-1.
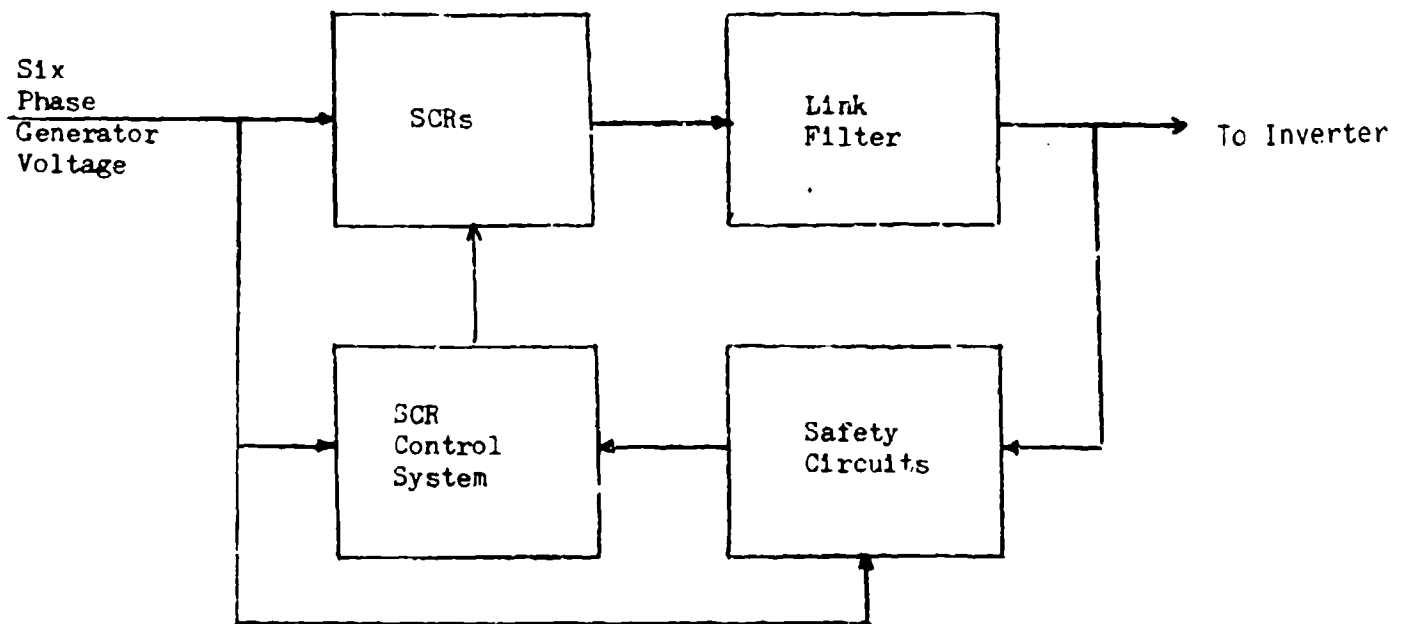
Figure 1.2.3.1-1

Preregulator Major Components

1-67

1.2.3.2 Preregulator Link Filter

It is a design goal that the DC-Link voltage have no more than 1% ripple contribution from the generator/rectifier/preregulator so that distortion, modulation, etc., meet specification requirements. Hence, filtering the preregulator output is necessary. Some filter inductance will be necessary between the preregulator and an existing link capacitor. (In the preregulator design this inductance is designed into the interphase transformer.)

The size of the filter inductor is important because excessive inductance results in a poor response time through the preregulator. It is desirable to have this response time at least similar to a conventional VSCF generator so that regulation, loop stability, response time, etc., meets system performance requirements. If the preregulator response time is approximately ten times faster than the generator feeding the preregulator, then the effects of the preregulator become insignificant. If, on the other hand, the response time is approximately equal to that of the generator, a classic second order (or higher) servo system exists, with great potential for instability. Hence, the design goal was to provide a response time for the preregulator of ten times faster than a typical VSCF generator. Two to three milliseconds is a typical open loop response time for a VSCF generator; therefore, the design goal was 0.2 to 0.3 millisecond for the preregulator.

A computer model of a twelve-pulse converter illustrates its ripple characteristics. Figure 1.2.3.2-1 shows the output of a twelve-pulse converter using a four microhenry link inductor. The ripple is 1.1% peak-to-peak. The transient response of approximately 0.3 millisecond is shown in Figure 1.2.3.2-2. Both the ripple and transient response of this design are acceptable for the preregulator at 1,892 Hz and full load. Other speeds are shown in Figures 1.2.3.2-3 and 1.2.3.2-4. The ripple for these two cases is 1.25% and 1.20%, respectively.

508 V.   # 12 PULSE CONVERTER SIMULF.FION, Vlink vs. Time*

Link Inductor   ~ 4 uhy.
Link Capacitor ~ 800 uf.
Link Load   ~ 120 kw.
Link Voltage   ~ 300 volts
Fgen   ~ 1892 hz.
Vgen   ~ 240 volts

.083
Sec.
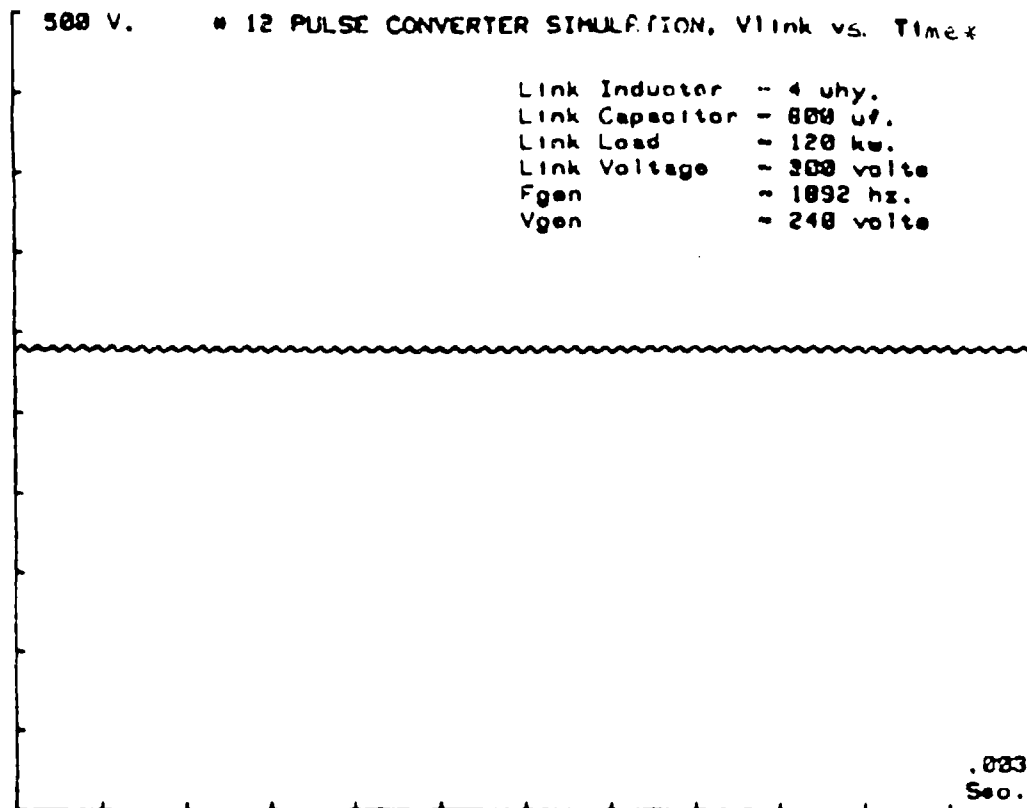
Figure 1.2.3.2-1

Twelve Pulse Converter Ripple (1.1%)

500 V.   * 12 PULSE CONVERTER SIMULATION, Vlink vs. Time *

Link Inductor	- 4 uhy.
Link Capacitor	- 600 uf.
Link Load	- 120 kw.
Link Voltage	- 300 volts
Fgen	- 1892 hz.
Vgen	- 240 volts

.003
Sec.
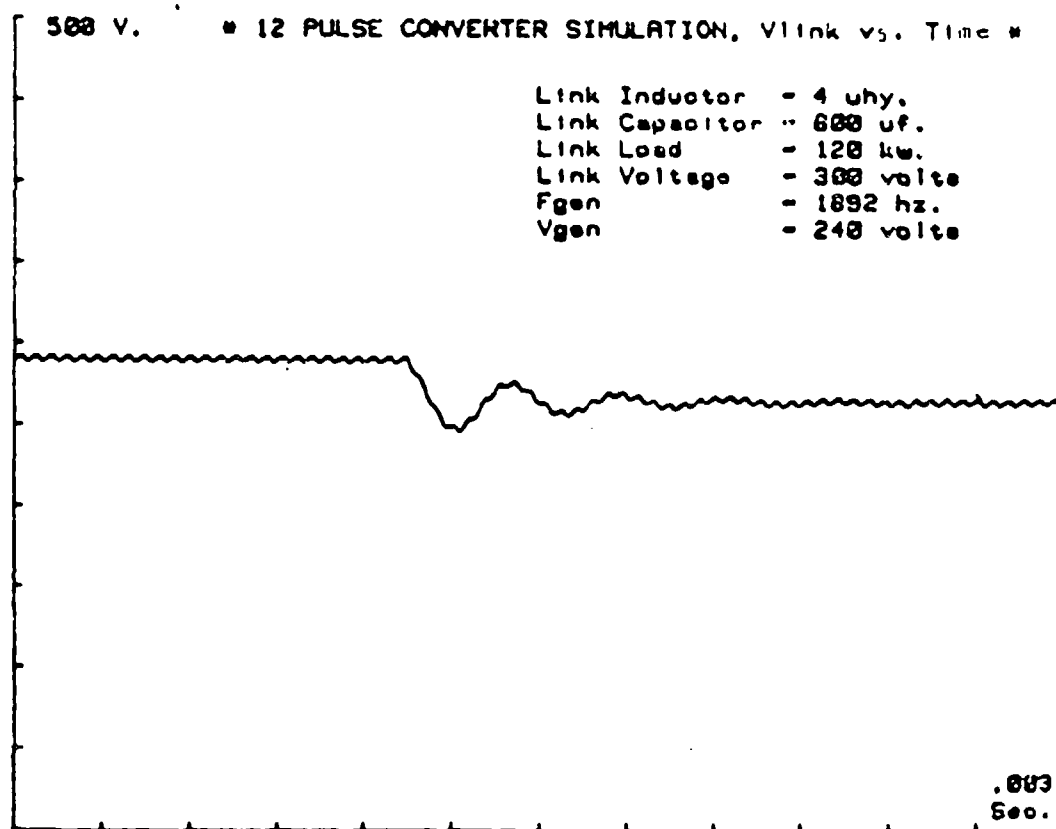
Figure 1.2.3.2-2

Twelve Pulse Converter Response to 10% Phase-Back

1-70

500 V.   * 12 PULSE CONVERTER SIMULATION, Vlink vs. Time *

Link Inductor   = 4 uhy.
Link Capacitor = 600 uf.
Link Load   = 120 kw.
Link Voltage   = 300 volts
Fgen   = 1360 hz.
Vgen   = 173 volts

.003
Sec.
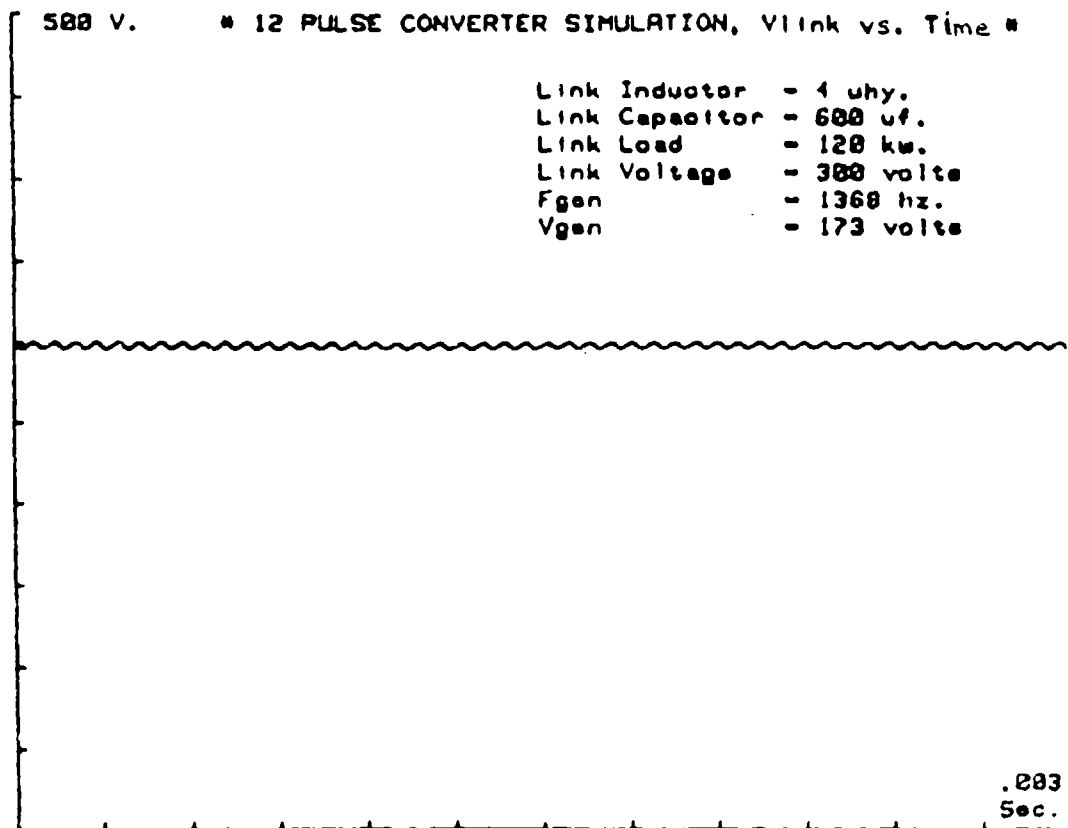
Figure 1.2.3.2-3

Twelve Pulse Ripple (1.25%) at 60% Speed

1-71

500 V.   * 12 PULSE CONVERTER SIMULATION, Vlink vs. Time *

Link Inductor   = 4 uhy.
Link Capacitor = 600 uf.
Link Load   = 120 kw.
Link Voltage   = 300 volts
Fgen   = 1200 hz.
Vgen   = 153 volts

.003
Sec.
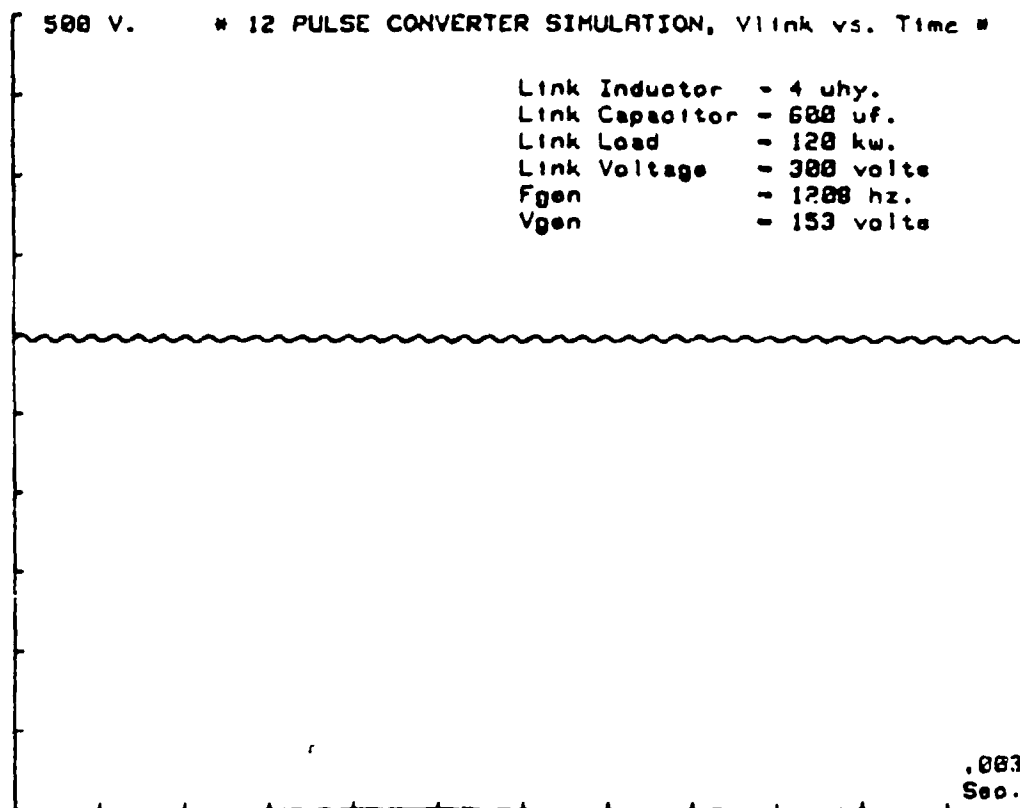
Figure 1.2.3.2-4

Twelve Pulse Ripple (1.2%) at 53% Speed

1-72

1.2.3.3   SCR Control System

Figure 1.2.3.3-1 is a block diagram of the SCR control system. The generator
output is six-phase (two three-phase sets staggered by 30 degrees). The VSCF
control circuit design uses a "phantom" approach having scaled down inputs
from the real system going to a mini-preregulator circuit. This phantom
system uses a 0 to 10 volt control voltage from the 400 Hz inverter in a
closed loop configuration to control the scaled down preregulator. The switch
commands in the phantom system are amplified and used to drive the SCRs in the
real system.

The four three-phase pulse circuits are identical. Figure 1.2.3.3-2 shows a
basic three-pulse integral control circuit. Figure 1.2.3.3-3 shows the
waveforms of this circuit.

The scaled down three-phase input signals from the generator are commutated
into the integrator using S1, S2, and S3. The input to the integrator looks
like waveform (a). The integrator output is waveform (b). When the
integrator output passes through zero volts, the comparator output changes
state. This transition steps the ring counter one count, which opens the
closed switch and closes the succeeding switch. The integrator input is then
more positive than the reference and the integrator output proceeds in a
positive direction. This operation is illustrated in Figure 1.2.3.3-4.

A problem with this circuit is that the waveform shown in Figure 1.2.3.3-5 may
also result. The distortion in the waveform represents an imbalance in firing
angles for the SCRs in different portions of the input frequency cycle. This
instability in firing angle can be corrected by modifying the circuitry as
shown in Figure 1.2.3.3-6. When the integrator output passes through the
voltage generated by the ramp generator, the comparator output changes state.
This transition resets the ramp generator to zero as well as stepping the ring
counter one count.
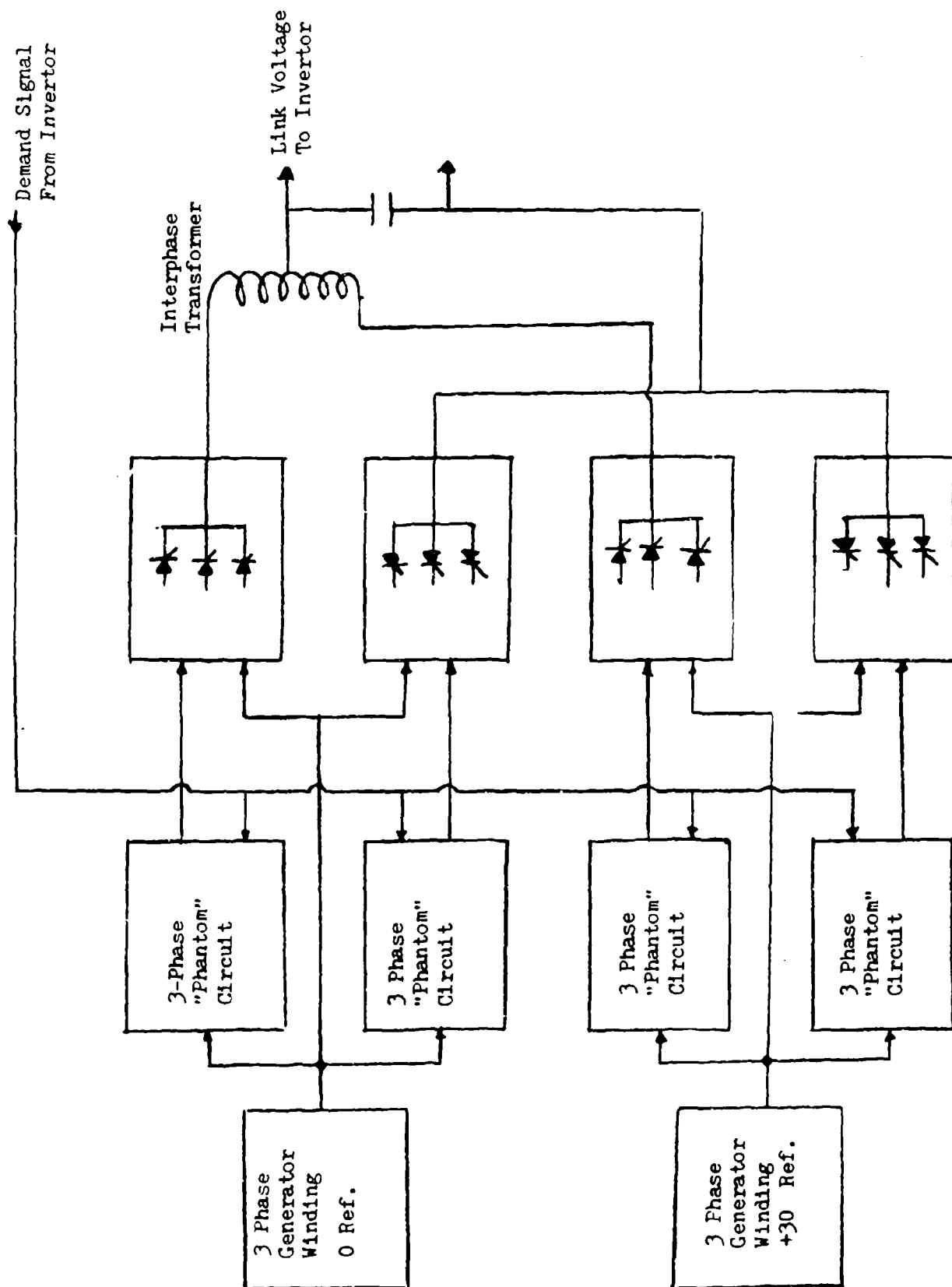
Figure 1.2.3.3-1

SCR Control System Block Diagram

RING COUNTER

ϕ_1 —— S1

ϕ_2 —— S2

ϕ_3 —— S3

INTEGRATOR

COMPARATOR

TO
SCR
DRIVE
CIRCUIT
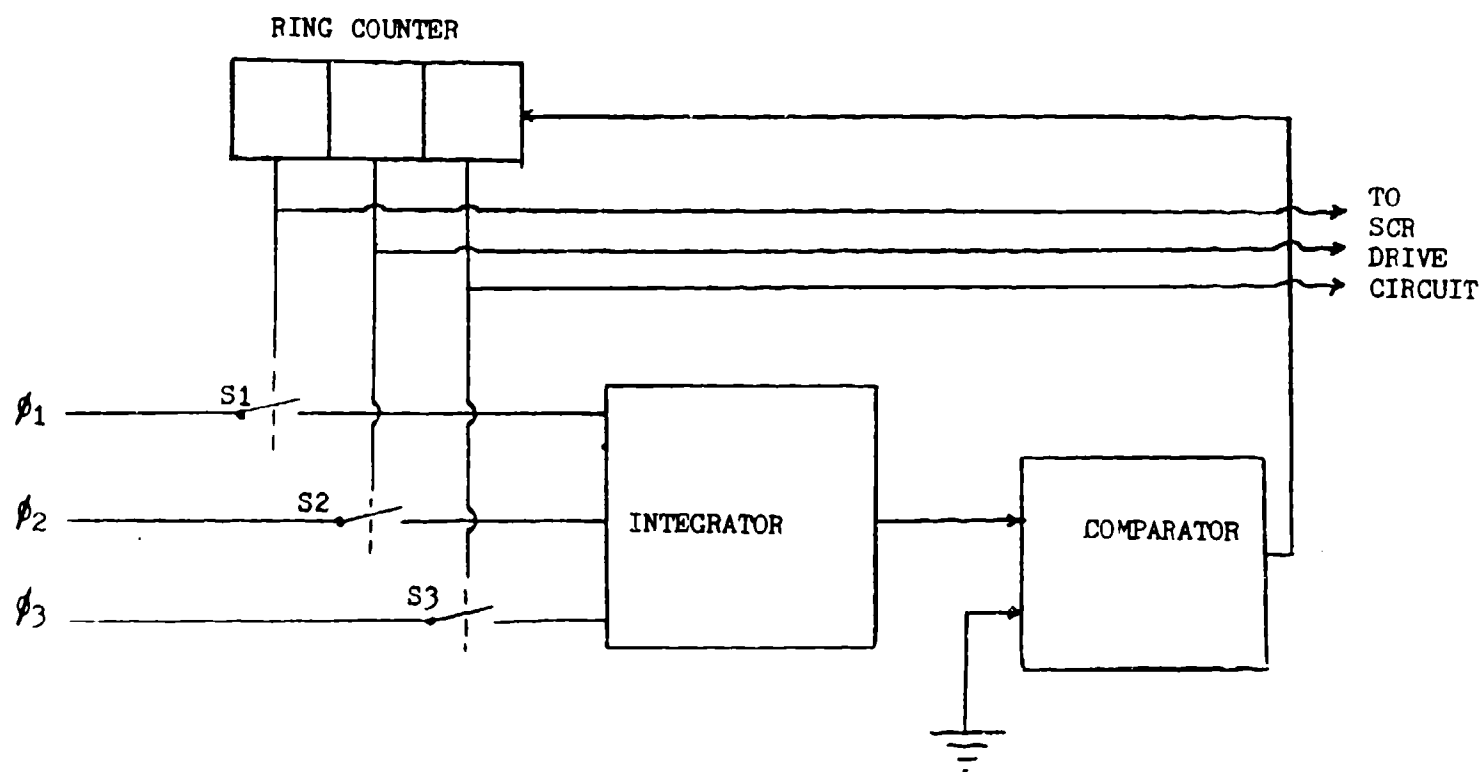
Figure 1.2.3.3-2
Basic Three-Pulse Integral Control Circuit

1-75
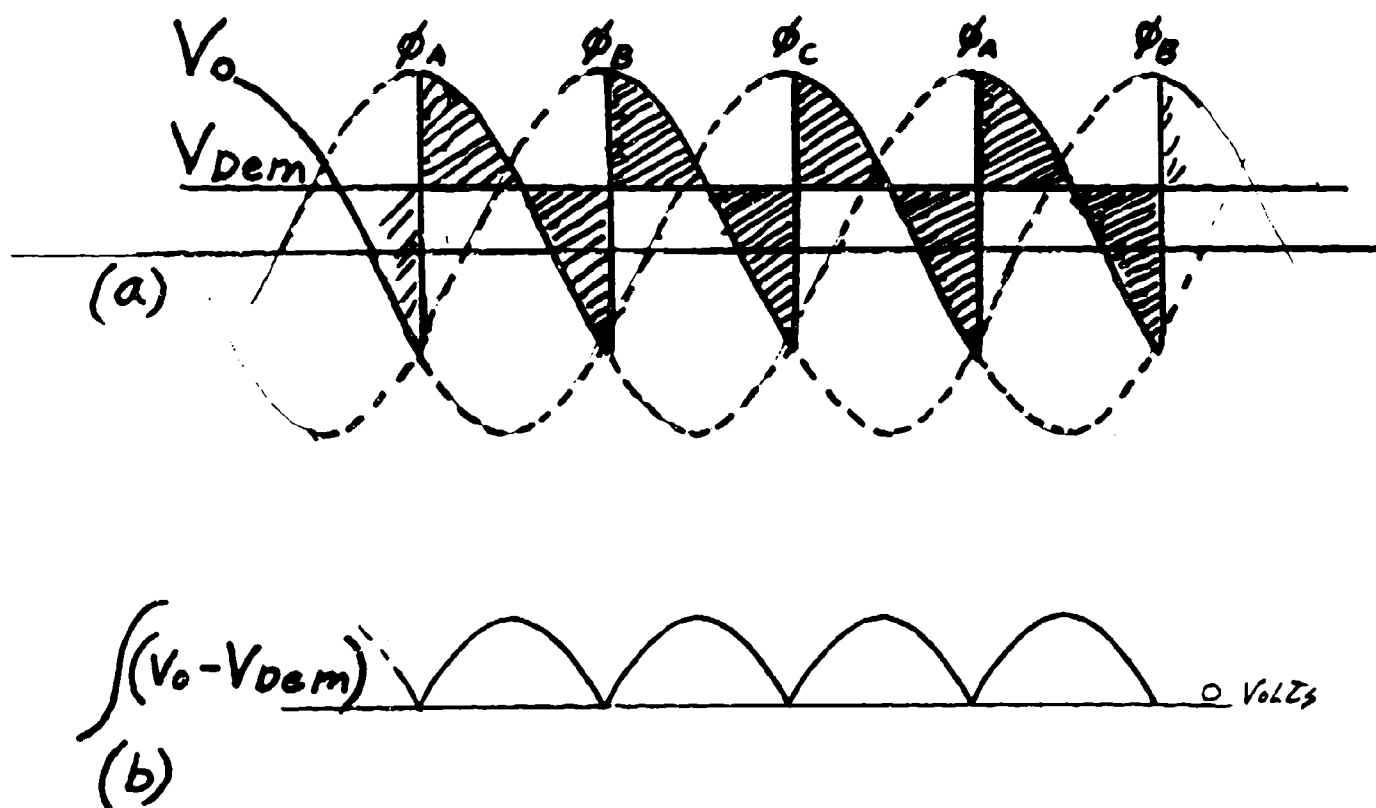
Figure 1.2.3.3-3

Waveforms of Basic Three-Pulse Integral Control Circuit
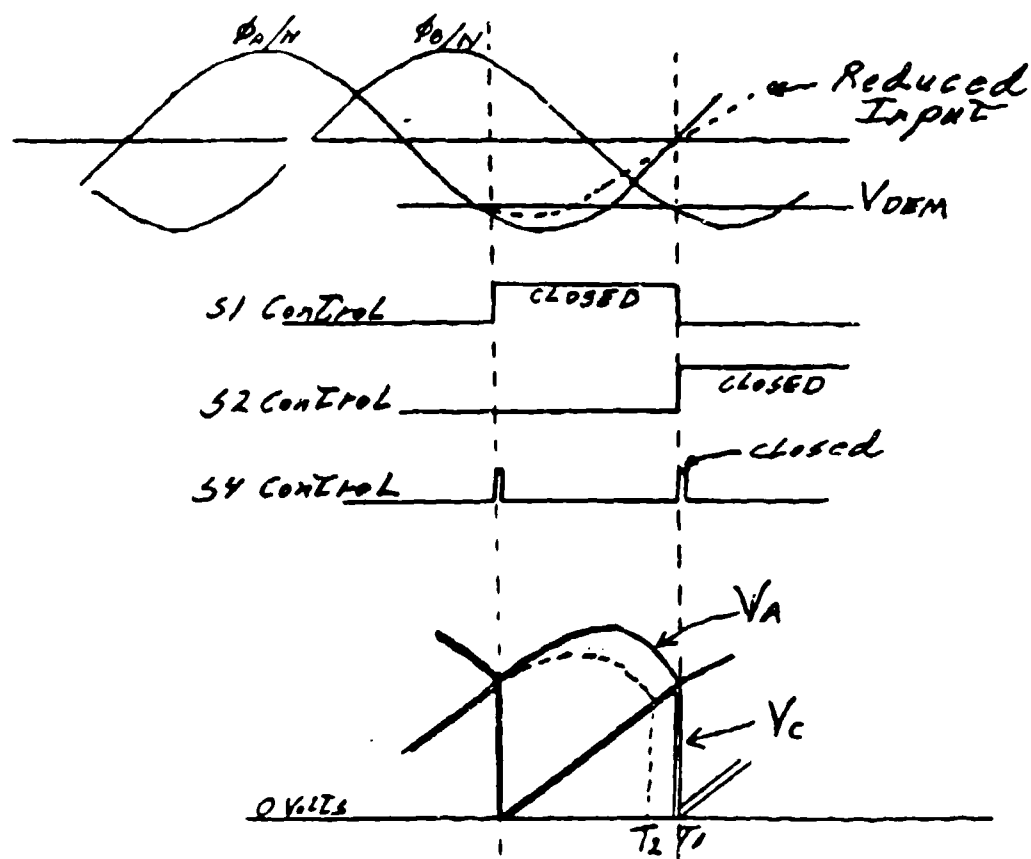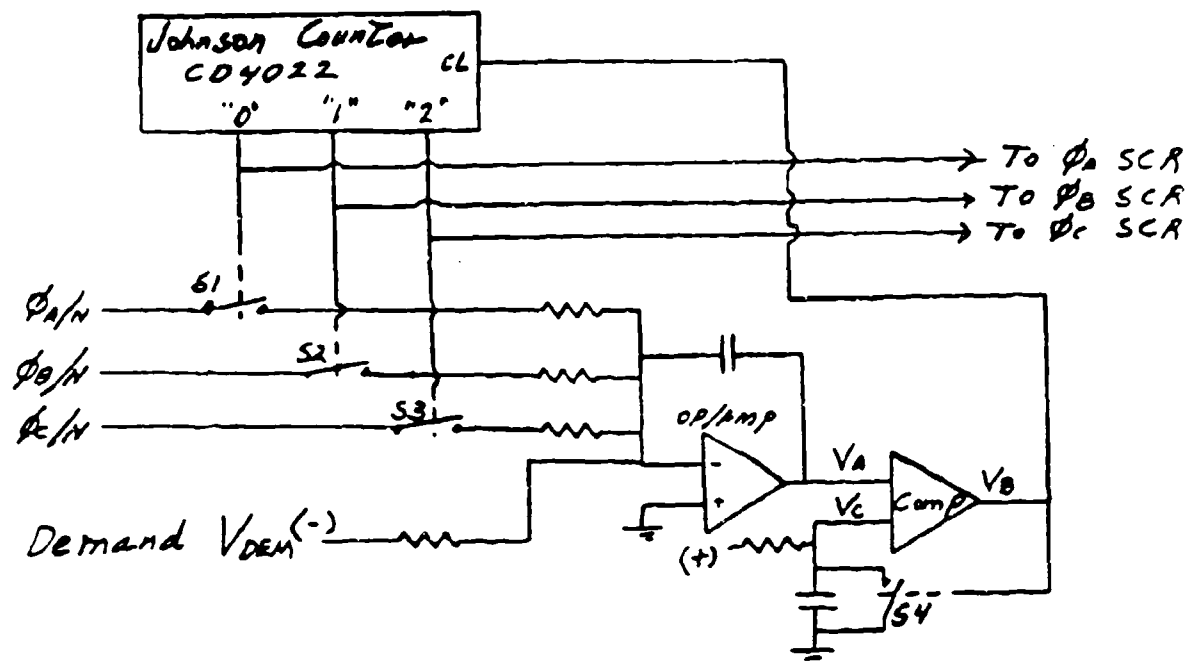
Figure 1.2.3.3-4

Simplified Circuit Showing Sensing
and Control of Crossover Switching

1-77
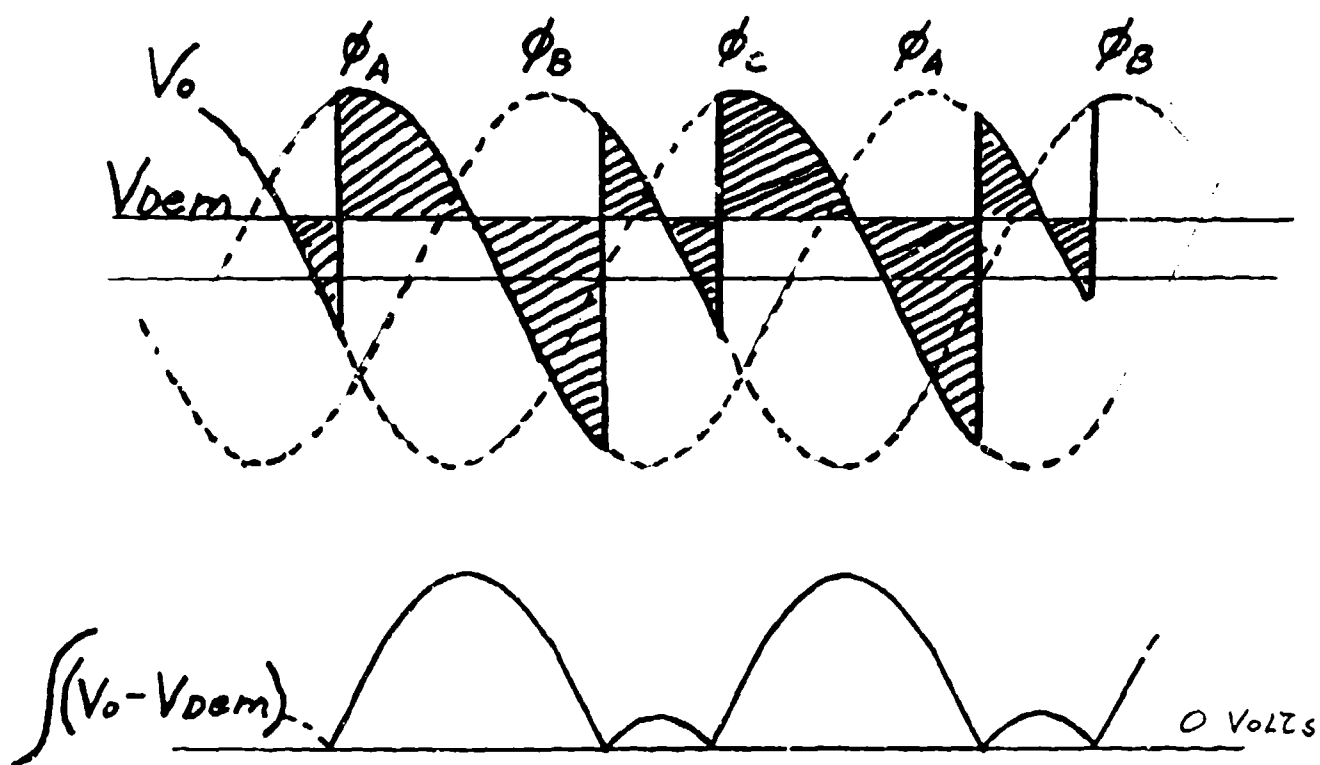
Figure 1.2.3.3-5
Distorted Waveform from Basic
Three-Pulse Integral Control Circuit

1-78

RING COUNTER

φ₁ S1

φ₂ S2

φ₃ S3

INTEGRATOR

COMPARATOR

RAMP
GENERATOR   RESET SIG.

TO
SCR
DRIVE
CIRCUIT
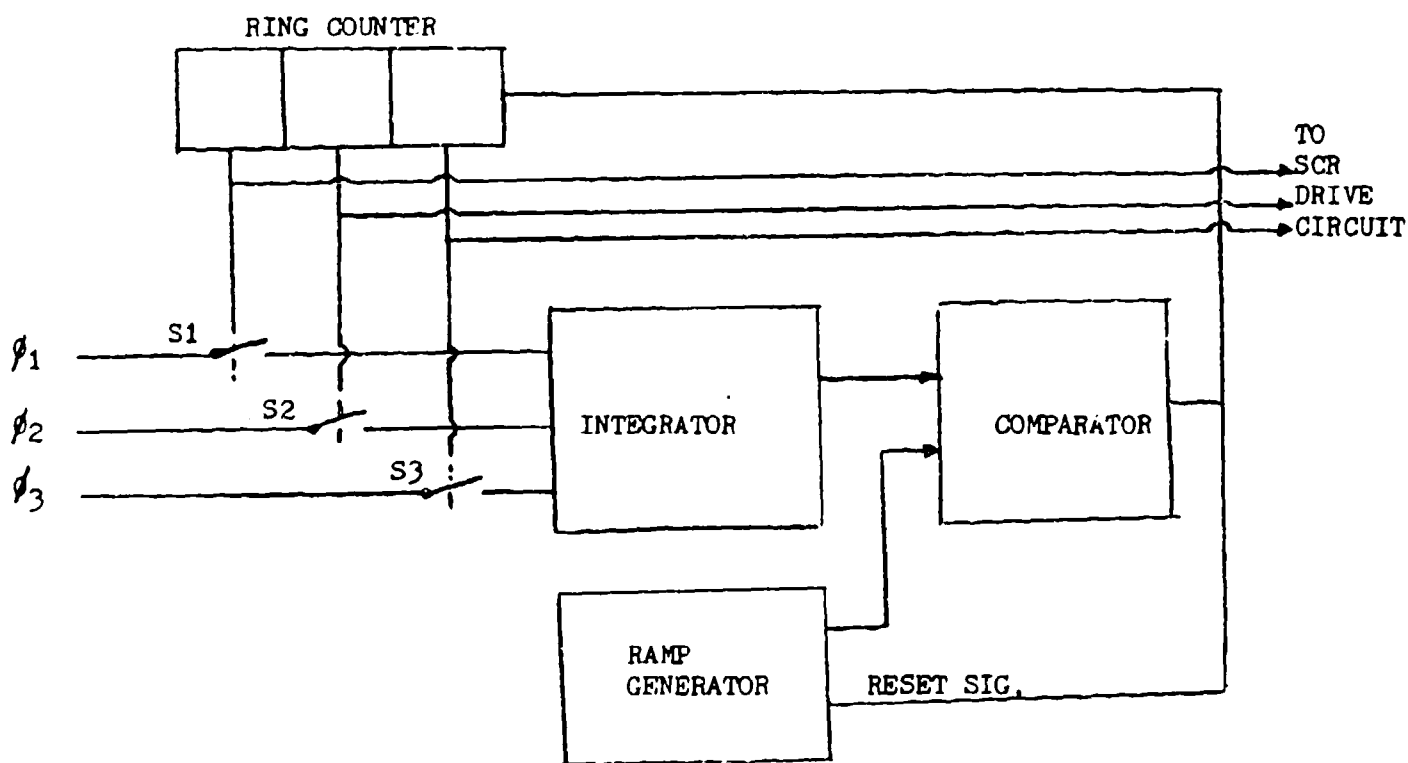
Figure 1.2.3.3-6
Modified Three-Pulse Integral Control Circuit

1-79

1.2.3.3   SCR Control System   (Continued)

Figure 1.2.3.3-7 shows how this modification to the basic circuit improves
timing. The "normal integrator output" is the integrator output under normal
steady-state conditions. The SCR firing point is at T3. The integrator
output caused by noise or a sudden change in input voltage is shown. Without
the modification, the SCR firing would be at T1. With the addition of the
ramp circuit, the SCR firing is at T2. The SCR firing time T2 is closer to
the ideal firing time T3. This circuit helps to hold adjacent SCR firing
angles constant and prevents abnormal input signals, caused by noise and
switching transients, from greatly changing the firing angles.

1.2.3.4   Safety Circuits

Figure 1.2.3.4-1 is a block diagram of the preregulator safety circuits. If a
higher DC voltage is demanded than can be provided with a particular AC
three-phase input, the SCR timing circuit advances the firing angles of the
SCRs beyond the point that creates maximum DC output. This results in
unstable system operation.

A "maximum permissible demand" signal is created by measuring the amplitude of
the AC input and calculating the equivalent DC output this AC input can
sustain. This maximum permissible demand is substituted for the actual demand
when the actual demand exceeds it.

If the demand becomes very low, the SCR firing circuit becomes very sensitive
to noise and becomes unstable. A "minimum demand signal" (demanding about 50
volts) is generated and is substituted for the actual demand when the actual
demand is lower than the minimum.

The preregulator system contains circuits to detect potentially destructive
(to the 400 Hz inverter) output voltage magnitude and output voltage rates of
change. When these undesirable conditions are detected the demand to the
control system automatically switches to the minimum demand signal, which
reduces the output to a safe level.
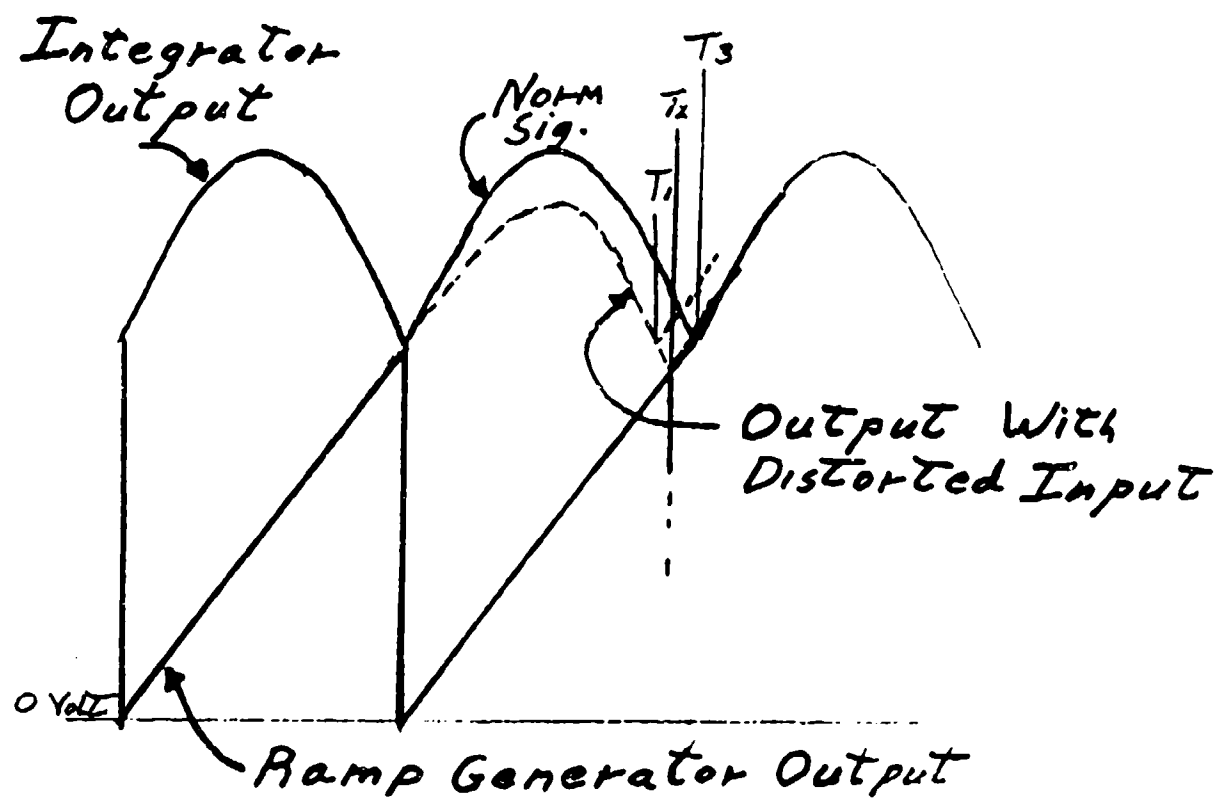
Figure 1.2.3.3-7
Impact of Improved Timing

1-81
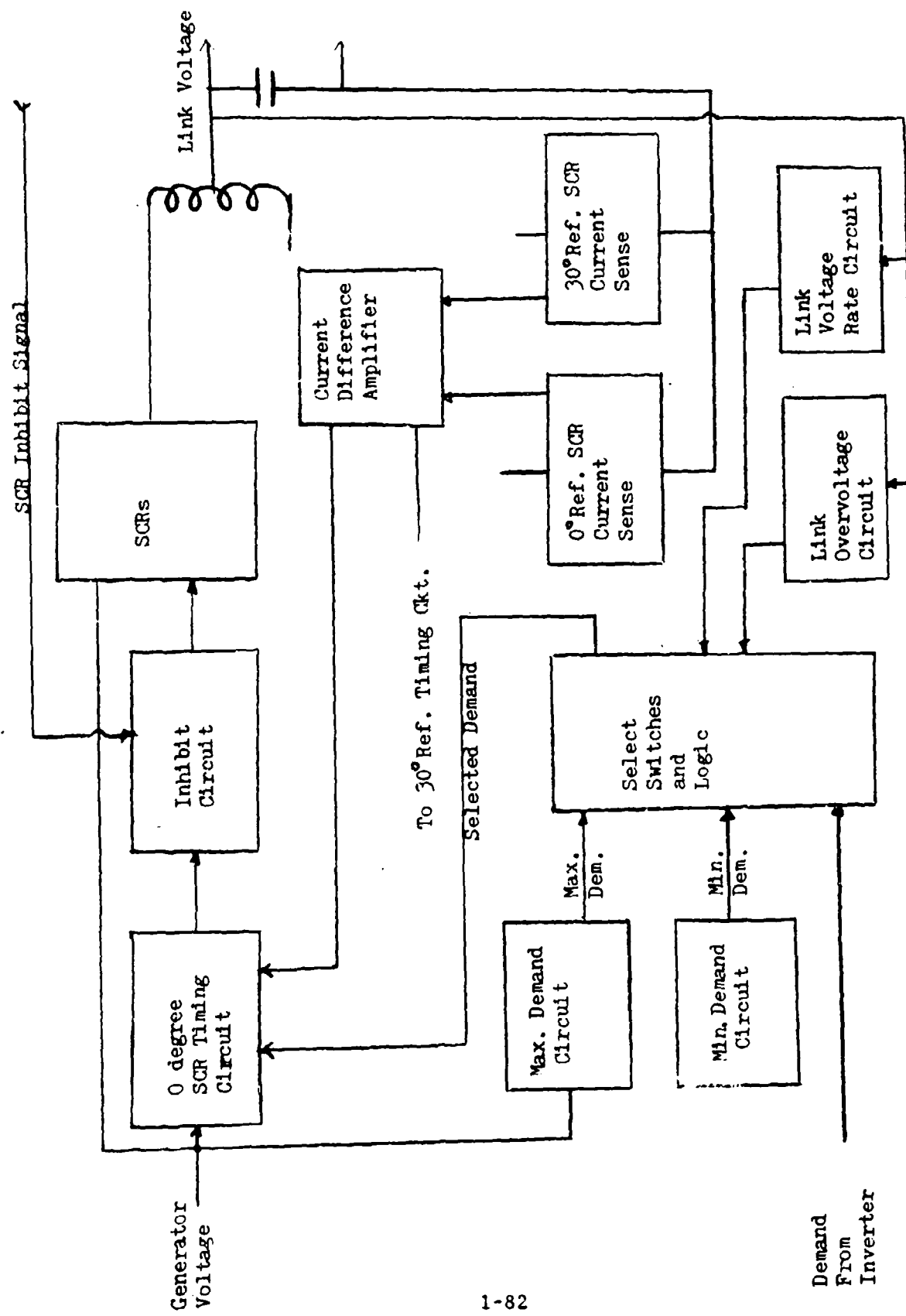
Figure 1.2.3.4-1

Preregulator Safety Circuits Block Diagram

1.2.3.4   Safety Circuits   (Continued)

One of the output voltage safety circuits is the output overvoltage trip
circuit. The output voltage is sensed, and when it exceeds 336 volts, the
controller demand is switched to the minimum demand signal.

A second safety circuit is the output voltage rate trip circuit. The scaled
link voltage is connected to a rate sense circuit. If the output voltage rate
exceeds 1,000 volts per millisecond, this circuit switches the controller
demand to the minimum demand signal.

All SCRs can be prevented from being fired by an inhibit signal sent from the
400-Hz inverter. This digital signal is optically isolated from the
preregulator power system. A five volt high on this inhibit line permits
normal operation of the SCR and a zero volt signal prevents SCR firings.

The DC current from each three-phase section of the preregulator passes
through the interphase transformer. These DC currents must be maintained near
the same level to prevent the interphase transformer from saturating.
Accordingly, the DC current from each three-phase section is passed through a
50-millivolt shunt in the positive side of each circuit. The difference
voltage from the shunts is applied to a current difference amplifier. This
amplifier has a one volt output for a 40-ampere difference in current between
the two three-phase systems. This error voltage is scaled and added to the
demand signal, for one three-phase system and subtracted from the demand of
the other three-phase system to equalize the system currents. The system is
scaled such that a 40-ampere difference in currents results in a 16-volt
differential in the DC demanded out of each system.

1.2.3.5   Inverter/Inverter Control Unit

The three-phase inverter and the inverter controls are based on the technology
developed on other DC-link VSCF type systems. The concepts that have been
developed are applicable to the inverter system and are presented in section
2, Theory of Operation.

1.2.3.6 Mechanical Design and Cooling

The package for the 400-Hz power conditioner will be similar in configuration and utilize many packaging techniques as required for equipment qualified for use on aircraft. Because this design is for a laboratory breadboard test unit only, size and weight considerations have been compromised with maintainability, manufacturability and cost considerations. Repackaging to meet space or environmental constraints for a specific aircraft application would not cause deviation in performance or require extensive redevelopment to make it work. Table 2.1-1 gives estimated weights of the breadboard unit assemblies. Weight reductions could be realized in many areas. The lab unit is designed using many standard component configurations, and could be repackaged for a particular aircraft application with an increase in packaging efficiency.

The power conditioner circuit has been divided into two groups; one that will be cooled by oil, and the other that will be cooled primarily by surrounding air. All power semiconductors with their drive circuits, plus all transformer/inductors which carry full load current, will be packaged with a sealed housing and cooled by means of spray oil conforming to MIL-L-7808. Power interfaces to the housing will be via feed-through terminals, and logic interfaces will be via hermetic sealed connectors. Filter components such as capacitors will be packaged outside of the sealed housing, and will be cooled by natural convection to the surrounding environment and by conduction to the aluminum mounting plate. Logic circuits for control, protection, paralleling, current limiting, waveform and frequency control, and regulation will be packaged in separate convection cooled modules. These will include a generator control unit, an inverter control unit, and a link suppressor module.

The rationale for the above divisions is as follows. All components with high dissipation will be cooled by the very effective method of spray oil.

1.2.3.6   Mechanical Design and Cooling   (Continued)

Components with low dissipation need not be in the spray oil, thus there are
significant weight savings by packaging them in a more conventional manner.
There are logical break points in the circuit schematic that allow the
following described separation of components without introducing great numbers
of power feed-throughs, or effecting circuit performance. Logic circuit
boards and many components used in logic circuits are not compatible with the
cooling oil because they are not hermetically sealed or cannot withstand high
temperature transients expected in aircraft, thus they must be isolated from
it. Maintainability is enhanced by packaging logic circuit cards in readily
accessible packages as may be accomplished with natural convection cooling.

1.2.4   High Voltage Power Supply

The high voltage power supply (HVPS) design meets the system requirements
listed in Table 1.2.4-1. Figure 1.2.4-1 is a block diagram of the 400-Hz
sections and HVPS. Each three-phase output of the generator is connected to a
delta-wye step-up transformer. The output of the transformer is rectified by
a three-phase full wave bridge. The two DC outputs are connected in
parallel. An LC filter is used to reduce the ripple to the specified level.
The distortion of the AC waveform by the phase back power supply for the
400-Hz inverter is the major factor influencing the selection of the power
supply circuit.

The following paragraphs describe the rationale for the selection of the power
supply circuit. The electrical and mechanical factors considered in selecting
the particular design for the high voltage power supply are:

    1. Electrical
        a) Generator frequency
        b) Number of phases
        c) DC voltage out
        d) Efficiency
        e) Power

Table 1.2.4-1
High Voltage Power Supply Specifications

```
| Input                                                           |
|   Voltage                          240-246 V L-N                |
|   Frequency                        1886-2500 Hz                 |
|   Phases                           6    (Note 1)                |
|   Line Distortion                  0.035 Max                    |
|                                                                 |
| Output                                                          |
|   Volts                            13,200 VDC +470, -1200       |
|   Amperes                          20    (Note 2)               |
|   Ripple                           260 V p-p Max                |
|                                                                 |
| Protection                                                      |
|   Channel Over Current                                          |
|   Interaction Each Channel Independent 1.2 PU for 5 sec.        |
|                                                                 |
| Weight                             150 lbs (goal)               |
|                                                                 |
| Cooling                            Air or MIL-L-7808 oil        |
|                                                                 |
```

Note 1.   The 6 phases consist of two normal three phase outputs
          displaced from each other by 30°.

Note 2.   The specified normal load on 4 power supplies is 60
          amperes. Since 3 power supplies must supply the full load
          each power supply must be designed for 20A.

1-86
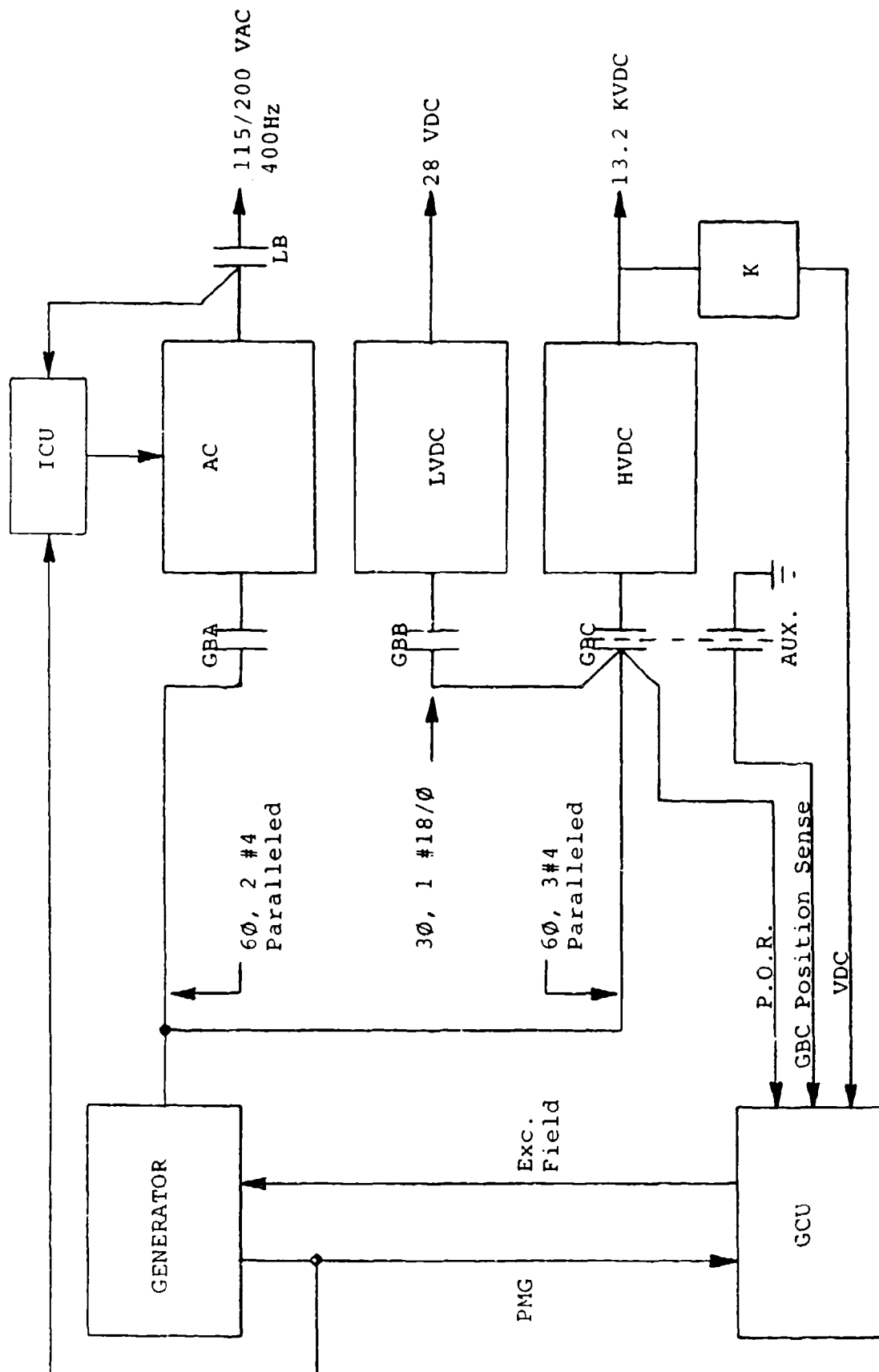
Figure 1.2.4-1

System Block Diagram Showing 400-Hz and HVPS Connections

1.2.4   High Voltage Power Supply   (Continued)

      f) Regulation

      g) Reliability

      h) Generator characteristics

   2. Mechanical

     a) Volume

     b) Weight

     c) Safety

1.2.4.1   General Considerations

Since the line voltage is less than required output voltage, the HVPS must
contain a step-up transformer. Usually the higher the frequency of operation,
the smaller the transformer. Minimum size may be limited by the high voltage
insulation requirements and power losses in the transformer. Previous studies
have shown that the minimum size for transformers at the voltage and power
levels required occurs between 2 KHz and 5 KHz. As the power levels increase,
the minimum size occurs nearer to 2 KHz. Since the line frequency is between
1800 and 2500 Hz for the HVPS, a transformer/rectifier is considered the best
approach. The increased size and weight for an inverter is not warranted by
the small decrease in transformer size. The additional circuitry for an
inverter reduces the reliability.

The input power to the power supply is from a dual three-phase generator. The
outputs from one section are phase shifted from the other section by 30°. If
a conventional three-phase bridge rectifier is connected to each of the three
phases, and the outputs connected to a common load, the DC output has a ripple
of 12 times the input frequency. The peak-to-peak ripple is 3.4% of the peak
AC. This is approximately 450v peak-to-peak.

1.2.4.1   General Consideration   (Continued)

It is possible to connect the secondary windings of a transformer to produce
phase shift. If two secondaries are used on one transformer to produce a ±15°
phase shift, the ripple is also 12 times the fundamental frequency. For
similar power supplies connected to the two generator outputs, the ripple
output for the two power supplies are in phase. This type of connection was
considered.

A transformer that shifts the output phase ±7.5° from the input has a higher
ripple than one with ±15° phase shift. Two such transformers connected to the
generator, produce a rectified output that has ripple at 24 times the line
frequency. The ripple amplitude is .856% peak-to-peak or 113 volts. Since
this is less than the 250v peak-to-peak required, no DC filter is used.

1.2.4.2   Computer Studies

The power supply with the 24 pulse ripple was more thoroughly
investigated. A computer analysis of the circuit was done using Simulation
Program with Integrated Circuit Emphasis (SPICE). This is a general circuit
analysis program. The program was run on a
DEC-VAX 11/780 computer.

Computer analyses of three-phase rectifier circuits had been done before.
In doing these previous analyses, general models of a three-phase
generator and a three-phase rectifier had been developed. To analyze the
complete system, two of these generator/rectifier models were needed. One
generator was phase shifted by 30° with respect to the other. One half of the
system was modeled and analyzed. The ripple for the two halves was manually
shifted to give the final result.

The three-phase transformer models were made up from the single-phase models.
Models for more complex circuits that were to be used repeatedly were written
as subcircuits. The generators, transformers, and rectifier bridges were
written as subcircuits.

1.2.4.2   Computer Studies   (Continued)

Figure 1.2.4-2 is the computer model of the generator. V1 is an independent sine wave source that is specified at the lowest frequency at which the HVPS is to operate. The amplitude of this source is equal to the phase-to-neutral voltage. E1 is a voltage-controlled voltage source. The output is the same amplitude as V1 but is phase shifted by 180°. C2, R2 and C1, R1 shift the output of E1 ±30°. There are, therefore, three voltages produced that are 120° apart. These are used to drive sources EA, EB, and EC. This is an ideal three-phase generator. R9, R10, and R11 are equal to the direct axis resistance of the generator. L1, L2, and L3 are equal to the subtransient reactance of the generator. R15, R16, and R17 represent the magnetic losses in the generator. All of the other resistors in the circuit are required to make the computer program complete. The values used have no influence on circuit performance. To change the voltage it is only necessary to change the voltage of V1. To change the frequency, the frequency of V1 is changed and the values of C1 and C2 are changed to maintain the ±30° phase shift at the new frequency.

The basic transformer model is shown in Figure 1.2.4-3. L1 is equal to the primary open circuit inductance of the actual transformer. L2 is equal to the secondary open circuit inductance. This is equal to the square of the theoretical voltage ratio times the primary inductance. To represent the leakage inductance, the coefficient of coupling between L1 and L2 can be set to less than one. In the model shown here, L1 and L2 are perfectly coupled. L3 is equal to the leakage inductance. R1 and R4 represent the primary and secondary copper losses. R2 and R3 are selected to give total losses equal to the core loss at the applied voltages. C1 is the secondary distributed capacitance. The remainder of the resistances are required by the computer to do the analysis circuit.

Two models were set up, one for the basic transformer and one for the phase shift section. These are connected as shown in Figure 1.2.4-4 to simulate the ±7.5 degree phase shift of the double zig-zag transformer for the computer analysis.
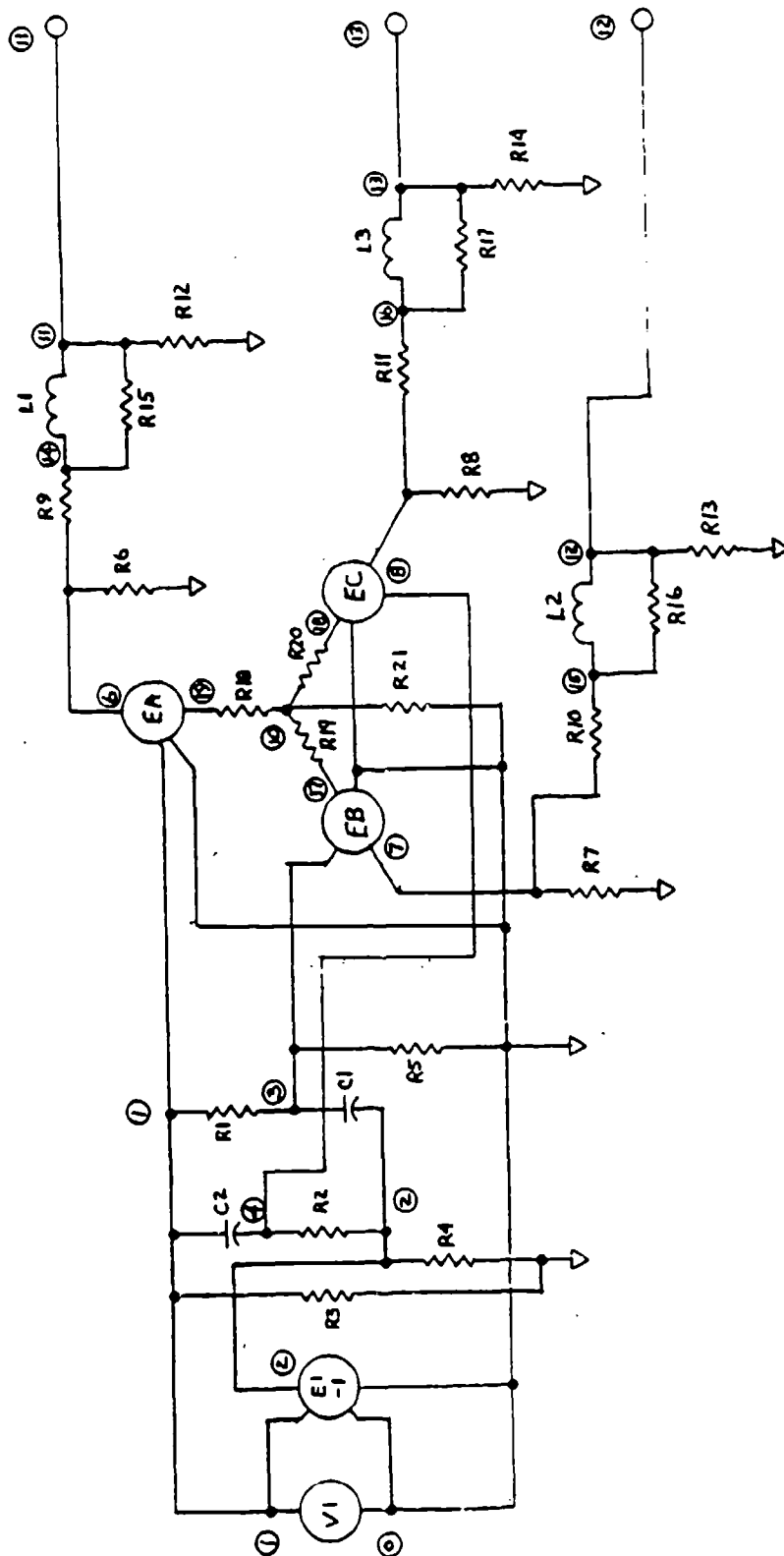
Figure 1.2.4-2

Computer Model for a Three-Phase Generator
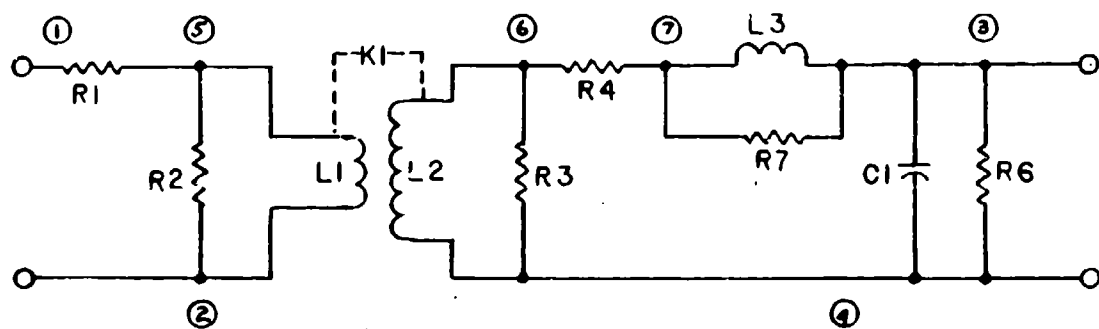
Figure 1.2.4-3

Computer Model for a Single-Phase Transformer
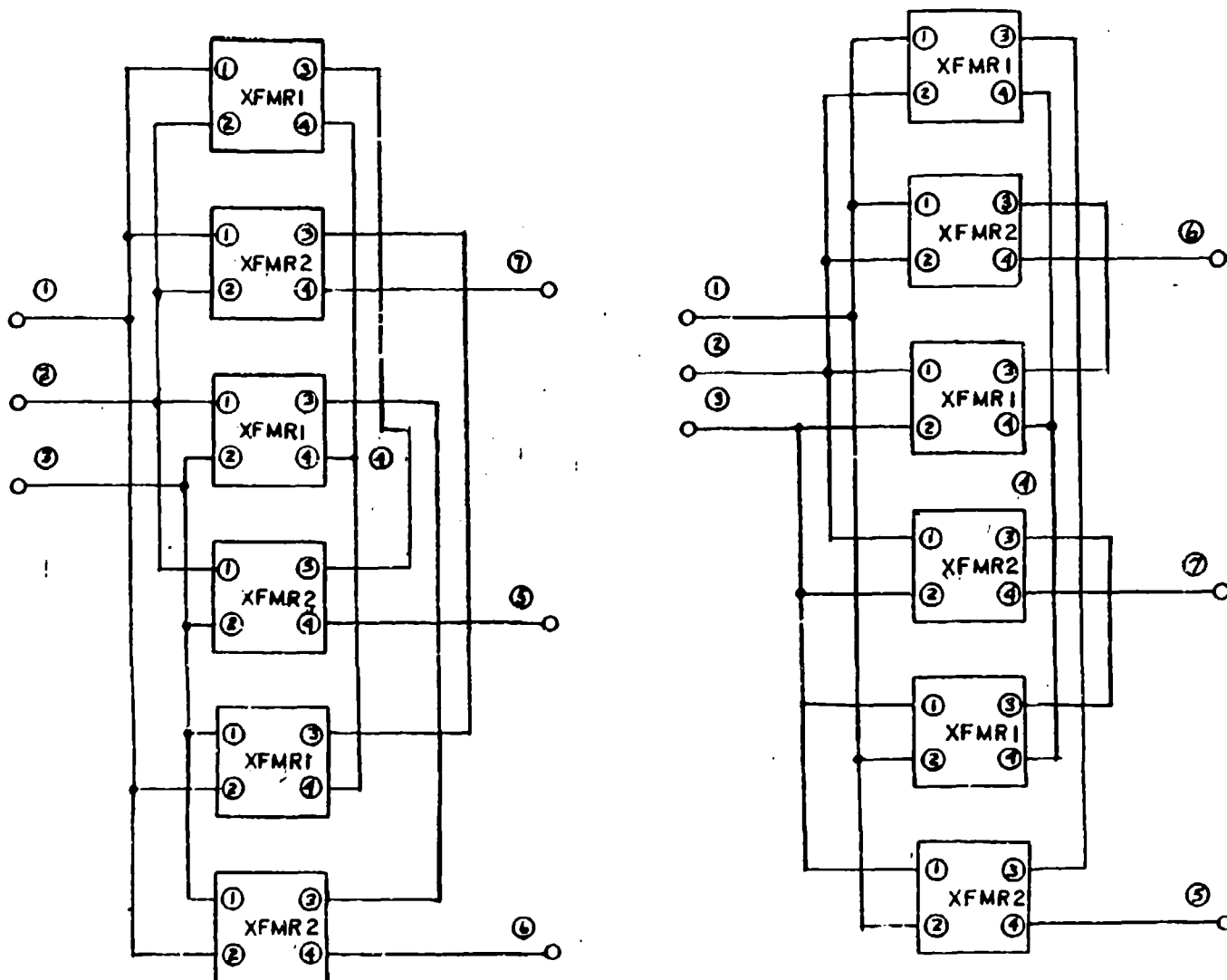
Figure 1.2.4-4

Computer Model for the Zig-Zag Transformer Connection

1.2.4.2   Computer Studies   (Continued)

Figure 1.2.4-5 is the model for the three-phase rectifier. The series RC
networks are to reduce high frequency interference due to commutation. The
resistors shunting the diodes are for simulation of reverse leakage of the
diodes.

Three different computer analyses were carried out. First, a program was
written to analyze the operation of a double zig-zag rectifier with ±7.5°
phase shift. The second analysis was to determine the operation of the DC
supply for the 400-Hz inverter. Since a constant 300v dc was desired for the
400-Hz inverter, a full-control phase-back power supply was used. Due to the
high reactance of the generators, the phase-back greatly distorted the voltage
waveform at the generator. Since this voltage also is the input of the HVPS
it was necessary to analyze both power supplies operating together.

The third analysis was a composite of the phase back and high-voltage power
supplies. The composite analysis was done with no line filtering, 1 μf
capacitors from line to line at each power supply and the generator, and with
a harmonic filter in each power supply feeder.

The first computer calculations were done on the double zig-zag circuit with
±7.5° phase shift. The subcircuits used were the generator, 12 transformers
(6 each of two different types) connected as in Figure 1.2.4-4 and two
three-phase rectifier bridges.

The line current for the 12 pulse circuit (±7.5° phase shift) is shown in
Figure 1.2.4-6. The load on each section of the generator was the load shown
in Figure 1.2.4-6. The generator voltage distortion was as shown in Figure
1.2.4-7. The ripple was as shown in Figure 1.2.4-8. The total ripple would
be equal to the sum of two ripple waveforms equal to Figure 1.2.4-8 displaced
15° in phase. The composite ripple was about 135v p-p.
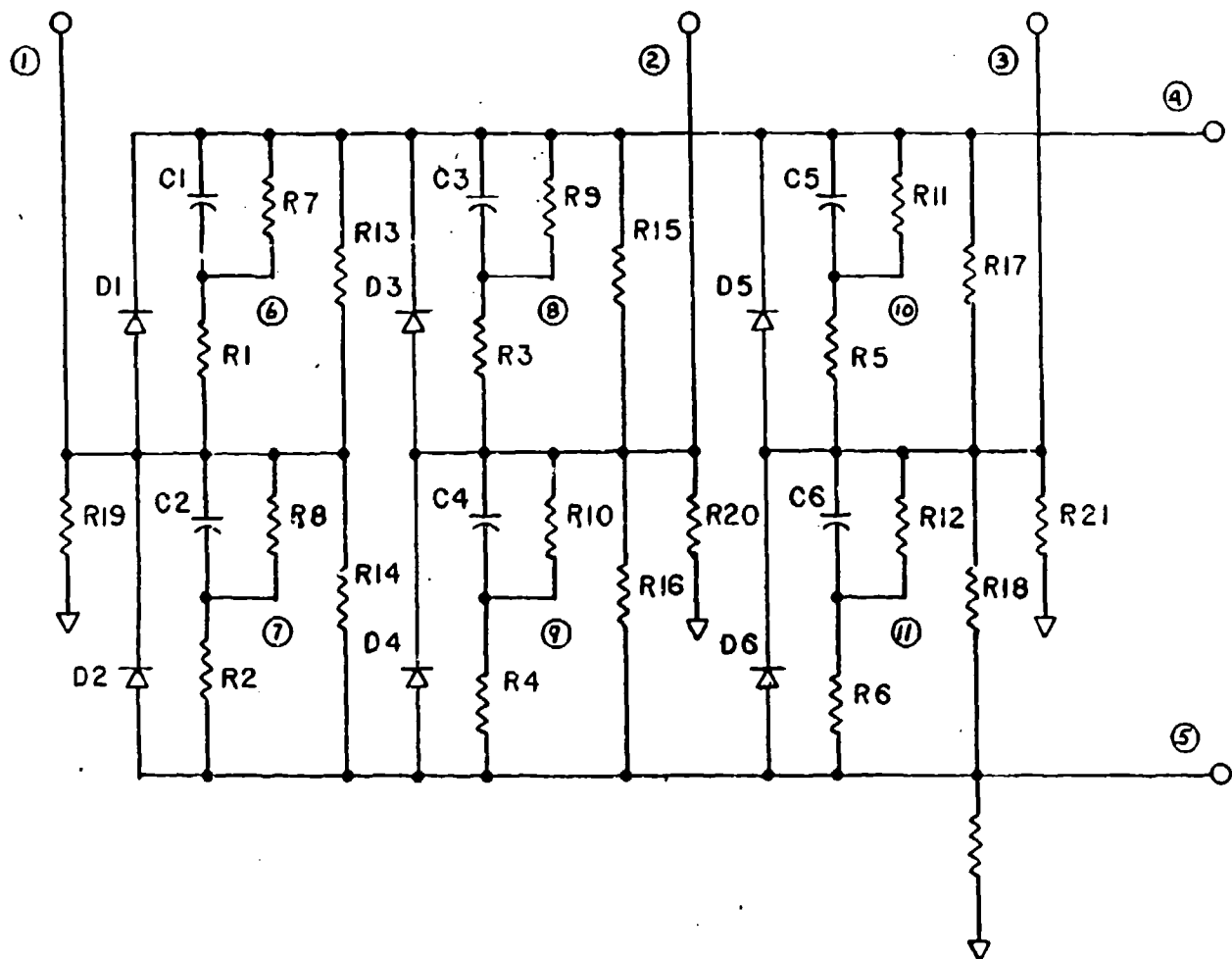
Figure 1.2.4-5

Computer Model for a Three-Phase Rectifier
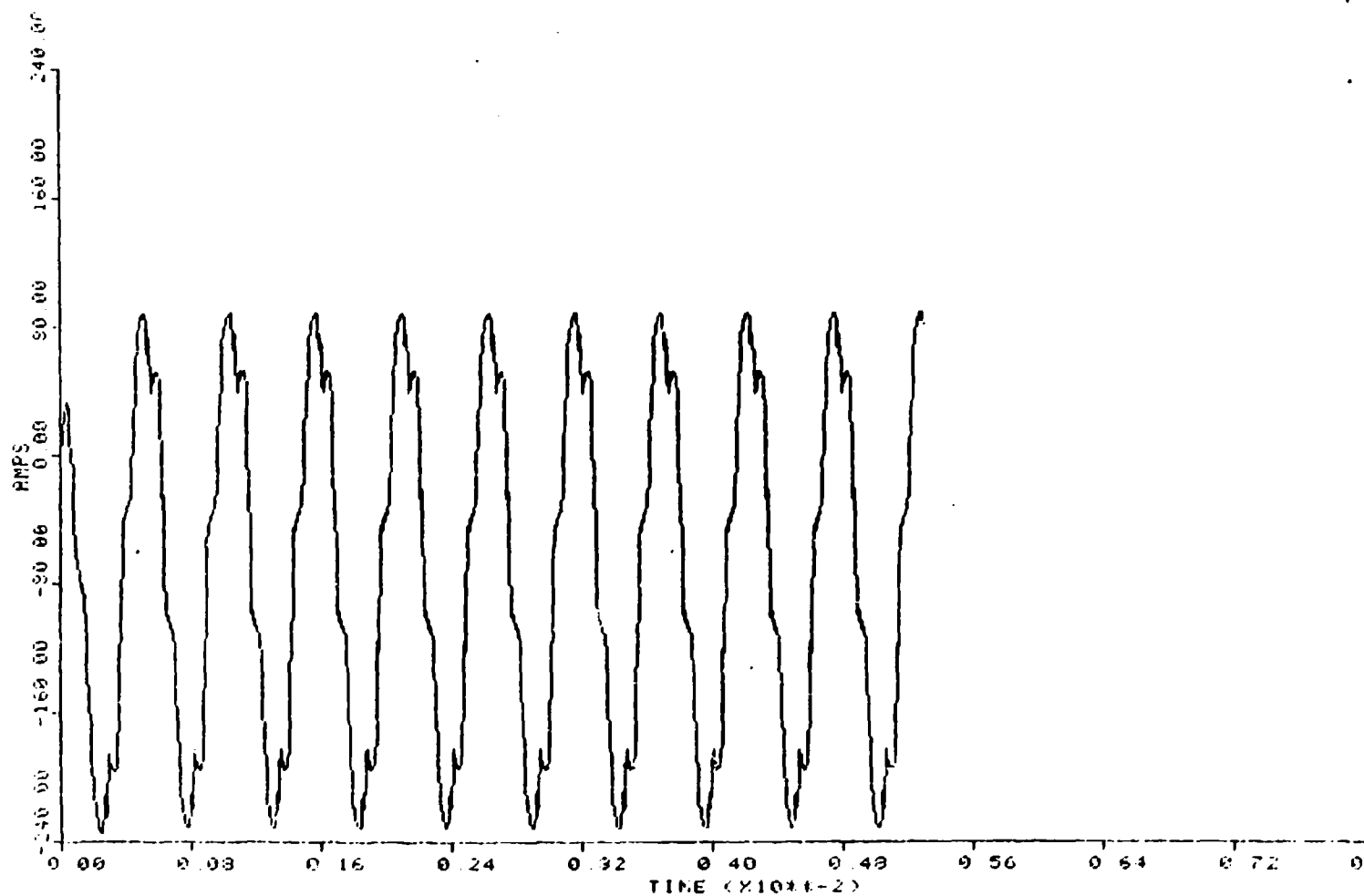
Figure 1.2.4-6

Calculated Line Current for a 12-Pulse Rectifier

Circuit with +/- 7.5-Degree Phase Shift
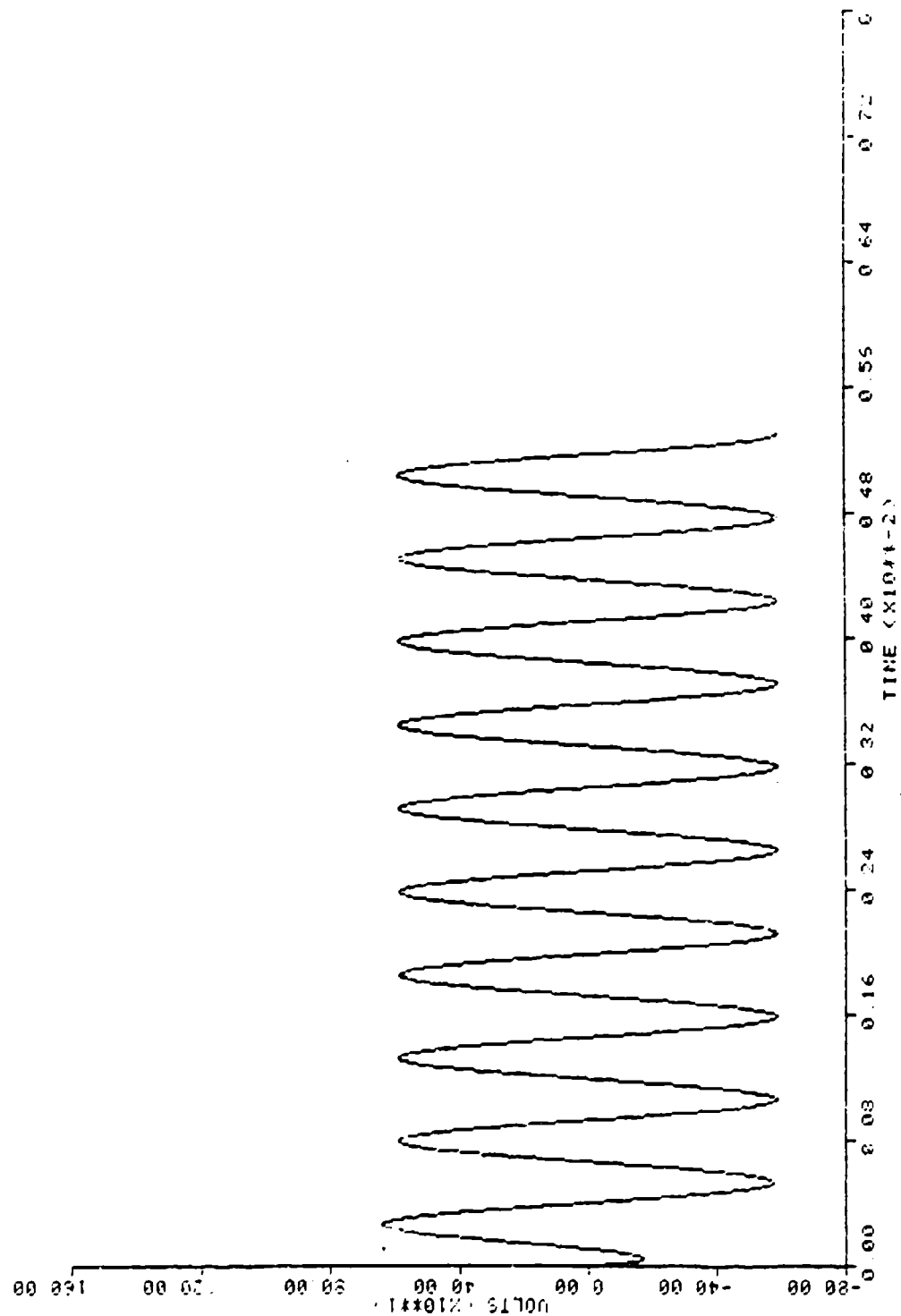
Figure 1.2.4-7

Calculated Generator Voltage With a 12-Pulse

Rectifier Circuit with a +/- 7.5-Degree Phase Shift
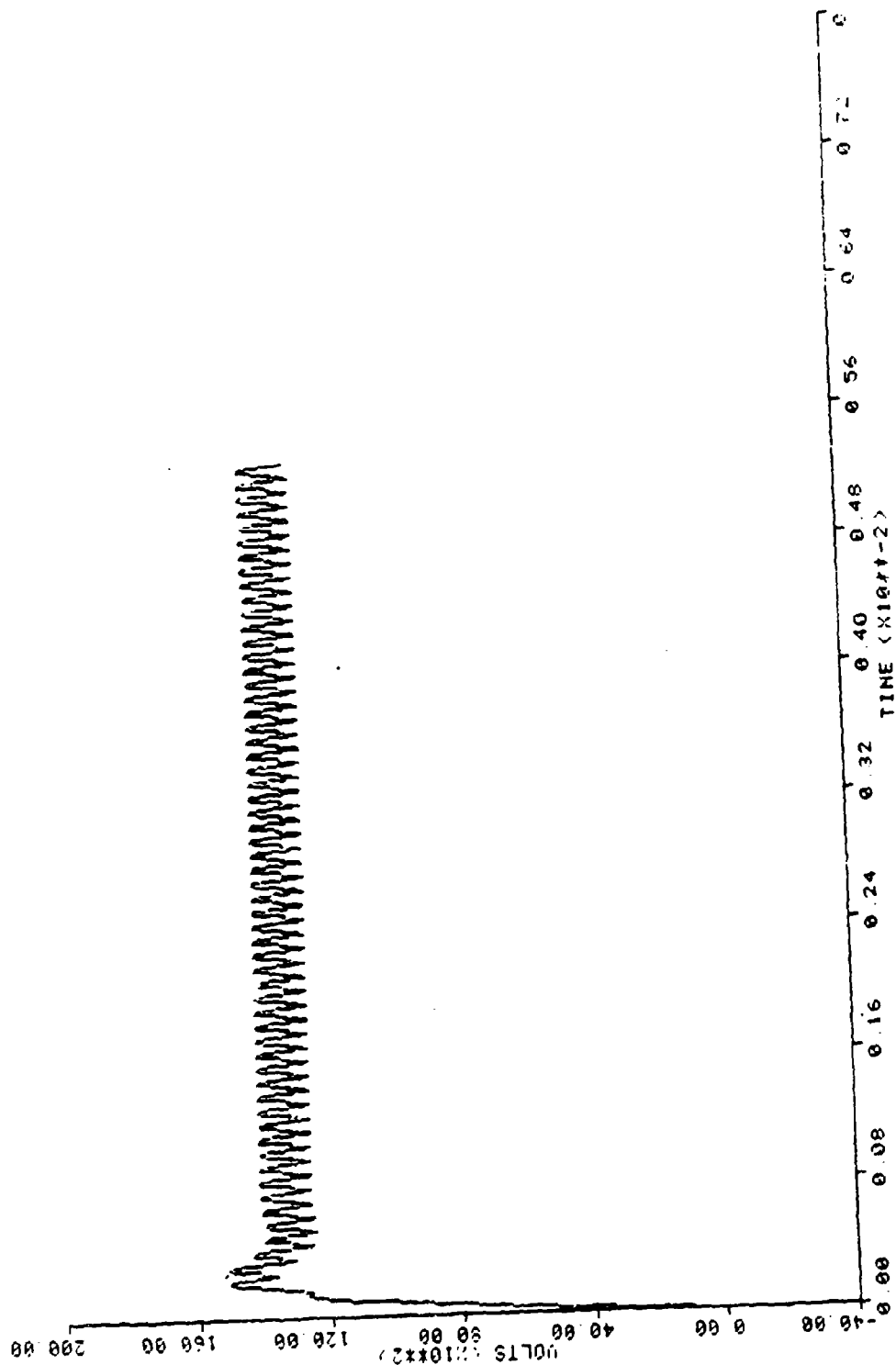
Figure 1.2.4-8

12-Pulse Power Supply Ripple

1-98

1.2.4.2   Computer Studies   (Continued)

The phase-back power supply for the 400-Hz inverter was modeled on the computer. The original analysis was done on a different computer from the analysis done on the HVPS. The analysis showed that the generator voltage was greatly distorted by the phase-back power supply. For 300 volts out at the lowest operating frequency of the HVPS, a phase-back angle of 57° was required. This phase-back angle (the angle from the crossing of the input sine waves at which a Silicone Controlled Rectifier (SCR) turns on) occurs near the natural commutation point of the HVPS rectifiers. Qualitatively, it was suspected that there would be significant interaction between the two power supplies. The ripple on the HVPS would increase. The amount of increase could not be calculated without simulating the two power supplies on the computer. It was also suspected that the distortion of the line voltage would also cause false commutation, which could lead to unstable operation of the system.

It would have been possible to take the voltage data from this computer run as an input to the HVPS. This would have given the ripple output. Unstable operation would not necessarily have been predicted because the input voltage would not have been affected by the HVPS.

It was decided to model the complete system using Simulation Program with Integrated Circuit Emphasis (SPICE). The first step in developing this total model was to model the SCR phase-back power supply by itself.

No transformers are used in the phase back power supply since operation is directly from the power line. In place of the diode bridge a full control SCR bridge is used.

1.2.4.2   Computer Studies   (Continued)

A diagram for the SCR phase-back rectifier for computer analysis is shown in
Figure 1.2.4-9.   One SCR model is also shown.   The pulse sources for the SCRs
are set to turn on the SCRs in the proper sequence.   The phase-back angle is
set to 60°.   In the actual equipment the phase-back angle would be variable
depending on the input voltage.   A variable time was not necessary for the
analysis.   A 60° phase-back angle on a full bridge is the angle at which
current conduction between phases becomes discontinuous in the ideal case.
This represents the worst case harmonic content in the input current.   Figure
1.2.4-10 is the computer-calculated line current waveform.   Figure 1.2.4-11 is
the calculated SCR voltage waveform for the same conditions.   The good
agreement between the theoretical and calculated waveforms indicates that the
model was accurate.

The line voltage waveform at the generator terminals is shown in Figure
1.2.4-12.   This waveform agrees with the previously calculated generator
voltage using a different program.

The next step was to combine the SCR phase-back power supply and the HVPS in
the same prog:.am.   The block diagram for this is shown in Figure 1.2.4-13.
There was some difficulty in getting the program to run.   The program gave a
diagnostic: "Internal timestep too small".   What this meant was that the
timestep required to achieve convergence of the algorithm was smaller than the
preset limit.   The timestep limit could have been made smaller, but the amount
of Central Processing Unit (CPU) time would have been increased.   By examining
each node voltage, it was possible to determine that the two power supplies
were causing ringing in the simulated power cable.   The values being used gave
a very high "Q" for the power line inductors.   A different model was used
which gave a more realistic value of "Q".   This program ran but the dc voltage
output of both power supplies was unstable.   The peak-to-peak ripple voltage
for the zig-zag power supply was greater than the calculated peak-to-peak
voltage for a three-phase full-wave bridge rectifier.
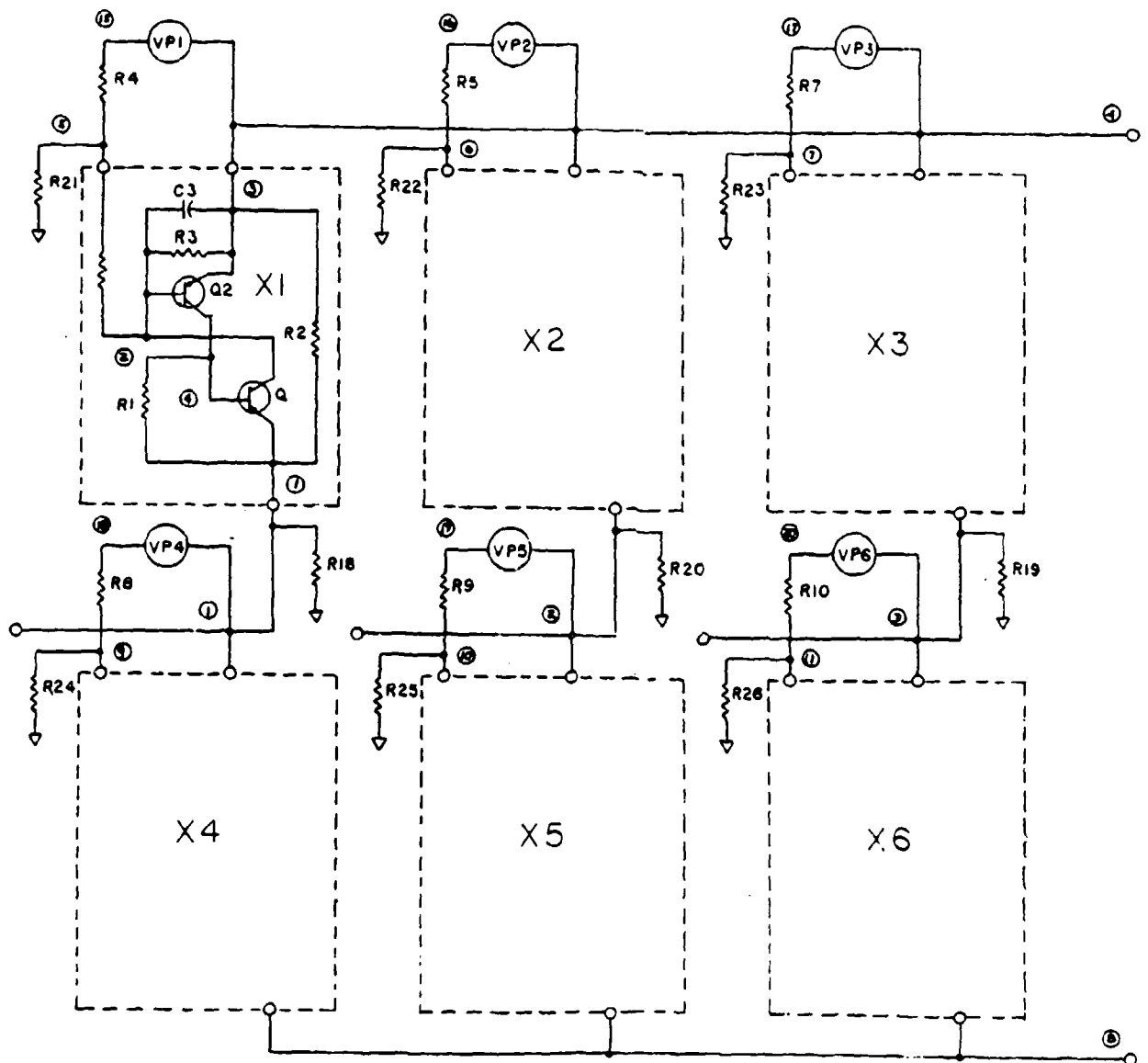
Figure 1.2.4-9

Computer Model for a Three-Phase Full-Control
Phase-Back Rectifier Showing the SCR Model

1-101
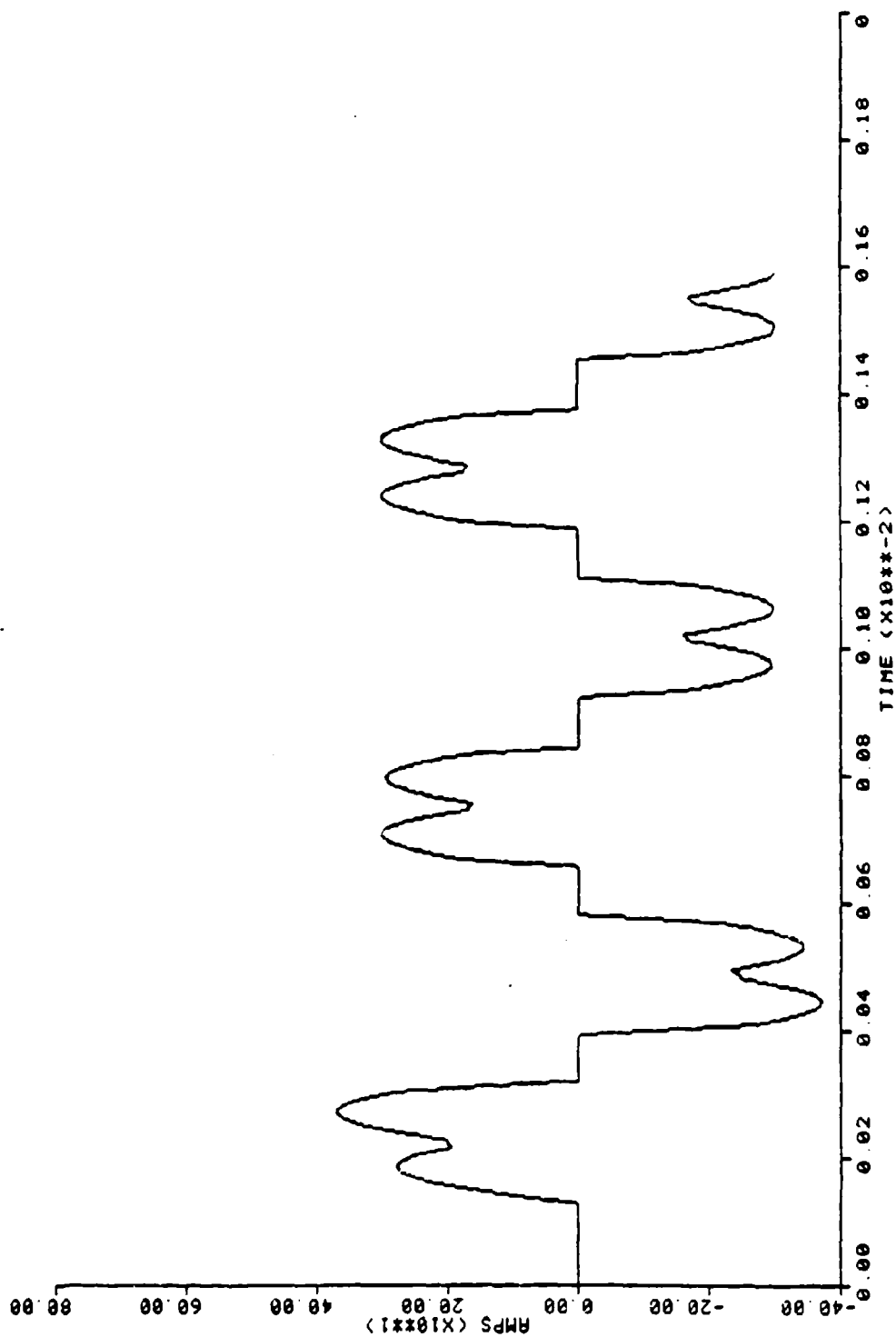
Figure 1.2.4-10

Computer Calculated Line Current for a Full-
Control Rectifier with 60-Degree Phase-Back
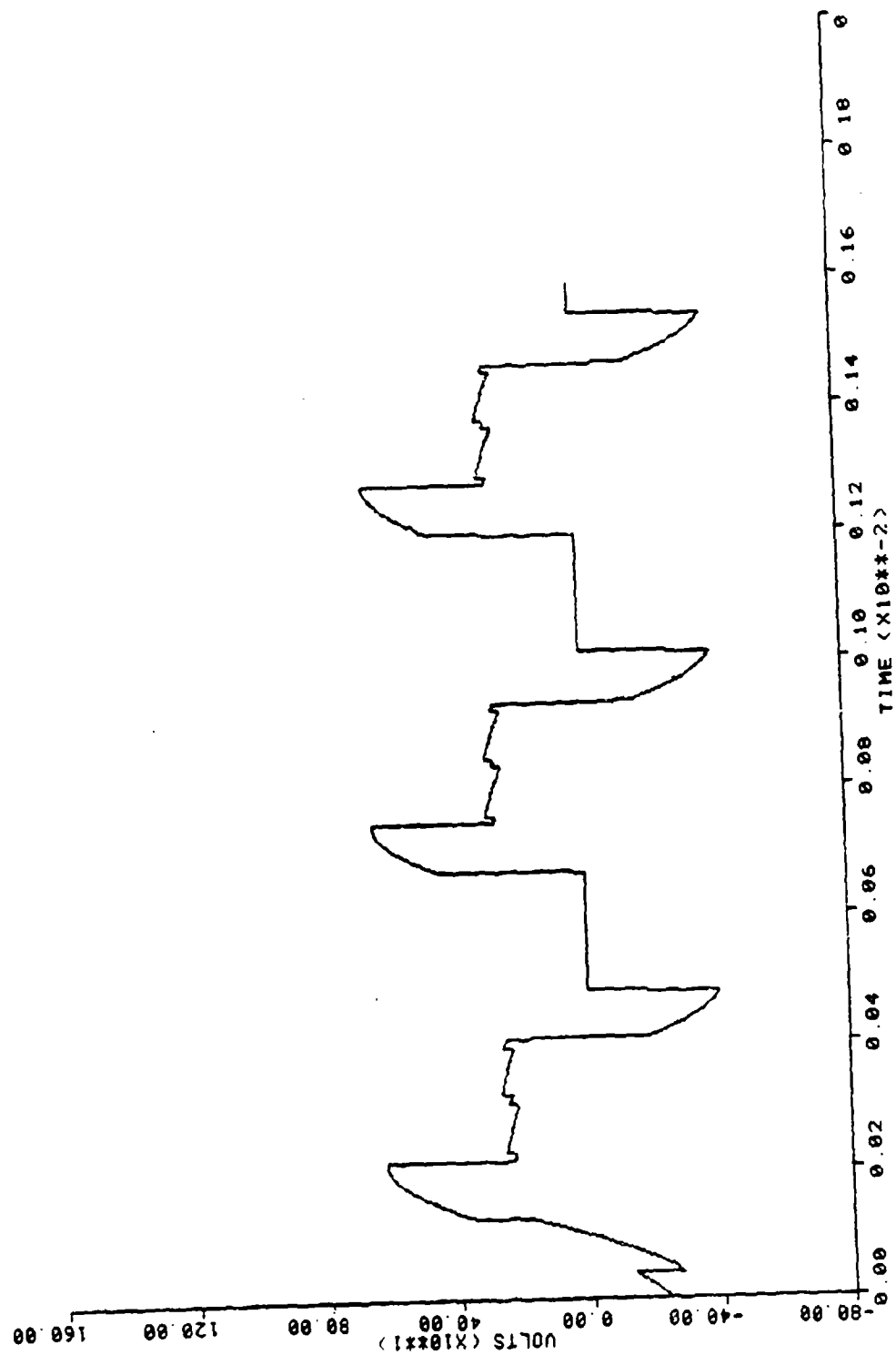
Figure 1.2.4-11

Computer Calculated SCR Voltage for a Full-
Control Rectifier with 60-Degree Phase-Back

1-103
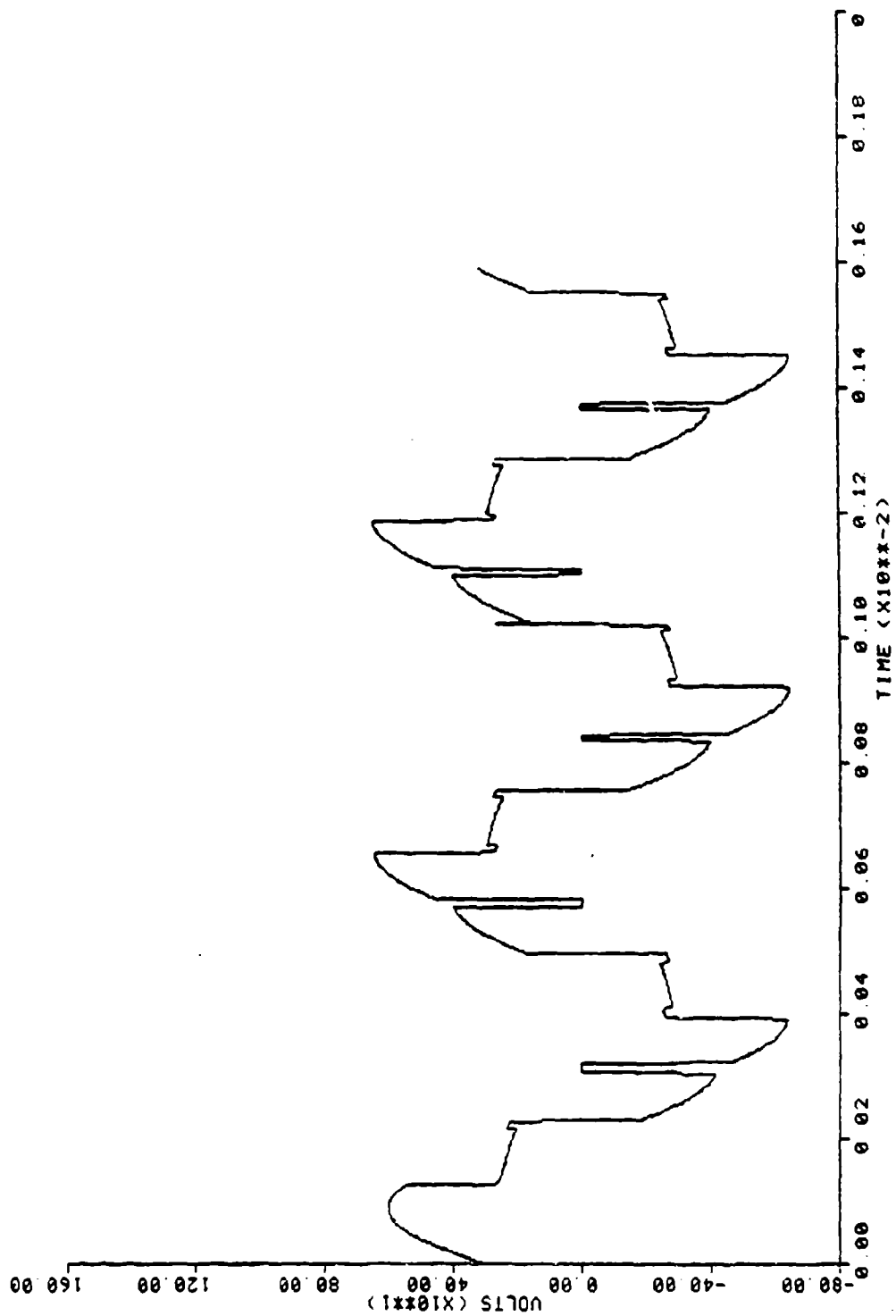
Figure 1.2.4-12

Computer Calculated Generator Voltage

with the Phase-Back Power Supply Koad

1-104
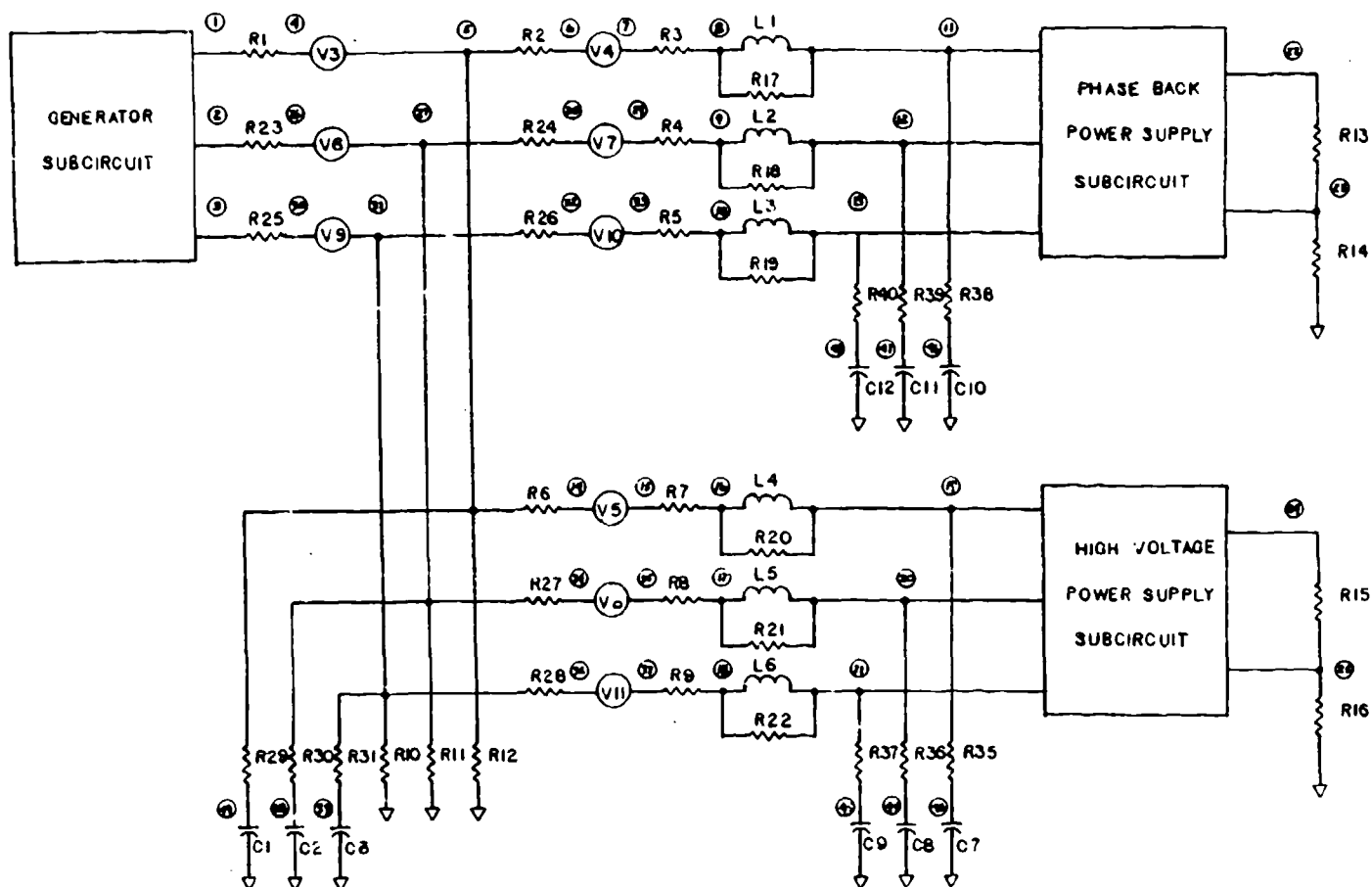
Figure 1.2.4-13

Block Diagram for the Computer Model for the

Combined HVPS and Phase-Back Power Supply

1-105

1.2.4.2   Computer Studies   (Continued)

The line and generator voltages and currents were recalculated using a conventional three-phase bridge and an L-C filter on the dc output. These calculations were done with 1 µf line capacitors at the inputs of each power supply and at the output of the generator. The line voltages at the generator, phase-back power supply, and the HVPS are shown in Figures 1.2.'-14, 1.2.4-15, and 1.2.4-16. The currents are in Figures 1.2.4-17, 1.2.4-18, and 1.2.4-19. One version of the program is shown in Figure 1.2.4-20. This program is the date input for a transient analysis using SPICE.

A harmonic filter was calculated for the input of each power supply. A computer run was made with these filters in the line. The line voltages for the generator, phase-back power supply, and HVPS are shown in Figures 1.2.4-21, 1.2.4-22, and 1.2.4-23. The corresponding currents are shown in Figures 1.2.4-24, 1.2.4-25, and 1.2.4-26. The use of harmonic filters reduced the dc ripple to the theoretical level for the rectifier circuit.

If harmonic filters are used on the inputs of each power supply, the source voltage is approximately sinousoidal. Under these conditions, the output ripple would be equal to the theoretical value. Each of these filters weighs 75 pounds. The total weight of harmonic filters for each generator would be 300 pounds.

If we allow the waveform to be distorted, the ripple from the HVPS is increased and a dc filter is required. The dc filter for each high voltage power supply weighs 15 pounds. In addition to the dc filter, line stabilization capacitors are required. Nine capacitors are required for each output of the generator for a total of 18 capacitors. The capacitors weigh 3 pounds each for a total of 54 pounds. The weight of the line correction capacitors and dc filters is 84 pounds. This is 216 pounds lighter than the system with line harmonic filters.
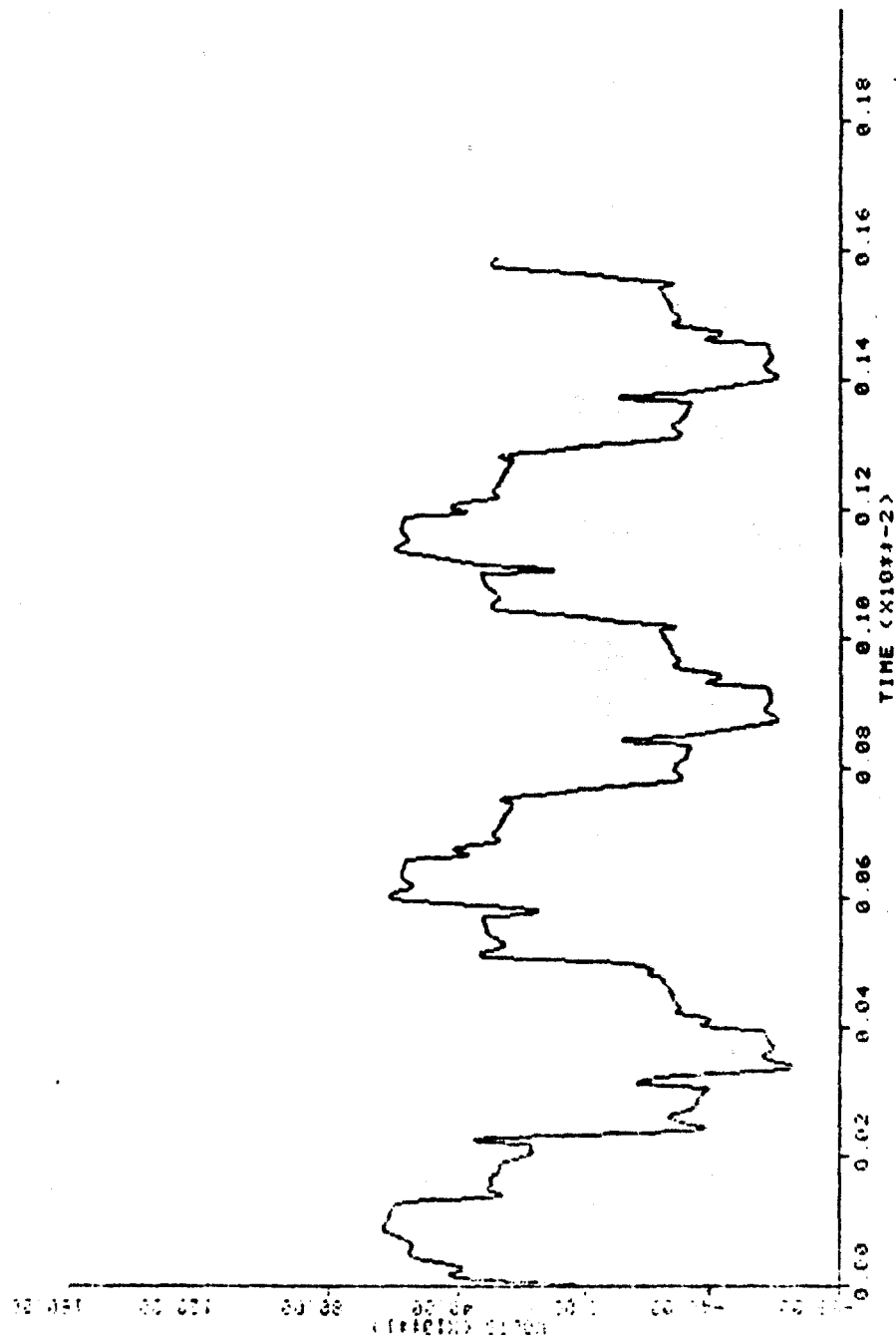
Figure 1.2.4-14

Computer Calculated Generator Voltage,

Combined System, 1 μf Line Capacitors

1-107
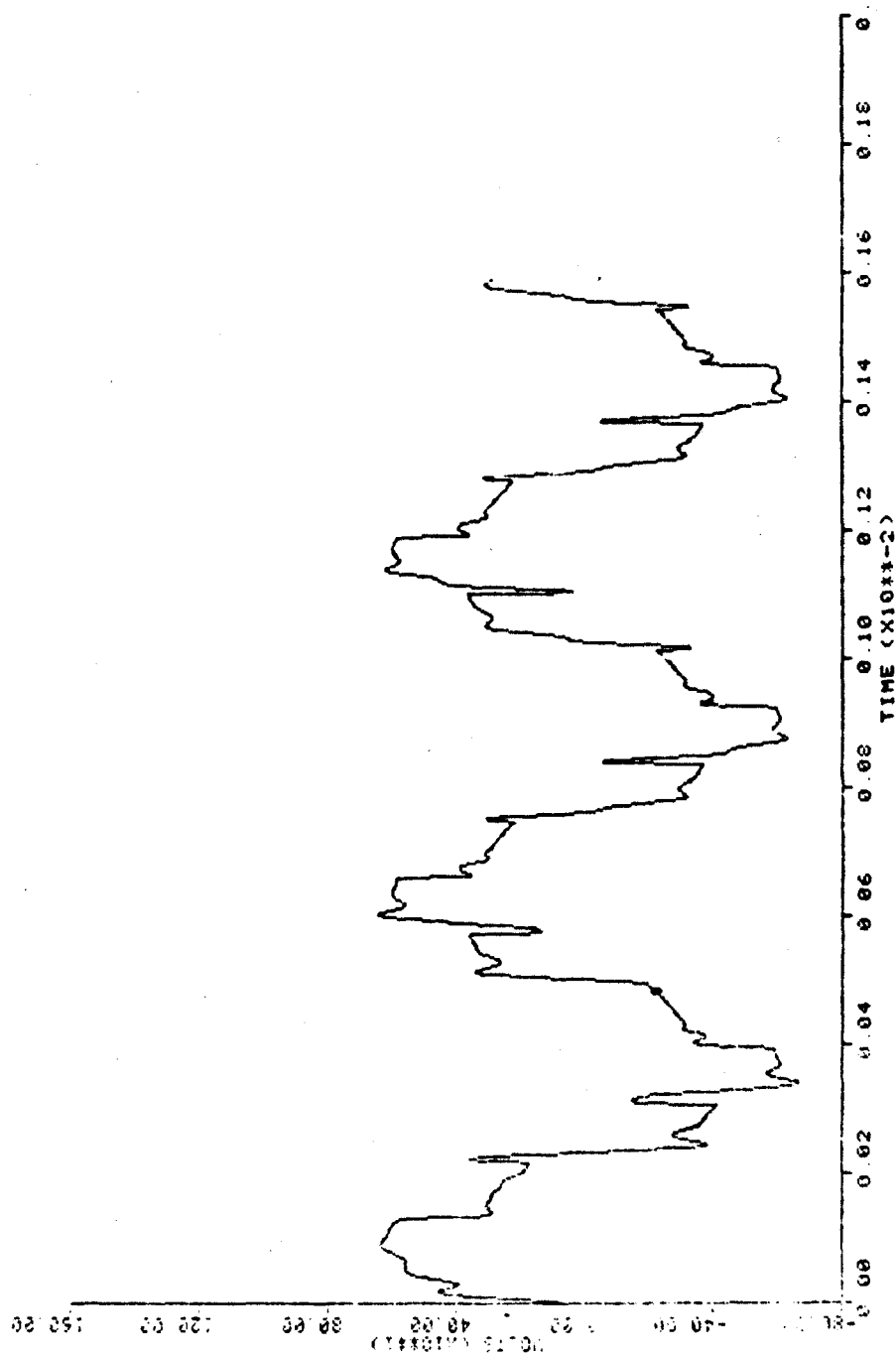
Figure 1.2.4-15

Computer Calculated Phase-Back Power Supply
Input Voltage, Combined System, 1 µf Line Capacitors
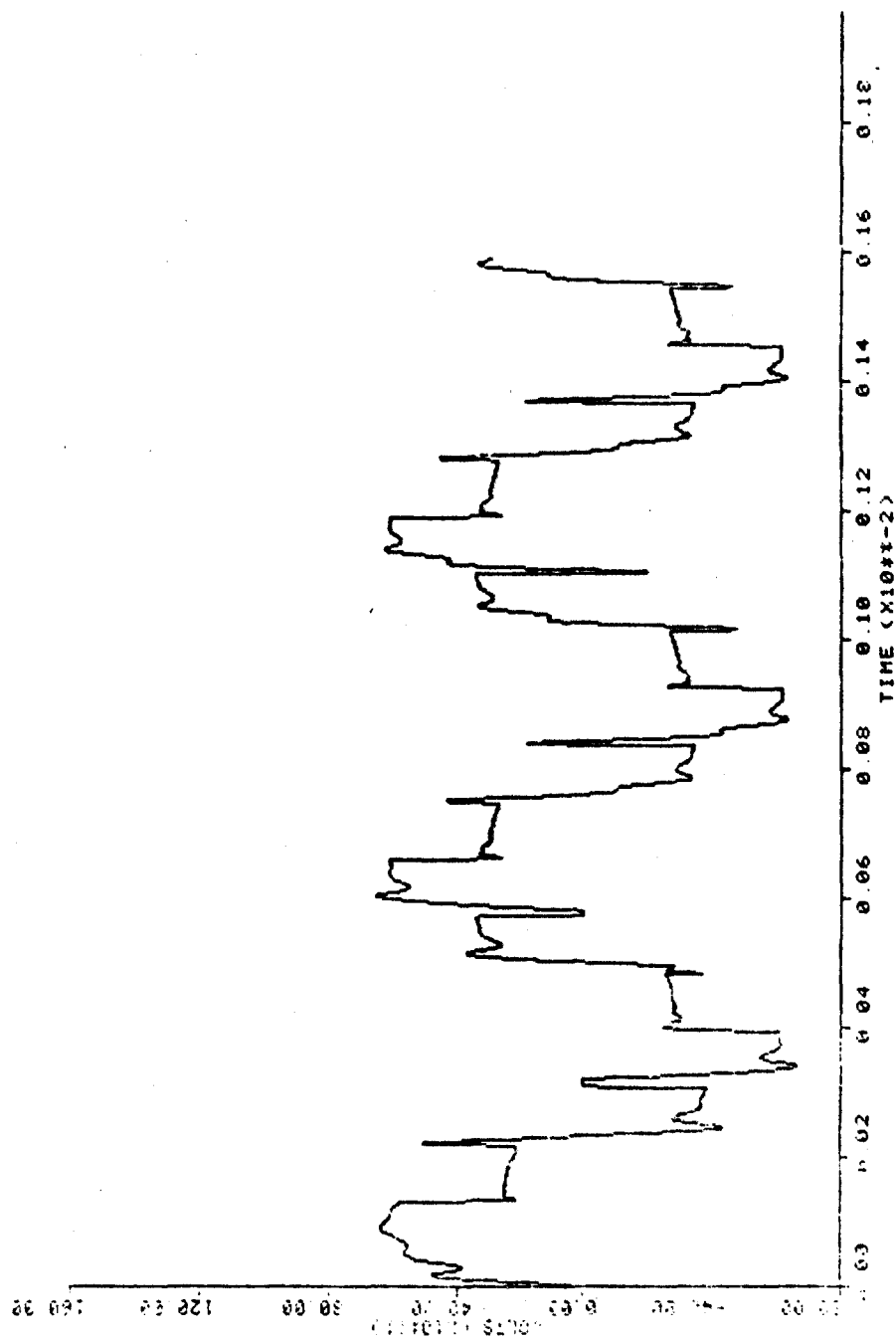
Figure 1.2.4-16

Computer Calculated HVPS Input Voltage

Combined System, 1 µf Line Capacitors
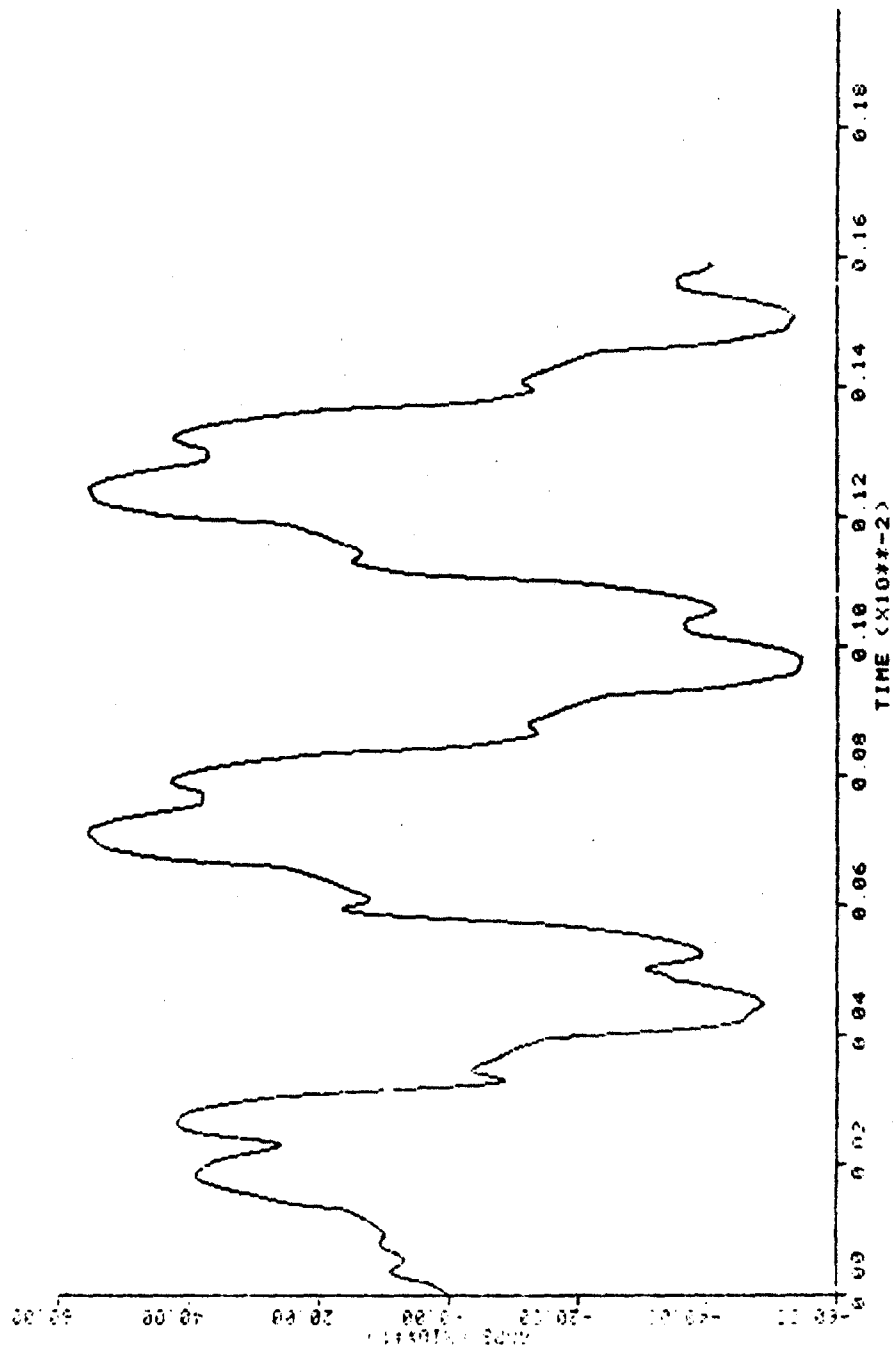
Figure 1.2.4-17

Computer Calculated Generator Current,
Combined System, 1 µf Line Capacitors
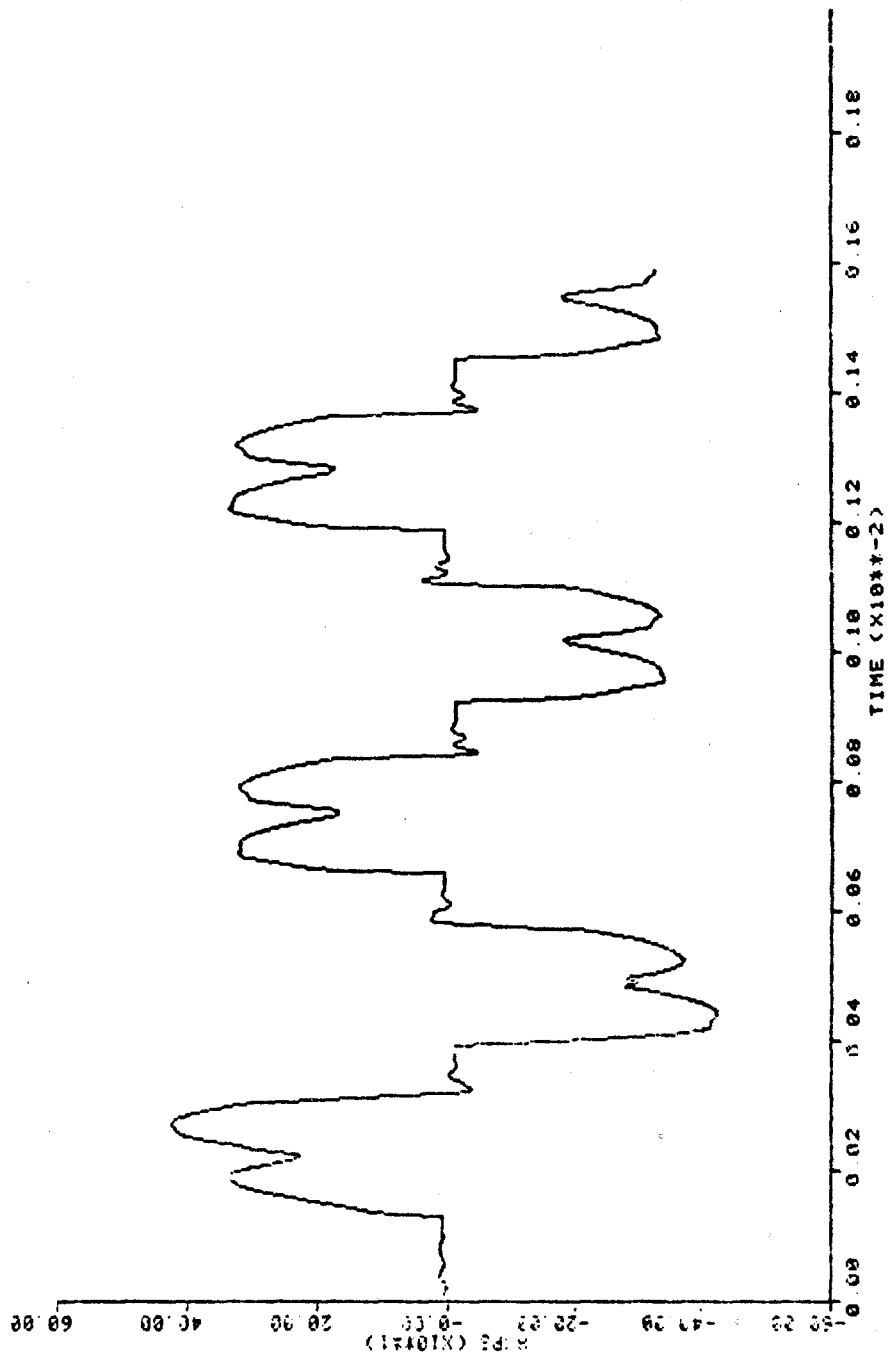
Figure 1.2.4-18

Computer Calculated Phase-Back Power Supply

Input Current, Combined System, 1 µf Line Capacitors
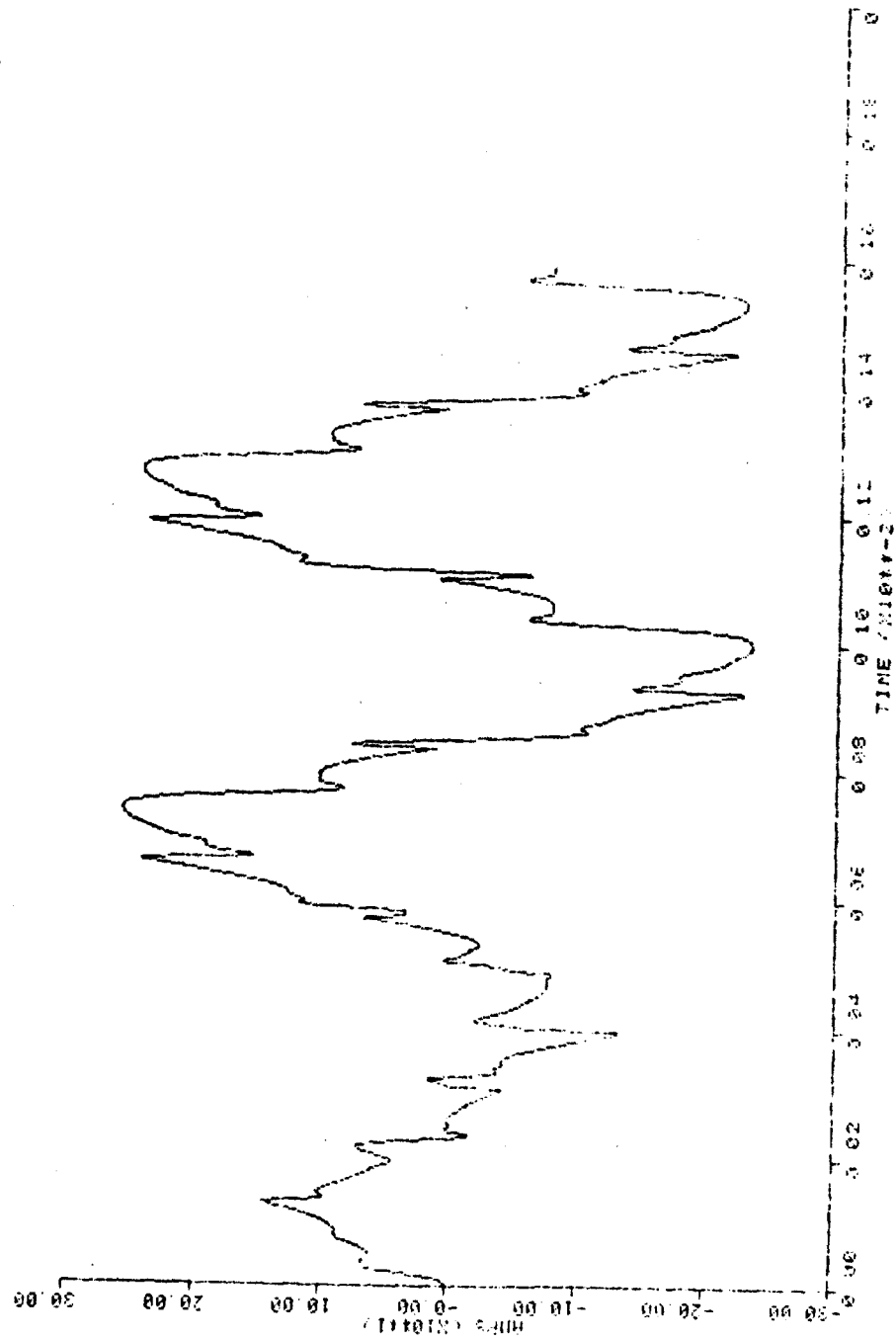
Figure 1.2.4-19

Computer Calculated HVPS Input Current,
Combined System, 1 µf Line Capacitors

```
LIMA POWER SYSTEM
.SUBCKT GEN3P 11 12 13
V1 1 10 SIN(0 362.04 1886 0 0)
E1 2 10 1 10 -1
EA 6 19 1 10 1
EB 7 17 3 10 1
EC 8 18 4 10 1
C1 2 3 146.16U IC=313.53
C2 1 4 48.72U IC=-313.53
L1 14 11 12U
L2 15 12 12U
L3 16 13 12U
R1 1 3 1
R2 2 4 1
R3 1 0 10MEG
R4 2 0 10MEG
R5 3 0 10MEG
R6 6 0 10MEG
R7 7 0 10MEG
R8 8 0 10MEG
R9 6 14 .011
R10 7 15 .011
R11 8 16 .011
R12 11 0 10MEG
R13 12 0 10MEG
R14 13 0 10MEG
R15 14 11 10
R16 15 12 10
R17 16 13 10
R18 19 0 1U
R19 17 0 1U
R20 18 0 1U
R21 10 0 10MEG
.ENDS GEN3P
```

Figure 1.2.4-20

Typical Computer Input for SPICE

```
.SUBCKT SCR 1 2 3
C3 2 3 .1U
Q1 2 4 1 Q1MOD
Q2 4 2 3 Q2MOD
R3 2 3 100
R1 1 4 100
R2 4 3 100K
.MODEL Q1MOD PNP
.MODEL Q2MOD NPN
.ENDS SCR
.SUBCKT XFMR1 1 2 3 4
L1 5 2 6.4M
L2 6 4 1.18
L3 7 3 5.06M
K1 L1 L2 1
C1 8 4 200P
R1 1 5 2M
R2 5 2 1300
R3 6 4 260K
R4 6 7 .37
R6 3 4 10MEG
R7 7 3 1K
R8 3 8 100
.ENDS XFMR1
.SUBCKT RECT3P 1 2 3 4 5
D1 1 4 DMOD
D2 5 1 DMOD
D3 2 4 DMOD
D4 5 2 DMOD
D5 3 4 DMOD
D6 5 3 DMOD
C1 4 6 390P
C2 7 5 390P
C3 4 8 390P
```

Figure 1.2.4-20 (Continued)

Typical Computer Input for SPICE

```
C4 9 5 390P
C5 4 10 390P
C6 11 5 390P
R1 6 1 1.3K
R2 1 7 1.3K
R3 8 2 1.3K
R4 2 9 1.3K
R5 10 3 1.3K
R6 3 11 1.3K
R7 4 6 10MEG
R8 7 5 10MEG
R9 4 8 10MEG
R10 9 5 10MEG
R11 4 10 10MEG
R12 11 5 10MEG
R13 1 4 100K
R14 5 1 100K
R15 2 4 100K
R16 5 2 100K
R17 3 4 100K
R18 5 3 100K
R19 1 0 100MEG
R20 2 0 100MEG
R21 3 0 100MEG
R22 4 0 100MEG
R23 5 0 100MEG
.MODEL DMOD D
.ENDS RECT3P
.SUBCKT PBACK 1 2 3 13 8
X1 1 5 4 SCR
X2 2 6 4 SCR
X3 3 7 4 SCR
X4 8 9 1 SCR
X5 8 10 2 SCR
```

Figure 1.2.4-20 (Continued)

Typical Computer Input for SPICE

```
X6 8 11 3 SCR
L1 12 13 4U IC=245
C1 21 8 650U IC=270
R2 4 12 .005
R3 12 13 100
R4 15 5 10
R5 16 6 10
R7 17 7 10
R8 18 9 10
R9 19 10 10
R10 20 11 10
R18 1 0 10MEG
R19 3 0 10MEG
R20 2 0 10MEG
R21 5 0 10MEG
R22 6 0 10MEG
R23 7 0 10MEG
R24 9 0 10MEG
R25 10 0 10MEG
R26 11 0 10MEG
R27 1 4 100K
R28 2 4 100K
R29 3 4 100K
R30 8 1 100K
R31 8 2 100K
R32 8 3 100K
R33 13 21 5M
VP1 15 4 PULSE(-2 10 128.14U 5U 10U 100U 530.22U)
VP2 16 4 PULSE(-2 10 304.88U 5U 10U 100U 530.22U)
VP3 17 4 PULSE(-2 10 481.62U 5U 10U 100U 530.22U)
VP4 18 1 PULSE(-2 10 393.25U 5U 10U 100U 530.22U)
VP5 19 2 PULSE(-2 10 39.769U 5U 10U 100U 530.22U)
VP6 20 3 PULSE(-2 10 216.51U 5U 10U 100U 530.22U)
.ENDS PBACK
```

Figure 1.2.4-20 (Continued)

Typical Computer Input for SPICE

1-116

```
.SUBCKT HVPS 1 2 3 14 12
X1 1 2 5 4 XFMR1
X2 2 3 6 4 XFMR1
X3 3 1 7 4 XFMR1
X4 5 6 7 11 12 RECT3P
R1 4 0 100MEG
R3 11 13 .1
R4 13 14 1K
R5 14 15 1
L1 13 14 3.6M IC=10
C1 15 12 1.5U IC=13200
.ENDS HVPS
X1 1 2 3  GEN3P
X2 11 12 13 22 23 PBACK
X3 19 20 21 24 25 HVPS
C1 49 0 1U
C2 38 0 1U
C3 39 0 1U
C7 43 0 1U
C8 44 0 1U
C9 45 0 1U
C10 46 0 1U
C11 47 0 1U
C12 48 0 1U
R1 1 4 1U
R2 7 6 1U
R3 5 8 .016
R4 27 9 .016
R5 31 10 .016
R6 5 14 1U
R7 15 16 .016
R8 35 17 .016
R9 37 18 .016
R10 31 0 10MEG
```

Figure 1.2.4-20 (Continued)

Typical Computer Input for SPICE

```
R11 27 0 10MEG
R12 5 0 10MEG
R13 22 23 1.1
R14 23 0 10MEG
R15 24 25 1320
R16 25 0 100
R17 8 7 5
R18 9 29 5
R19 10 33 5
R20 16 19 5
R21 17 20 5
R22 18 21 5
R23 2 26 1U
R24 29 28 1U
R25 3 30 1U
R26 33 32 1U
R27 27 34 1U
R28 31 36 1U
R29 5 49 1
R30 27 38 1
R31 31 39 1
R35 19 43 1
R36 20 44 1
R37 21 45 1
R38 11 46 1
R39 12 47 1
R40 13 48 1
R41 49 0 1MEG
R42 38 0 1MEG
R43 39 0 1MEG
R44 43 0 1MEG
R45 44 0 1MEG
R46 45 0 1MEG
R47 46 0 1MEG
```

Figure 1.2.4-20 (Continued)

Typical Computer Input for SPICE

```
R48 47 0 1MEG
R49 48 0 1MEG
L1 8 7 4U
L2 9 29 4U
L3 10 33 4U
L4 16 19 4U
L5 17 20 4U
L6 18 21 4U
V3 4 5 0
V4 6 11 0
V5 14 15 0
V6 26 27 0
V7 28 12 0
V8 34 35 0
V9 30 31 0
V10 32 13 0
V11 36 37 0
.OPTIONS ITL5=0 LIMPTS=1000 LVLTIM=1 NODE
.TRAN 2.0711U 1.5907M UIC
.PRINT TRAN V(22,23) V(24,25) V(1) V(1,2) V(2,3) V(3,1)
.PRINT TRAN V(11,12) V(12,13) V(13,11) V(19,20) V(20,21)
V(21,19)
.PRINT TRAN I(V3) I(V6) I(V9) I(V4) I(V7) I(V10)
.PRINT TRAN I(V5) I(V8) I(V11)
.FOUR 1886 V(1,2) V(11,12) V(19,20)
.END
```

Figure 1.2.4-20 (Continued)

Typical Computer Input for SPICE
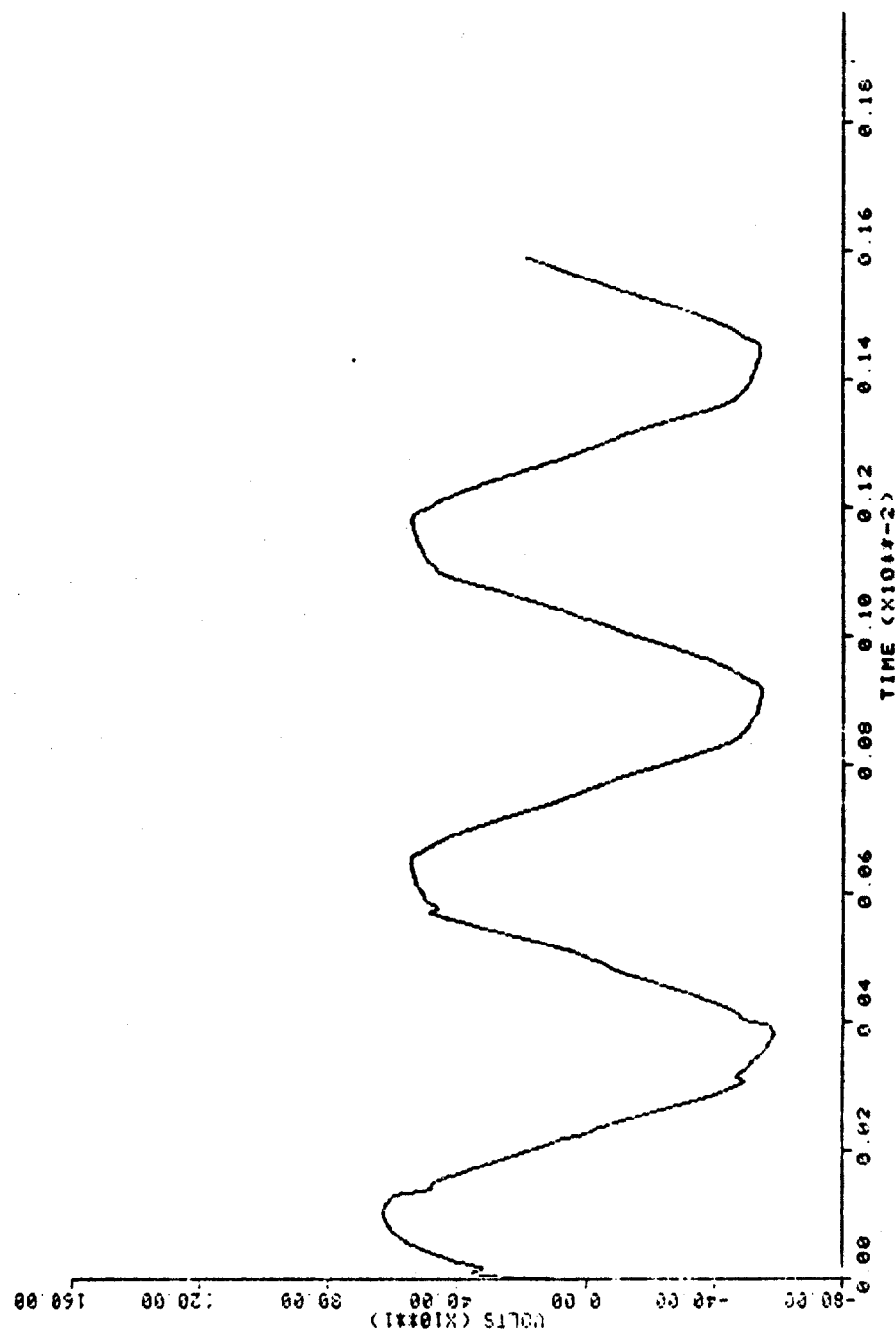
Figure 1.2.4-21

Computer Calculated Generator Voltage, Combined System,
Harmonic Filters in Each Power Supply Input

1-120
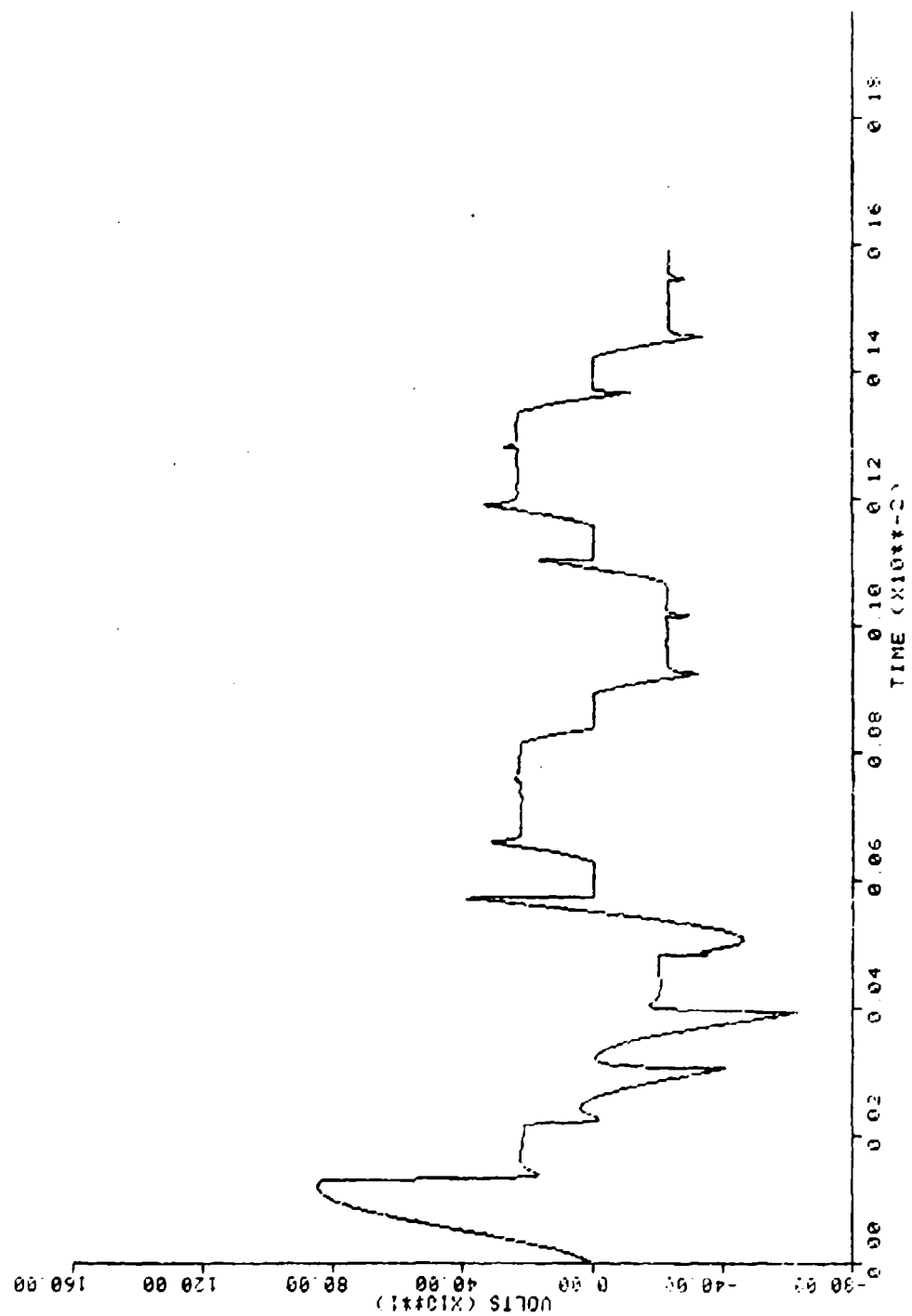
Figure 1.2.4-22

Computer Calculated Phase-Back Power Supply Input Voltage,
Combined System, Harmonic Filters in Each Power Supply Input

1-121
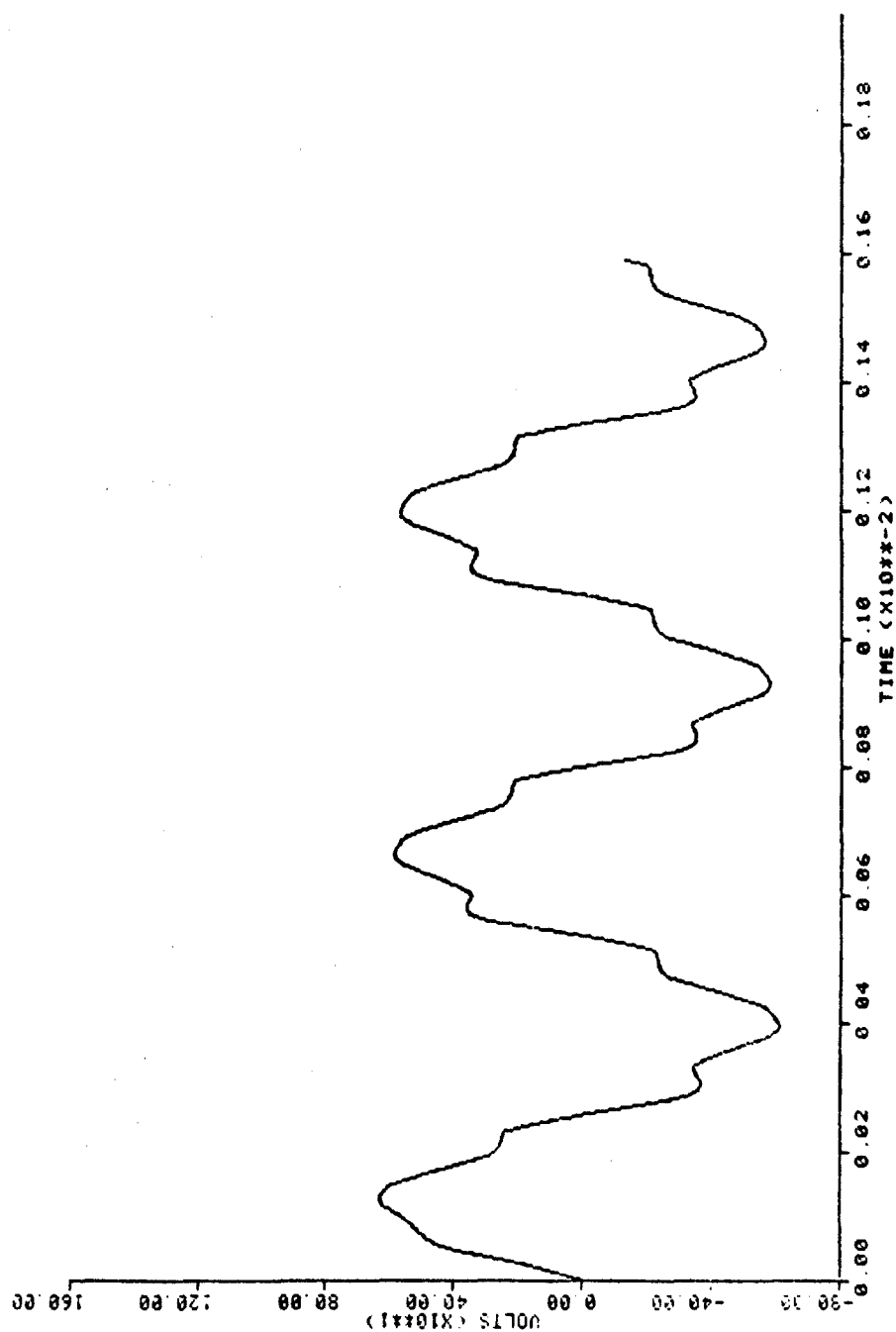
Figure 1.2.4-23

Computer Calculated HVPS Input Voltage,

Combined System, Harmonic Filters in Each Power Supply Input

1-122
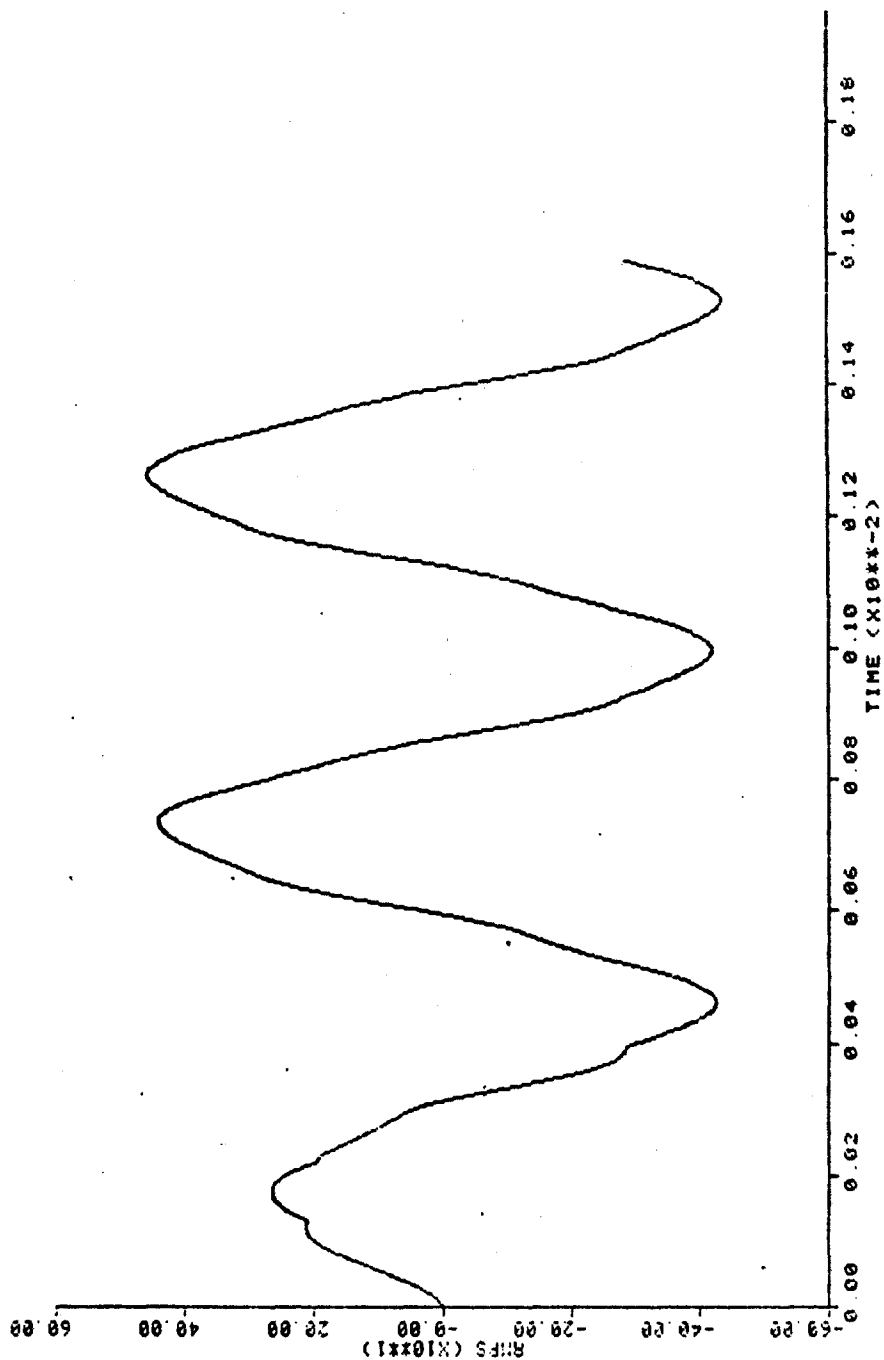
Figure 1.2.4-24

Computer Calculated Generator Current,

Combined System, Harmonic Filters in Each Power Supply Input

1-123
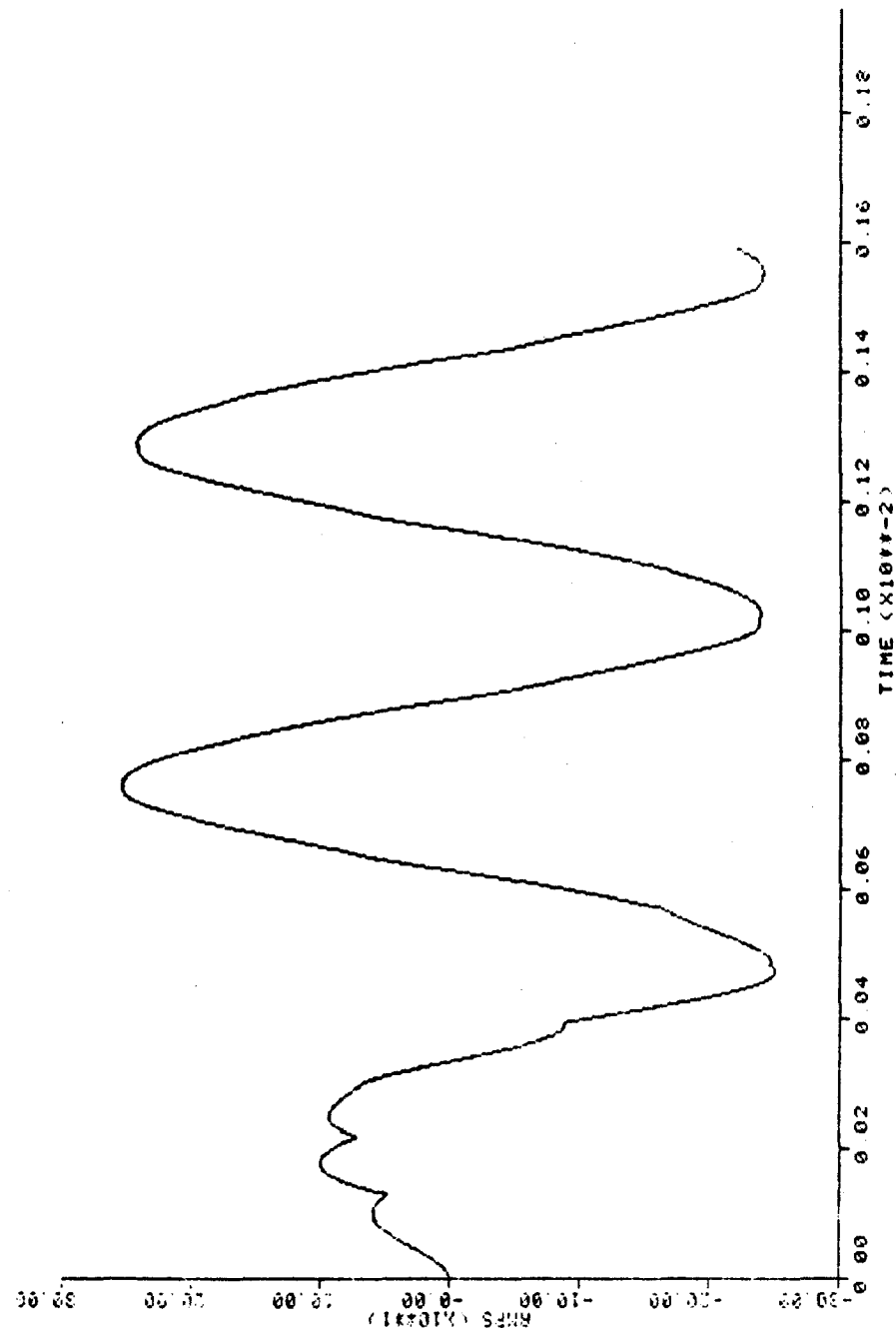
Figure 1.2.4-25

Computer Calculated Phase-Back Power Supply Input Current,
Combined System, Harmonic Filters in Each Power Supply Input

1-124
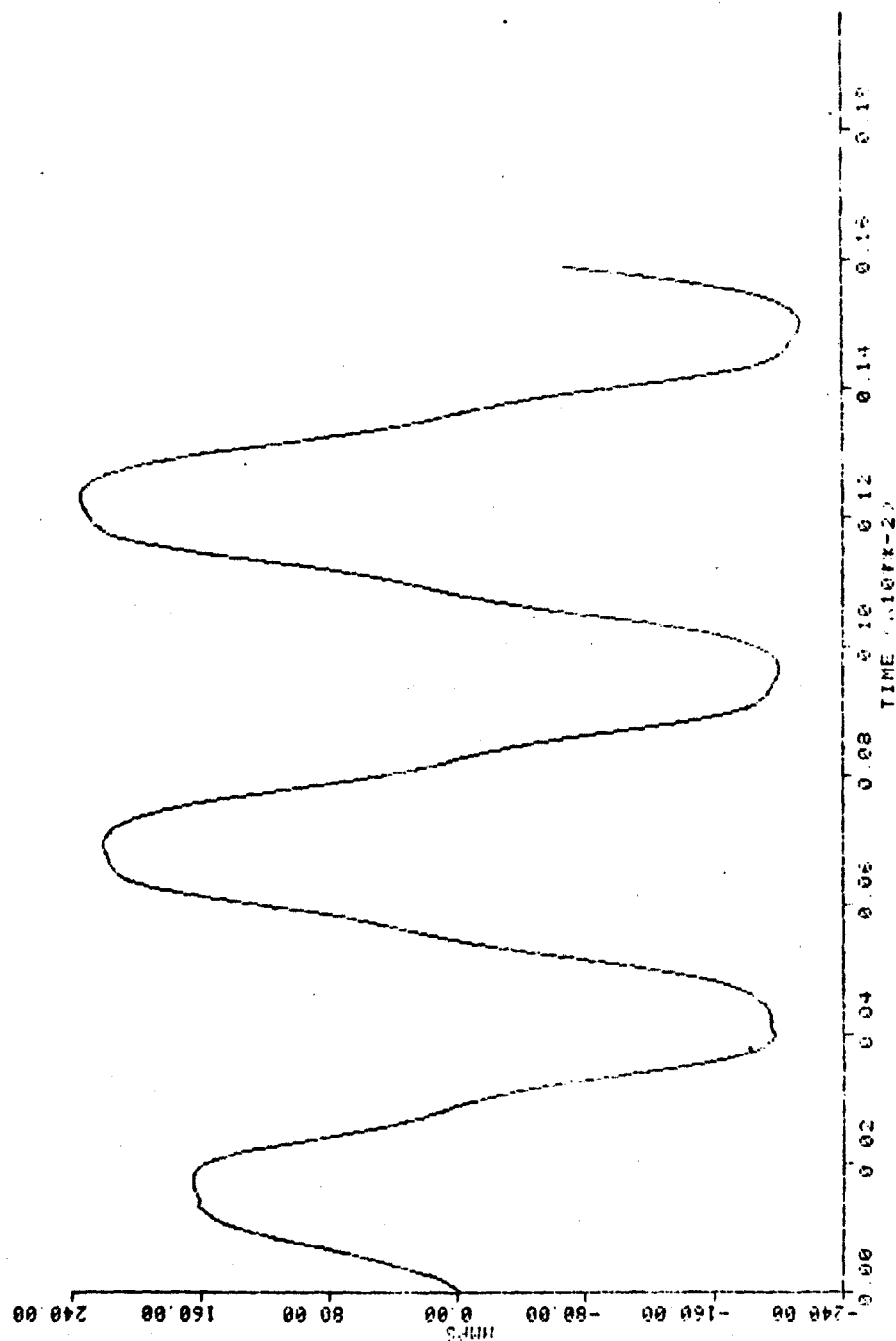
Figure 1.2.4-26

Computer Calculated HVPS Input Current, Combined
System, Harmonic Filters in Each Power Supply Input

1-125

1.2.4.2   Computer Studies   (Continued)

The line harmonic filters must be designed to work into a given load at a
given frequency. At other frequencies or loads, the filters can resonate
internally or cause resonant rise in the output voltage. These conditions are
predictable but would probably be difficult to avoid at some point within the
generator frequency range.

There could also be problems with interactions between the filter for the
phase-back supply and the filter for the HVPS.

As a result of the studies made on the electrical circuit, the following
conclusions were reached:

1.   There is no advantage to be gained from using an inverter.

2.   Line harmonic filters could eliminate the need for dc filters for the HVPS.

3.   Line harmonic filters are not necessary for the system to work. They may
     cause additional problems.

4.   Line stabilizing capacitors are required.

5.   Without line harmonic filters, the double zig-zag power supply originally
     proposed has no advantages over a conventional three-phase bridge
     rectifier.

1.2.4.3   Selection of Insulation System

The previous paragraphs have discussed the various studies used to determine
the best electrical design for this particular application. However, the
advantages of a good electrical design can be defeated if the mechanical
design and insulation system are not compatible with the electrical design.

1.2.4.3   Selection of Insulation System   (Continued)

The conditions in the requirements that are used to determine the mechanical design are:

1. Operational Altitude
2. Personnel Safety
3. Voltage and Power Levels
4. Size and Weight

The impact of each of these factors on the choice of mechanical design are discussed below.

1.2.4.3.1   Operational Altitude

In normal operation, the HVPS is enclosed in a part of the aircraft where the equivalent altitude is below 10,000 feet. However, it is necessary for the HVPS to operate at the operational altitude of the aircraft. To do this requires extremely large spacings between the components of the power supply to hold off the operating voltages at 50,000 feet. Since the spacings required are impractical, some form of controlled environment is indicated. A controlled environment implies some form of container for the environment.

1.2.4.3.2   Personnel Safety

Personnel safety implies an enclosed high voltage area. It also requires high voltage connections between units by means of shielded cables with enclosed connectors. The container for the controlled environment provides the safety features for the HVPS. A container requires connectors for the high voltage output.

1.2.4.3.3   Voltage and Power Level

Previous paragraphs considered the need for an enclosure. The basic
insulation need can be met by the use of sea level air in some form of plastic
container. If the voltage levels are low (less than 1kv) and the power levels
not too high (less than 10 kw), a plastic container is probably satisfactory.

Sea level air is a poor insulator and a poor coolant. The variations in the
composition of air also make its performance as an insulator unpredictable.
At 13.2kv and 280 kw a better insulator and coolant must be used. (In
discussing coolant we are looking at the medium used to transfer heat from the
components to the final heat sink coolant.)

Insulators can be solids, liquids, or gases. Coolants are either liquids or
gases. Liquids as coolants can be used with or without a change of state
(ebullient cooling).

1.2.4.3.4   Size and Weight

Transformers in a power supply are usually the largest and heaviest components
in a power supply. The size of the transformer is controlled by the heat it
can dissipate within the temperature limits of the materials used in the
construction of the transformer. Therefore, the size of a transformer is a
function of the operating temperature of the transformer. In high voltage
transformers, the size may be determined by the spacings needed for voltage
clearances.

Ebullient cooling can remove very large amounts of heat. Transformer size can
be minimized. This technique however, has some very basic disadvantages for
this application.

1.   There must be some means of recondensing the coolant. Usually this must
     be at or near the top of the container. In a moving vehicle of changing
     attitudes this condition is difficult to achieve.

1.2.4.3.4.   Size and Weight (Continued)

2. At cold temperatures the vapor pressure may not be sufficient to maintain
    the electric strength needed.

3. The materials used are high molecular weight per fluorocarbons. The
    weight of the liquid may offset any weight savings achieved by reducing
    the size of the transformer.

Liquids are also used as insulators and coolants. There are many materials in
this class from mineral oils to silicones. Perfluorocarbons can be used as
liquids without boiling. Liquids completely cover the high voltage
components. There are several disadvantages to using liquid coolants in
airborne equipment.

1. Some means must be provided for thermal expansion of the liquid. This can
    be done by allowing air space in the top of the container, providing a
    bellows or allowing the container to breathe.

2. The container must be designed to maintain a liquid over all parts at all
    operational attitudes.

3. The weight of the liquids can increase the total weight by a significant
    amount.

4. The hydrocarbon based fluids are flammable.

5. The non-flammable silicones can decompose under possible fault conditions.

The disadvantages of gases used as insulators and coolants have to do with the
design of the container. The apparent disadvantages are:

1-129

1.2.4.3.4   Size and Weight (Continued)

1. The container must be of spherical or cylindrical shape to withstand the
    pressure. The wall thickness and therefore the weight for small vessels
    at low pressures is controlled by the thickness of the material required
    to support the structure weight. It is often difficult to obtain a good
    packaging spacing. Minimum spacing is limited by voltage clearances.

2. Possible explosion if the tank is accidentally penetrated. This safety
    hazard is controlled by proper tank design.

3. The cylindrical shape is not optimum for packaging the components.

Gases, while they have some disadvantages, also have certain advantages in
airborne equipment. Some of the advantages are:

1. Gases are lightweight. Even in large containers at higher pressures the
    weight of the gas will be only a few pounds.

2. Gases have high operating temperatures. Many good dielectric gases can be
    operated at temperatures that exceed the thermal capability of many solid
    dielectrics and other components.

3. Higher molecular weight gases with forced circulation can equal the
    cooling capability of liquids under normal convection.

4. The electric strength of a gas can be controlled by using a pressure that
    makes the electric strength, heat transfer, and other properties optimum
    for the application.

5. No personnel or fire hazards.

1.2.4.3.4   Size and Weight   (Continued)

In the past, gas insulation systems have been used in airborne equipment. An
insulation system of 1½ to 2 atmospheres absolute of sulfur hexafluoride (SF6)
results in the lightest weight for the HVPS.

As a result of the computer studies and other considerations, the HVPS design
selected has the following features:

1.   Two identical three-phase transformers with delta primaries and WYE
     secondaries.

2.   Two identical three-phase full wave bridge rectifiers.

3.   The dc voltage from each transformer rectifier combination will be the
     full 13.2 KV.

4.   The dc outputs will be connected in parallel through a balancing inductor.

5.   An L-C filter will be used. The values will reduce the ripple to 130V p-p
     from the ripple calculated by the computer. The ratio of L and C will be
     chosen to limit any resonant rise to 10% of the 13.2kv.

Since pressurized gas is the choice for the insulating medium, the basic
cylindrical shape is dictated. The SF6 gas in the tank will be force-
circulated through the transformers and past the other components. The gas
will be circulated through a finned area inside of the tank to transfer the
heat to the tank wall. The heat will then transfer to the cooling oil or
water. The medium that will be used will be selected at the final design.
Details of the design will be discussed in section 3.4.

1-131

1.2.5   28 Volt Power Conditioner

The 28-volt power subsystem to be described below is one part of a large EW
system to be used on an AF aircraft. This is a preliminary design to be part
of a variable speed constant frequency system where electrical performance is
of primary concern. The description below encompasses one 28-volt supply.
Three of these supplies connected in parallel are required to meet the load
requirements.

The 28-volt power conditioner is designed to provide a pulse of power to a
.01586 ohm load resistor. Although four of these supplies may be paralleled
three must be able to supply 50 kw to the load. This power pulse is supplied
for one millisecond with a 31 millisecond repetition rate. Each conditioner
must therefore supply approximately 17 kw peak or 600 watts average.

The selected design approach charges a large bank of capacitors during the off
time. These capacitors then supply the load current pulse. A schedule of
events is shown in Figure 1.2.5-1

To supply 50 kw to a .01568 ohm load requires a voltage of:

$$v^2 = PR$$
$$v^2 = 50,000 \times .01568$$
$$v = 28 \text{ Volts}$$

The current will be:

$$I = 28/.01568 = 1,786 \text{ Amperes}$$

Each conditioner supplies 1,786/3 amperes.

Using the MIL-STD-704C steady state maximum of 29 volts, the average will be
28 volts if the pulse terminates at 27 volts.
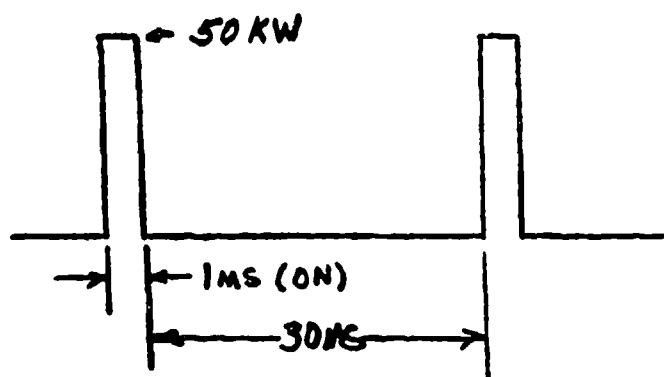
Figure 1.2.5-1

Loading on 28-vdc Supply

1-133

1.2.5   28 Volt Power Conditioner   (Continued)

The total change is two volts.

From C = I T/, the capacitor for each conditioner will be:

   C = 1,786/3 × .001/2 = .3 Farad

The 28 vdc power is derived from a 140-vac to 240-vac system through a
three-phase transformer. The secondary supplies a range of 38 to 65 volts.
Each conditioner contains a pulse width modulator operating at a 20 KHz rate.
Approximately 22 amps average DC current is supplied over 30 milliseconds to
raise a .3 farad capacitor from 27 to 29 volts.

1.2.6   Paralleling

Paralleling in the 200/300-kVA-conditioned power system consists of three
different paralleling systems, one for each of the three different types of
power provided by the total system. For r·.iability of mission requirements,
it is assumed that the three parallel systems are to be independent from one
another. That is, each of the systems (13.2kv dc, 115v ac, 28v dc) is capable
of parallel operation independently of the others. If a particular system
fails to perform in the parallel mode, the ability of the other system types
to function in the parallel mode is not affected, at least to the maximum
extent possible. Further, if a channel of ac power cannot function in the
parallel mode it is capable of functioning in the separate or isolated mode.

The protection functions for parallel operation are the same as for non-
parallel operation, plus there is the capability of selectively detecting and
isolating the failed channel.

1.2.6　　　　Paralleling　(Continued)

Initially, only one channel of prototype hardware is to be built, hence parallel operation will not be possible. To verify the performance of the system under parallel operation, a computer simulation was developed. The program is an extension of one already developed at Westinghouse Lima to assist in the paralleling development for 400-Hz VSCF systems that has been underway for several years now. The simulation is a specialized program rather than a "canned" general purpose program. The Euler method is used. It was developed originally on a Hewlett-Packard 9835A desktop computer, which has virtually no-run time costs. It compares favorably with canned programs such as SPICE with respect to speed, but offers much more flexibility and is more friendly to the developer-operator. Details of the simulation program are covered in section 2.0, Theory of Operation.

The criterion for the design selection for parallel operation is discussed for the three power types in the following subparagraphs.

1.2.6.1　　　Paralleling, HVDC

To parallel dc power supplies that have approximately equal source impedances, it is only necessary to make the Thevenin voltages of the participating power supplies equal. Therefore, it is not necessary to control the generator frequency or relative phase angle between participating channels of dc systems employing transformer rectifier units (TRUs). So, the method of control for load division on the HVDC parallel system is by magnitude only. If a dc system has sufficiently large impedance between the participating channels, then the need for an active load division control loop is eliminated. The magnitude of the impedance required for such passive load division would be:

$$Z_{th} = Ve/Ie$$

1.2.6.1　　　Paralleling, HVDC　(Continued)

Where Ve is the equivalent voltage regulator set point error (or difference) between the participating voltage regulators; Ie is the error (or difference) current between channels allowed by the design specification; and Zth is the Thevenin difference impedance between the parallel channels, including the feeder impedances.

Typically, Ve is 2 percent of rated voltage and Ie is 5 percent of rated current, making the Zth equal to .02/.05 or approximately 0.4 (40 percent) of rated impedance. This represents a source impedance much higher than any real system will have; thus, passive load division control of the HVDC system cannot be considered as a practical approach.

Load division control between the participating channels will be controlled through the normal voltage regulator loop, which includes the generator. Differential load current sensing will be used to detect unequal load balance between high voltage power supplies. The unbalance error will, in turn, be used to trim the voltage regulator, thus giving closed loop control of load sharing.

Sensing the unbalance currents at the 13.2 kV dc output has problems related to the dielectric insulation from such high voltages, plus the inherent difficulty of sensing DC currents. Sensing on the ac input side of each of the participating channels is, on the other hand, a relatively simple and reliable method. For this reason ac current sensing for parallel control of the HVDC has been selected. A single wire running between the generator control units is enough to provide the necessary information for differential load sensing and control. The theory of operation of the scheme is detailed in section 2.0 of this report.

1.2.6.1   Paralleling, HVDC   (Continued)

A unique problem exists when paralleling dc systems such as described here.
Consider that one channel of a multi-channel parallel system has its voltage
regulation set point set 2 percent lower than the others, which are all set
right on. Also, consider that no load exists on the system. Under these
conditions the low channel voltage regulator tries to regulate the output to 2
percent below the others; however, the rectifier action of the TRU prevents
any reverse current and so no corrective (negative) error can be applied. The
generator excitation is therefore driven to zero by the voltage regulator.
The generator assumes an idle condition. This is not an uncommon problem with
dc rectifier parallel systems. The situation exists only at (or near) no load
on the total dc system. The dc voltage on the parallel bus is regulated
properly by the other channels. In a real system, the voltage regulator set
points are all different for each channel, so that the dc is regulated to the
one with the highest set point. Therefore, in a four-channel system three
generators are idled when at (or near) no load. The performance penalty for
such a condition is the transient response to a step applied load to such a
system. The idled generators take time to come up to full capacity and the dc
voltage droops accordingly. Only one channel can provide the total load
momentarily. Obviously, the more channels in a parallel system, the worse the
voltage droop becomes when full system load is step applied.

This peculiarity was verified on the parallel simulation program. It was
assumed that such performance could not be tolerated and so a fix was
proposed. The fix was also verified on the simulation. It consists of an
added loop that detects the error between the generator voltage and a minimum
acceptable idle voltage the generator can assume. This error voltage will
then keep the idling generator(s) voltage to approximately 90 to 95 percent of
rated voltage. Now, if a load is step applied to the unloaded parallel
system, the idling generators can respond quickly with performance similar to
the ideal (non idling) system.

1-137

1.2.6.1   Paralleling, HVDC   (Continued)

If a component in one HVDC rectifier fails shorted, such that a short circuit
is imposed on the HVDC output, then it is necessary to disconnect that channel
from the parallel bus. A normal requirement is that a single component
failure cannot shut down the entire HVDC system. A 13.2 kv dc contactor with
enough current capability for this application would be prohibitively
expensive in terms of dollars and size. On this basis it was decided to put a
rectifier diode on the output terminal of each channel of the HVDC. The diode
serves no other purpose except to isolate failed channels from the parallel
bus.

1.2.6.2   Paralleling, 28 V DC

The 28-v dc system has a load defined as one millisecond on and 30
milliseconds off with a magnitude of 50,000 watts total, or approximately 595
amperes per channel. Each channel of the 28-v dc supply is basically a
constant current device that charges a capacitor during the load off time.
When the capacitor reaches the desired 28 volts the internal circuits turn off
the constant current. The capacitor is now ready for the load pulse. The
capacitor provides all of the 595 ampere pulse and it is sized to provide this
energy while keeping the voltage near 28 volts. It is not necessary to
control the constant current charging circuits in the participating parallel
channels in a load sharing manner. If one channel charges at a higher rate,
then it is ready sooner than the others and this has no effect on the actual
load pulse sharing. All channels are ready before the load pulse occurs.

Load pulse sharing for this type of dc system is controlled by the impedances
in the feeders and the internal resistance of the capacitors. Assuming that
the feeders are 10 feet for each channel, then approximately 2.0 microhenry
feeder inductance can be assumed. With a 28-volt source, the reset time of
the current on the step applied load is: 28/2E-6 = 14 ampere per microsecond.

1.2.6.2   Paralleling, 28 V DC   (Continued)

Assuming no other inductances, full current of 595 amperes is reached in 42.5 microseconds. That is, the feeder inductances control the first 40 to 50 microseconds of the load current pulse such that each channel shares the load equally. After this transient dies out, the dc resistance of each channel's capacitor and feeder determines the load sharing. This is based on the assumption that each channel has the same value of capacitor. This type of passive load sharing is adequate for the 28-v dc system. An active system would suffer from low reliability, high losses, and high costs.

Similar to the HVDC system, the 28-v dc system uses a diode on the final output of each channel. This diode serves as the isolation device if a channel fails and needs to be removed from the parallel bus.

1.2.6.3   Paralleling, 115 V AC

As in the dc systems, to get ac systems to parallel and to share load, it is necessary to make the Thevenin voltages equal. However, this involves two variables: magnitude and phase angle. Westinghouse has, over the years, developed paralleling methods for VSCF applications. This technology was used when making the paralleling design for the 115-v ac, 120 kVA portion of this program.

VSCF systems typically have frequency stabilities in the order of tens to hundreds of parts per million with respect to time, temperature, etc. However, the crystal clocks in such systems do not lend themselves to the frequency control that is necessary to control the phase angle of the Thevenin voltage for parallel operation. Also, many parallel systems are required to momentarily parallel with a ground power unit (GPU) or auxiliary power unit (APU) with no interrupt transfer. These power sources typically operate at 400 ± 20 Hz. In order to accommodate these frequency changes it was decided early in the Westinghouse parallel development to provide 400 ± 40 Hz capability. The actual operating frequency at which a channel operates is

1-139

1.2.6.3 Paralleling, 115 V AC (Continued)

determined by a frequency reference signal. This reference is 400 Hz ± a few parts per million for all normal operations but is changed to APU or GPU frequency when the need arises. This same system will be employed on the 200/300 kVA Conditioned Power System.

Figure 1.2.6-1 illustrates a two-channel parallel ac system with the pertinent impedances shown. Voltages V1 and V2 represent the terminal voltages of the inverters shown in dotted lines. An error current, I1-I2, flows if the Thevenin voltages are not equal or if there is an unbalance in the channel to load impedances. Unbalanced current also occur if the load bus is asymetrically loaded; i.e. if one of the loads is off.

Figure 1.2.6-2 shows the two types of errors that can exist between the Thevenin voltages on an ac system. Amplitude errors result in in-phase voltage components, and phase angle errors result in quadrature voltage components. If the Thevinen impedances and the feeder impedances were primarily resistive in nature, then the resulting currents would be in phase with the error voltages. That is, the amplitude errors would cause an in-phase current or real load unbalance, whereas the phase angle errors would cause quadrature current or reactive load unblance. In most real systems, however, the Thevenin impedances and feeder impedances are mostly reactive (inductive), whether the source is a generator, inverter, or cyclo-converter. Therefore, the error currents will be in quadrature (or nearly so) as shown by Figure 1.2.6-3. For our system then, the amplitude errors will give reactive load unbalance, and phase angle errors will give real load unbalance.

A synchronous demodulator is used in each channel of the 400-Hz ac system to separate the error into the real and reactive (or imaginary) components. Real load division (RLD) and reactive (imaginary) load division (ILD) controls take the demodulated error current and control the inverter so as to drive the unbalance currents toward zero through a closed loop control system. A functional diagram is given in Figure 1.2.6-4, which includes the difference

1.2.6.3 Paralleling, 115 V AC (Continued)

current CT loop. Any number of channels can be added to the system by including their CTs in the loop. If a channel is taken off the parallel bus, then its CT is disabled by a shorting switch on the parallel bus contactor.

Figure 1.2.6-5 is a more detailed functional diagram of one channel of the parallel system control concept. Details of operation and analysis of the control concepts are covered in section 2.0 of this report.
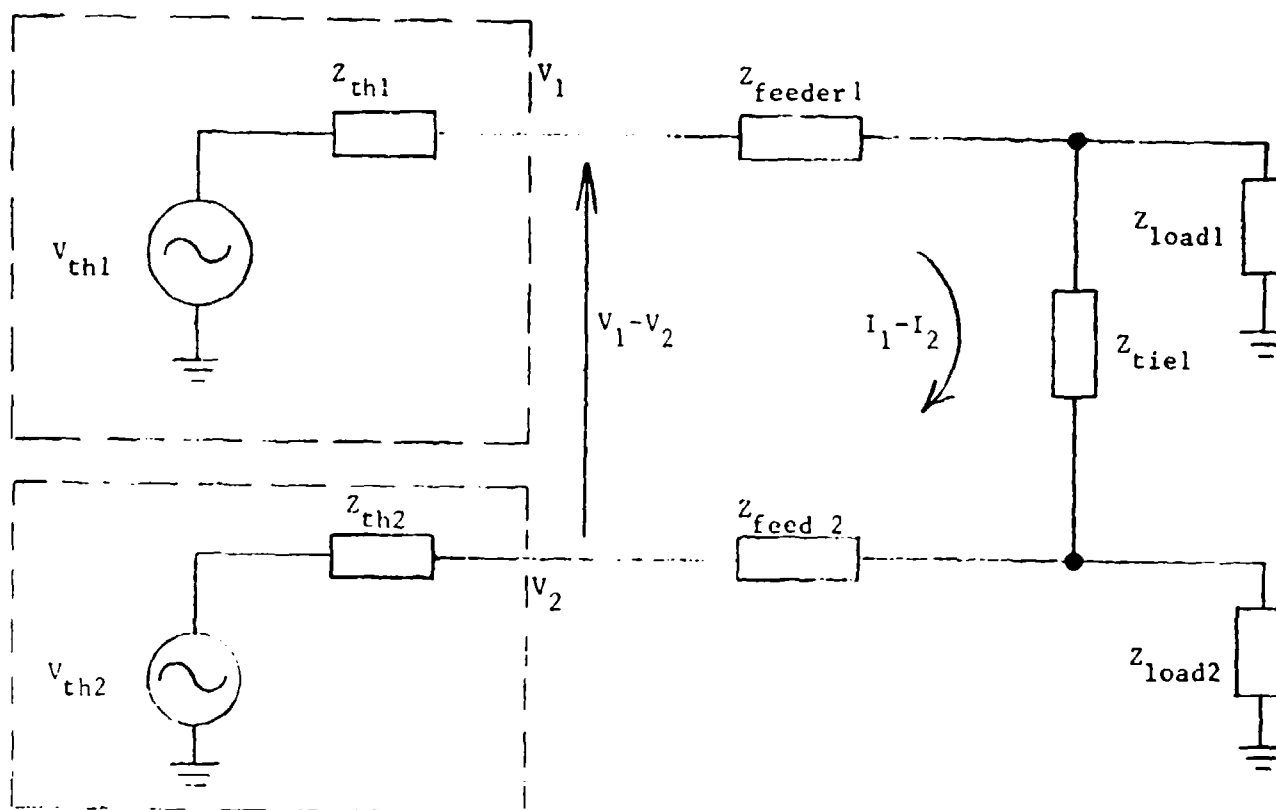
Figure 1.2.6-1

Thevenin Equivalent of Parallel System

Assuming equal feeder impedances and equal load impedances,

$$I_1 - I_2 = 0 \quad \text{if} \quad V_1 - V_2 = 0$$

Z_{th} and Z_{feed} are resistive

Amplitude Errors:
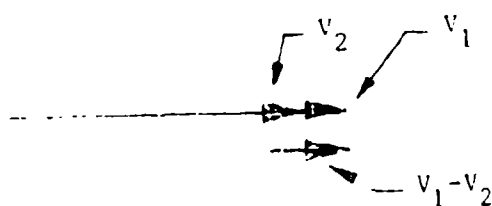
Phase Errors:
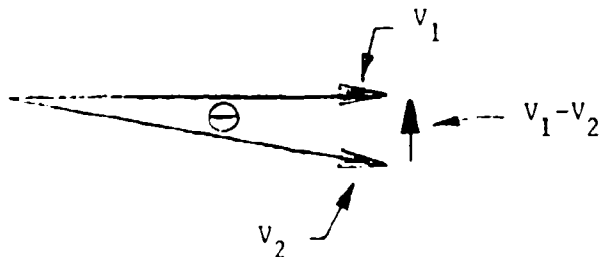
Figure 1.2.6-2

Vector Diagrams Showing Amplitude and

Phase Errors, with Primarily a Resistive Source

If Z_{th} and Z_{feed} are inductive:

Phase Error:
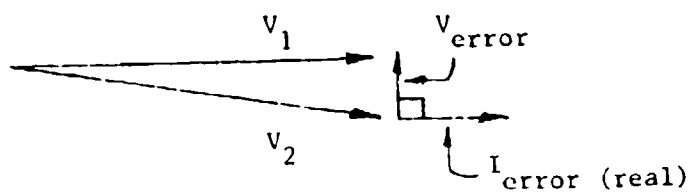
Amplitude Error:
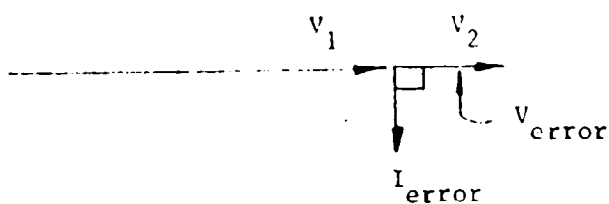
Figure 1.2.6-3

Vector Diagrams Showing Amplitude and

Phase Errors with a Primarily Inductive Source
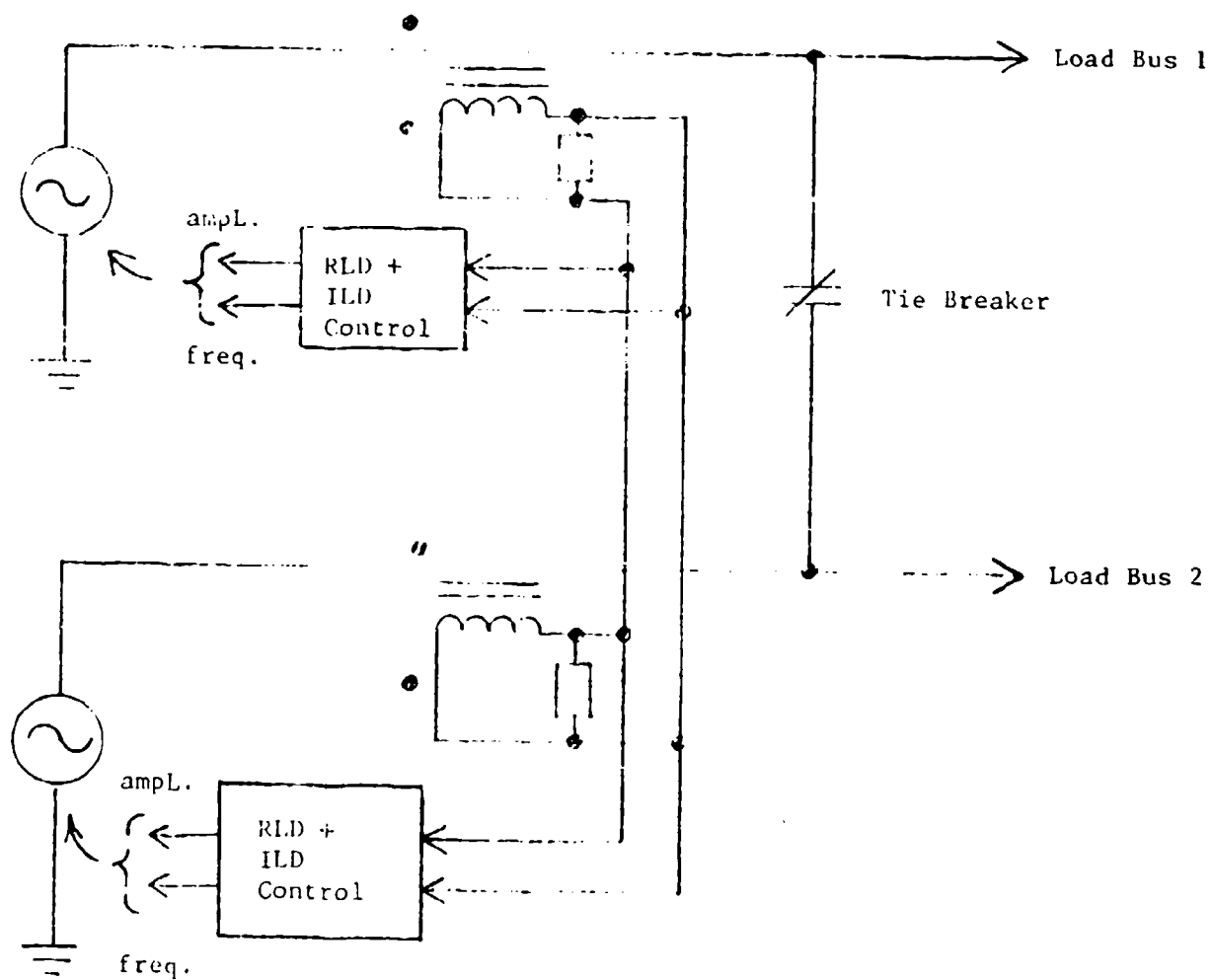
Figure 1.2.6-4

I_{error} Sensing and Control

(Any AC System)
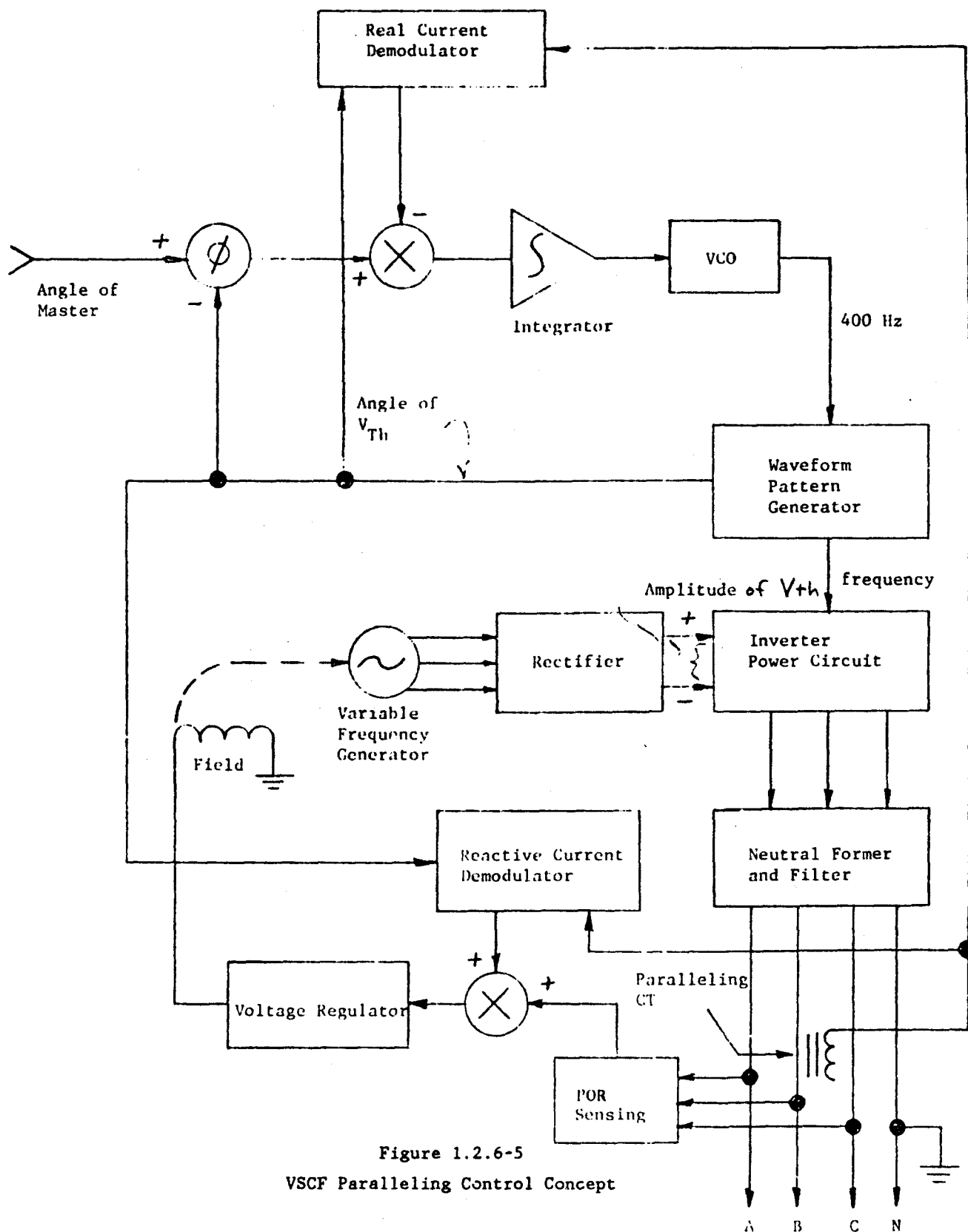
Figure 1.2.6-5

VSCF Paralleling Control Concept

1-146

2.0 THEORY OF OPERATION

2.1 Electric Power System

The system is designed to provide three types of electrical power from a single generator source. The outputs from each of the power conversion devices may be paralleled to provide up to four channels of power in parallel.

To accomplish this task, there are several line replaceable units that are required. A tabulation of the required units is provided in Table 2.1-1, along with their estimated weights (feeder weight is not included in the tabulation).

2.1.1 Generator

The generator is a three-stage machine, consisting of the main generator, a three-phase exciter with a rotating rectifier bridge, and a permanent magnet generator (PMG). The PMG is sized to provide the required power for the control and protection for each of the conversion devices as well as for the generator control unit (which provides generator exciter field power).

A single line diagram showing the basic system interfaces was shown in section 1.2.1 of this report. The following paragraphs provide a brief description of operation of the generator and its interface with the power conversion devices.

2.1.2 Generator Control Unit

The generator is controlled by the generator control unit (GCU). The logic for the GCU is depicted on drawing ED404324, Figure 2.1.2-1. Reference to this figure should be made for the following discussion.

Table 2.1-1 - Tabulation of the Required Line Replaceable Units,
with Estimated Unit Weights for Production per Channel

LRU	Estimated Weight	Dimensions
Generator	160	13.26D° x 16.50"L
Generator Control Unit	12	9.96 x 10.92 x 5.57
AC Power Conversion Unit	163	35.2 x 17.94 x 12.06
Inverter Control Unit	22	10.44 x 8.96 x 8.78
High Voltage DC Power Unit	400	19.00D x 33.00L
Low Voltage DC Power Unit	38	7 x 10 x 22
Load Breaker (400 Hz)	10	7.2 x 5.7 x 6.0
Bus Tie Breaker (400 Hz)	10	7.2 x 5.7 x 6.0
Generator Breaker (to AC unit) 2 per Channel	2 x 14	8.81 x 6.81 x 8.13
Generator Breaker (to HVDC unit' 2 per Channel	2 x 14	8.81 x 6.81 x 8.13
Generator Breaker (to LVDC unit)*	6	6.0 x 6.0 x 6.5
Current Transformer * 21 per Channel	21 x 1.0	3.0 x 3.0 x 2.0
Total Channel Weight	898	

* Estimated weight. All other weights are calculated.
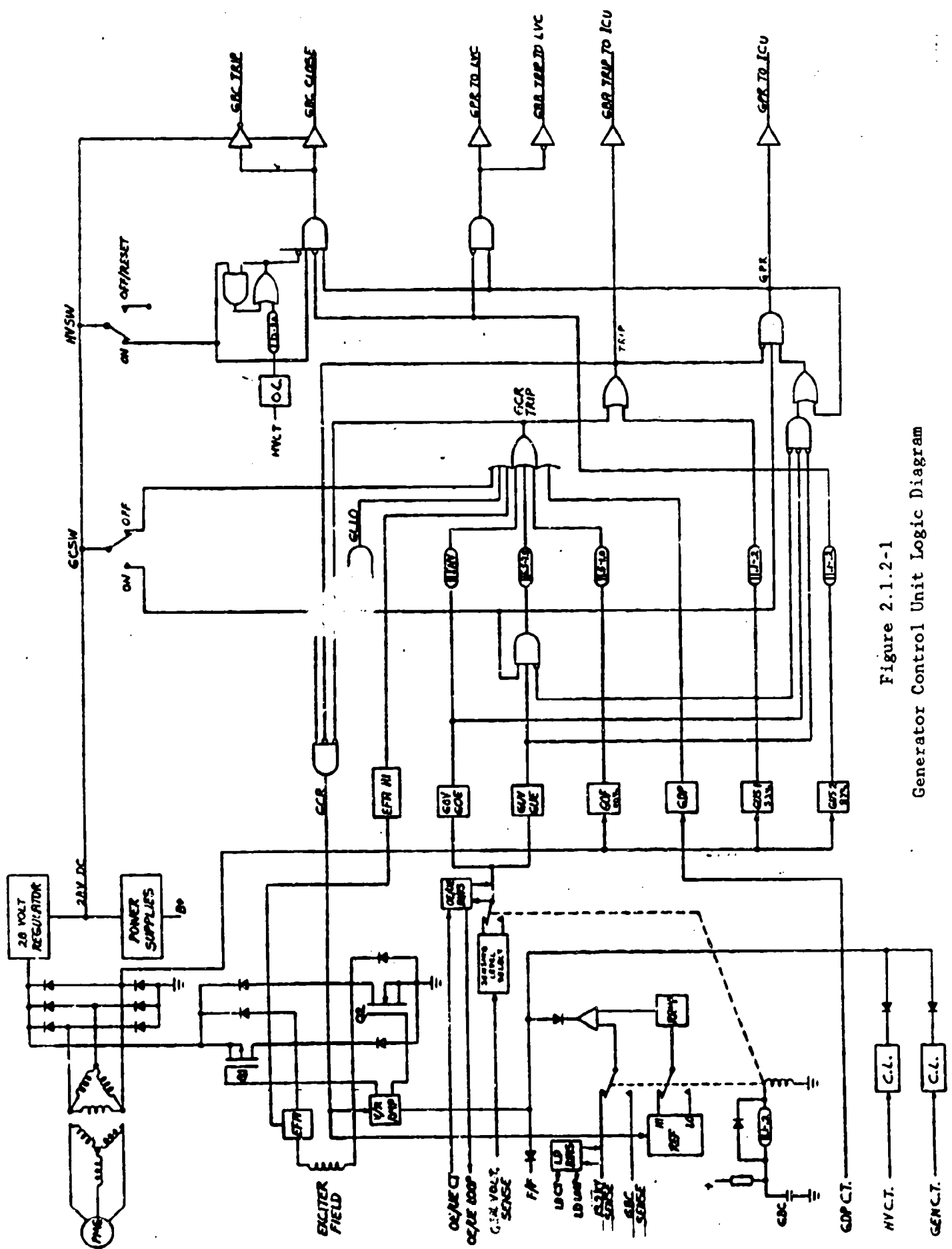
Figure 2.1.2-1

Generator Control Unit Logic Diagram

2.1.2.1   Generator Control Relay (GCR)

The GCR energizes the generator field circuit. It will close provided the
external generator control switch is in the ON position, there is not a GCR
trip signal and the generator is in its normal operating speed range (greater
than 53% speed).

2.1.2.2   System Power Ready

There are two Power Ready signals generated. The first occurs at the 53%
speed condition. Generator voltage is sensed and when voltage is normal (no
overvoltage and no undervoltage) with the generator in its normal operating
speed range, a Power Ready signal is latched, and stays on until either a trip
signal occurs or the generator control switch is moved to the OFF position.

This Power Ready signal is sent to the Inverter Control Unit (400 Hz AC
control).

The second Power Ready signal is energized when the generator speed reaches
83% (GUS 2). This Power Ready signal is sent to the Low Voltage Controller.
It is also used in conjunction with the High Voltage Switch to provide a close
voltage for the High Voltage Supply Contactors (GBCs). Loss of Power Ready or
setting the High Voltage Control Switch to OFF causes the GBC to trip.

2.1.2.3   Generator Voltage Regulator

As discussed earlier, the system is controlled by the GCR. The GCR allows the
regulator to perform its function controlling the system voltages in a
prescribed manner. The design is based on providing primary emphasis to the
HVDC power supply. Therefore, when this supply is ON, the regulator senses
and controls this output voltage. Control is transferred to the generator
output when the HVDC supply is not in operation.

2.1.2.3 Generator Voltage Regulator

The above is accomplished by sensing the GBC position. When this contactor is open, voltage is sensed at the generator side of the supply contactor, controlling generator output voltage. On closure of the GBC, the voltage reference level is changed and the sensed point is transferred to the HVDC output.

On closure of the GBC, a short time delay is initiated which allows the HVDC system to stabilize at the lower voltage. Then the reference is ramped up to the new operating level, thus minimizing overall transients on the system. When the reverse occurs, there is no delay in transfer, but the reference is ramped down.

A bias signal is provided to the voltage regulator for current limiting. This is an override of the voltage control and may come from either the HVDC supply or from generator overcurrent.

2.1.2.4 Generator System Protection

The GCU provides system protection. In the event of a protective function trip, the GCR trips and the Power Ready signals are removed. Manual action via the Generator Control Switch is required to reset the system.

As the generator system may operate at either a low voltage, from 53% to 83% speed, or a high voltage, from 83% to 110% speed, the generator overvoltage and generator undervoltage trip levels are also switched at the same time as the voltage reference level is changed.

The following paragraphs provide further information on each of the protective functions.

2.1.2.4.1 Overvoltage Protection

The generator output voltage is sensed at the generator point of regulation. If the overvoltage trip level is exceeded, an inverse time delay is activated, which trips the GCR if it times out. Once tripped, manual reset is required.

2-5

2.1.2.4.2   Generator Undervoltage Protection

A fixed time delay is initiated for generator undervoltage conditions. Time
out of this time delay causes the GCR to trip. Manual reset is required once
a trip occurs. Generator undervoltage is locked out by generator underspeed
(53%) and generator control switch set to OFF.

2.1.2.4.3   Generator Overfrequency

In the event of a generator overspeed, a fixed time delay is initiated that
trips the GCR. Manual reset is required once the GCR is tripped.

2.1.2.4.4   Generator Differential Protection

Current transformers sense generator phase currents relative to total phase
currents delivered to the conversion units. Any differences are an indication
of feeder or generator faults. A sensed fault results in a GCR trip. Manual
reset is required if a trip occurs.

1.2.2.4.5   Exciter Field Amps High

The exciter field current is sensed. If it exceeds specified levels, the GCR
is tripped.

2.1.2.4.6   Generator Underspeed

Generator speed is sensed by sensing PMG frequency. Two underspeed levels are
sensed: 83% speed and 53% speed.

On start-up when the 53% speed is reached, the GCR closes and the system
voltage builds up. On shutdown, when engine speed goes below 53%, the system
is de-energized and the system contactors are tripped after a short time delay.

The second generator underspeed controls the signals and contactor voltages
associated with operation of the HVDC supply and the 28-volt dc supply. This
underspeed circuit operates at the 83% speed condition.

2.1.2.4.7   Overcurrent

Current limiting is implemented in the voltage regulation system. However, to
provide for compatible operation of the HVDC system with respect to the other
supplies, an overcurrent protection function is implemented in the GCU for the
HVDC supply.

The time delay for overcurrent is shorter than the generator undervoltage time
delay. The sense level for overcurrent also is slightly less than the current
limiting level for the HVDC supply. After the time delay the contactor to the
HVDC system trips.

This scheme provides for compatible operation of overloads or short circuits
imposed on the generator system by the HVDC system.

2.1.2.4.8   Parallel System Protection

The parallel system protection is compatible with the parallel system
control. Concepts developed for system control are considered in the design
of the system protection.

The system is designed to include the HVDC system in the generator closed loop
control loop whenever the HVDC power system is in operation. The excitation
to the generator is therefore also controlled to maintain equal load division
on the HVDC power supplies when they are paralleled. As such, the protection
provided for parallel operation is based on the same principle.

Overexcitation/underexcitation signals are generated based on the combination
of generator output sensed voltage and the difference currents delivered to
the HVDC power supplies.

The preliminary design results in tripping of the generator as a direct result
of an excitation fault. This approach seems most reasonable, as it is
probable that control failure, which results in an overexcitation or
underexcitation condition, would be in the regulation system, not in the sense
point for control. Thus, the overall system disturbance is minimized.

2-7

2.1.2.5   System 400 Hz Feedback

A feedback signal is provided to the generator voltage regulator from the
Inverter Control Unit. The purpose of this feedback signal is to provide a
momentary voltage regulator cut-off signal for some types of failures in the
400 Hz system.

Analysis of the 400 Hz system indicated a feedback signal was desirable to
prevent catastrophic failure of the conversion equipment for these
predetermined faults in the system.

2.1.3   High Voltage DC System

The HVDC system consists of a transformer rectifier that converts generator
output power to 13.2 kv dc power. The system includes an output filter that
assures that the ripple amplitude will be within the limits of 0.26 kv.

The control and protection of this system is provided by the primary
protection system.

2.1.4   Conversion to 400 Hz AC

The 400-Hz ac conversion unit operates as a utilization equipment load on the
generator system.

The 400-Hz system consists of the Inverter Control Unit and the ac Power
Conversion Unit.

2.1.4.1   AC Power Conversion Unit

The ac power conversion unit converts the variable frequency input power from
the generator to constant voltage, constant frequency, 400 Hz output power.
The unit operates over a variable input voltage range to accommodate the
capabilities of the generator over its speed range.

2.1.4.1   AC Power Conversion Unit   (Continued)

The ac power conversion unit is controlled by the preregulator controls and
the inverter control unit. The preregulator controls the dc-link SCR bridge
to maintain a constant regulated 400-Hz ac output voltage. The inverter
control unit controls the switching of the power transistors in the inverter
stage to provide a controlled constant frequency output.

2.1.4.1 1   System Control

The logic for the 400-Hz ac system controls is depicted on drawing 949F229,
Figure 2.1.4-1. The system is controlled by a three-position switch. This
switch has a test position (momentary), an ON position, and a center OFF/RESET
position.

Control power for the ac power conversion unit is derived from the PMG through
transformer rectifier units.

Figure 2.1.4-1 shows the power supplies for the 400 Hz system. Refer to this
logic diagram in the following paragraphs on 400 Hz system controls.

2.1.4.1.2   Input Power Ready

There are two interface criteria that must be satisfied for the controls to
allow unit operation. They are a lack of a trip signal from the GCU and the
input voltage must be above the undervoltage sensed level.

2.1.4.1.3   Input Breaker/Load Breaker Control

The input breaker (GBA) closes if the generator power is ready, the 400 Hz
control switch is in the ON or TEST position, and there is not a sensed fault
in the system.

Figure 2.1.4-1

Logic Diagram for the 400-Hz-AC Conversion Unit

2.1.4.1.3   Input Breaker/Load Breaker Control   (Continued)

Once closed, the 400-Hz system goes through a programmed start-up. Once 400
Hz power ready conditions are sensed, the load breaker (LB) closes if the
control switch is in the ON position. If the control switch is in the TEST
position, the load breaker does not close.

2.1.4.1.4   Protective Functions

The protective functions sense faults on the output as well as the input to
the ac power conversion unit. The protective functions are presented below.
Greater detail is provided in paragraph 2.3.

Input Sensing

The following protective features sense faults at the input:

1.   Input Differential Current
2.   Input Overcurrent
3.   Input Undervoltage

Output Sensing

The 400 Hz system voltage is sensed at the POR (Point-of-Regulation). This
voltage is used for:

1.   Overvoltge Protection
2.   Undervoltage Protection
3.   Abnormal Frequency

The voltage at the inverter output terminals is used for sensing:

1.   Extraneous Frequency
2.   Direct Current Content

2.1.4.1.4   Protective Functions   (Continued)

The terminal voltage is used for this sensing to provide for selective
tripping of paralleled systems.

Added Protection

In addition, the following protection functions are provided:

1. Output Feeder Fault   3. Link Overvoltage
2. Inverter Fault Protection   4. Sustained Link Clamp

Each of the protective functions operates through its associated time delay.

2.1.5   System Power Ready

The following pertinent system parameters are sensed to determine that power
quality is within acceptable limits.

1. Input Undervoltage   4. Output Undervoltage
2. Abnormal Frequency   5. Output Extraneous Frequency
3. Output Overvoltage   6. Output DC Content

Once all of the above parameters are satisfied, a Power Ready signal is
generated after a short time delay. This allows the LB to close if the
control switch is in the ON position.

2.2   Generator

2.2.1   Electrical Discussion

2.2.1.1   Description of Operation

The generator is a brushless machine. The main machine is a salient pole generator with rotating poles. DC excitation power is supplied to the rotating field through the use of a rotating rectifier and a small ac generator (exciter). See Figures 2.2.1.1-1 and 2.2.1.1-2.

The exciter is also a salient pole machine, with the poles inside the three-phase ac winding structure (wound stack). The exciter ac wound stack is mounted inside the main generator shaft and rotates with it. The exciter poles are mounted on a stationary shaft. The regulator then supplies dc power to the exciter field (pins D-E of Figure 2.2.1.1-2).

A Permanent Magnet Generator is also available in the machine. This supplies three-phase ac power on the stationary shaft. The PMG uses samarium cobalt magnet poles. Power from the PMG is available for controls and the regulator.

2.2.1.2   Rating, Schematic, Weight, Outline and Efficiency

The generator has a variable rating over a wide speed range (53% to 110% speed). The voltage rating varies with speed so that the machine is fully rated as regards voltage capacity over the speed range. See Table 2.2.1-1

The generator rating is based on evaluation of the total system requirements with consideration given to non-linear loads.

          Schematic - See Figure 2.2.1.1-2
          Weight - See Table 2.2.1-2
          Outline - See Figure 2.2.1.1-3
          Efficiency - See Table 2.2.1-3 for a summary of efficiency
          calculations. These calculations are based at the 83% and 110% speed
          points at the maximum steady-state loads.
          PMG - See Figure 2.2.1.1.4 for Characteristics

2-13

Table 2.2.1-1
Generator Rating
P/N 977J333-1

Loading	Steady State				5 Second Overload			
Speed (%)	53	60	83	110	53	60	83	110
Speed, RPM	7,227	8,182	11,318	15,000	7,227	8,182	11,318	15,000
Frequency	1,205	1,364	1,886	2,500	1,205	1,364	1,886	2,500
kVA	79	161	532	532	119	247	657	657
Volts/Phase	143	146	245	245	144	149	245	245
Amps/Phase	92	184	362	362	138	276	447	447
Phases	6	6	6	6	6	6	6	6
Power Factor	.86	.86	.79	.79	.85	.86	.73	.73
Rot. Fld. Amps AFA	34.6	39.7	73.6	60	39.5	50.4	88	72
Rot. Fld. Res. Rf 260°C	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Exciter Field Amp. EFA	2.4	2.5	4.0	2.9	2.7	3.2	4.8	3.5
Exciter Res. Hot Ohm/80°C	19.1	19.1	19.1	19.1	19.1	19.1	19.1	19.1
Exciter Fld. V., EFV	46	48	76	55	52	61	92	67
Exciter Fld. Watts	110	119	306	160	139	196	440	234

1. Speed Range: 7,227/15,000 RPM
2. Overspeed: 15,750
3. Rating: See Table above
4. Cooling: Conduction and Oil spray
   Oil Spray Flow: 4 GPM (for end extensions and rotor winding.)
   Total Oil Flow: 12 GPM
   Pressure: 30 Psig
   Oil Temperature In (Assumed):   120°C
5. Altitude: Sea Level to 65,000 (Generator interior
                                    pressurized at 7 PSIA
                                    Minimum for corona purposes.)
6. Life (Assumed):   5,000 Hours
7. Bearings: Oil Lubricated
8. Type of Design: Brushless
9. PM Generator: See Figure 2.2.1.1-2
10. Waveform*:   Line-Line at No Load:
                                    Maximum = 4%, 5th (Calculated)
11. Phases: Two 3-Phase Windings displaced 30°.

* Note: Waveform when loaded is adversely affected by non-linear loading.

Table 2.2.1-2
Weight Breakdown (Calculated)

	Computer Calc. Weight, lbs
Main Stator	23.22
Main Rotor Steel	46.65
Main Rotor Wire Bare	9.04
Main Stator Wire Bare	11.00
	89.91
Exciter Field Wire	1.43
Exciter Armature Wire	1.15
Exciter Pole Steel	3.28
Exciter Armature Steel	2.20
	8.06
PM Generator (Rotor) Pole Structure	2.14
PM Generator (Stator) Armature	1.10
	3.24
Total Electrical Weight	101.2
Total Mechanical Weight	58.8
Total Weight	160.0

* Steel weight is weight of punchings.

Table 2.2.1-3
Efficiency (Calculated)

PHASES 6 (30° displaced)	kVA	532	532
	Volt/Phase	245	245
	Amp/Phase	362	362
	PF	.79	.79
	RPM	11,318	15,000
Main Generator			
Copper Losses, Watts			
AC Winding 260°C		10,417	12,085
Field Winding 260°C		11,766	7,710
Iron Losses, Watts			
Core* (Actual/Epstein = 2.2 Hip 27 .006 TK		9,084	8,267
Pole Face		603	491
Rotating Rectifier (2.2 X AFA), Watts		162	132
Windage, Watts			
Air		1,477	3,323
Spray Oil (3 GPM)		4,701	8,256
Exciter Losses, Watts		1,985	1,752
PM Generator (Estimated), Losses, Watts		426	589
Stray (3%), Watts		1,477	1,886
Total Losses, Watts		42,098	44,491
Output, Watts		?,391	420,391
% Efficiency		90.9	90.4

Figure 2.2.1.1-1
Generator Layout

2-16

LAYOUT OF 540 KVA
GENERATOR

EP395792

SECTION C-C
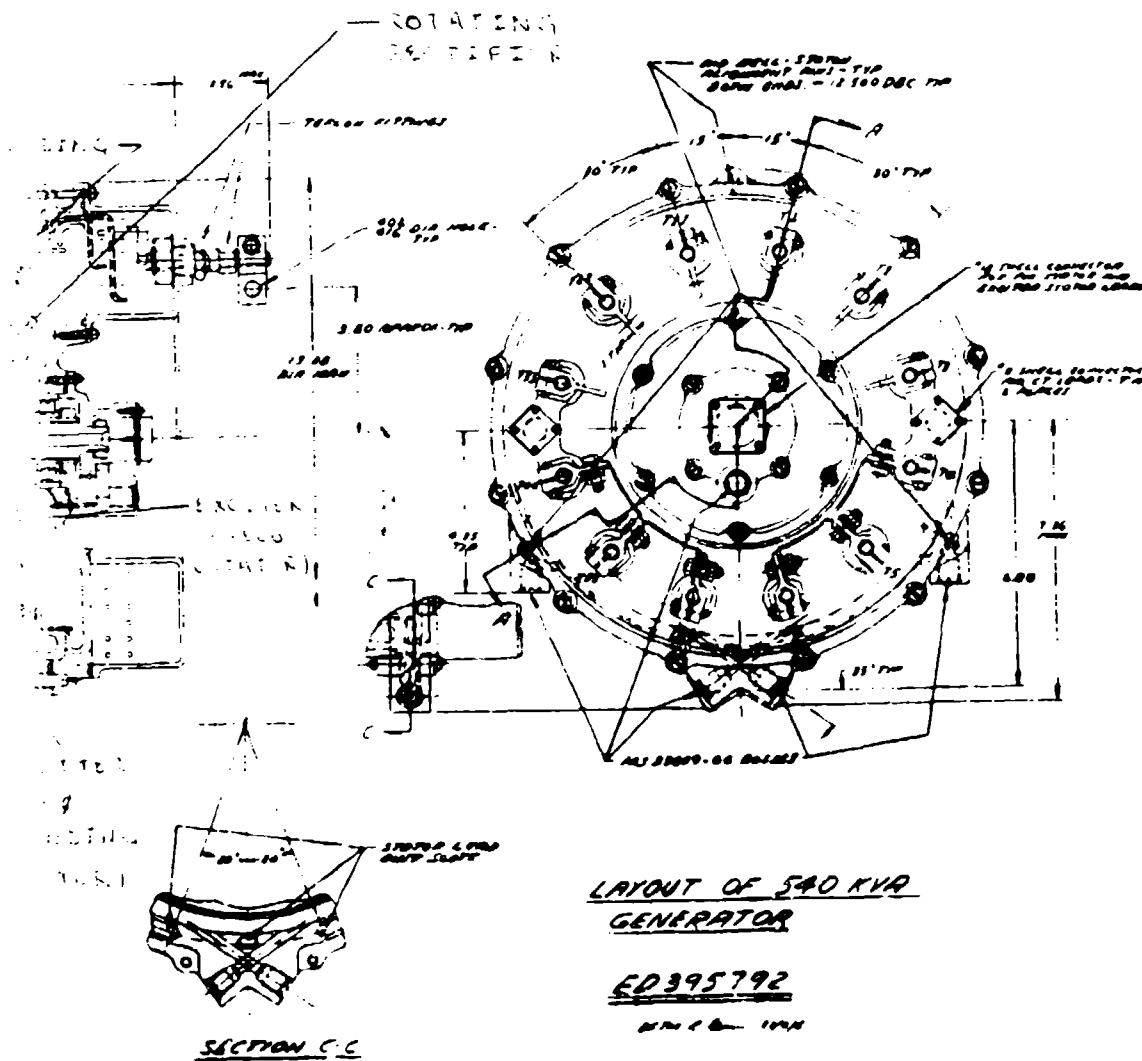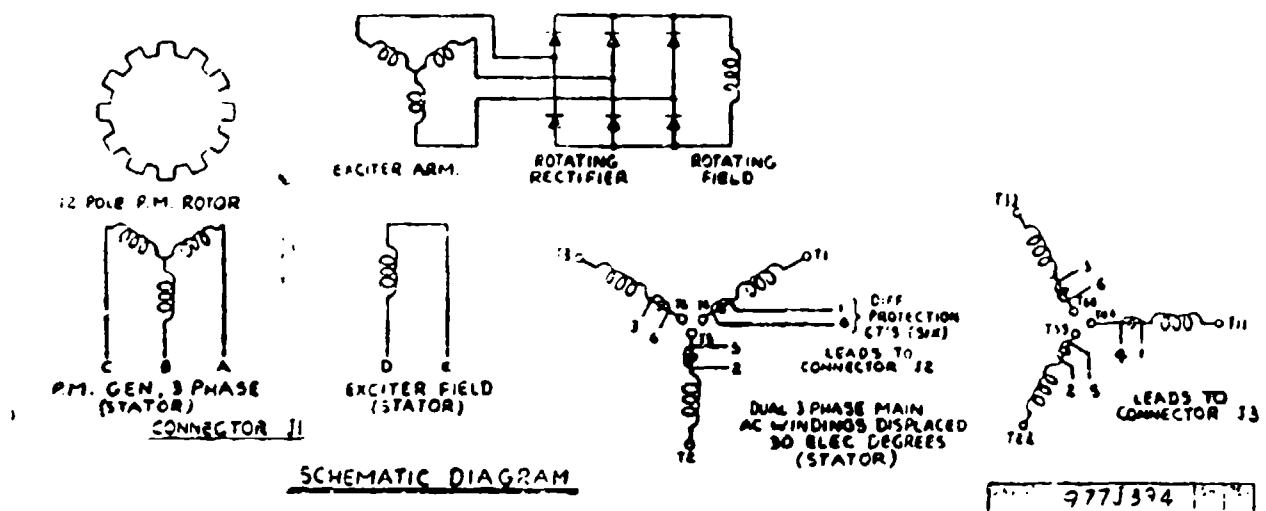
SCHEMATIC DIAGRAM

Figure 2.2.1.1-2

Schematic Diagram

2-18
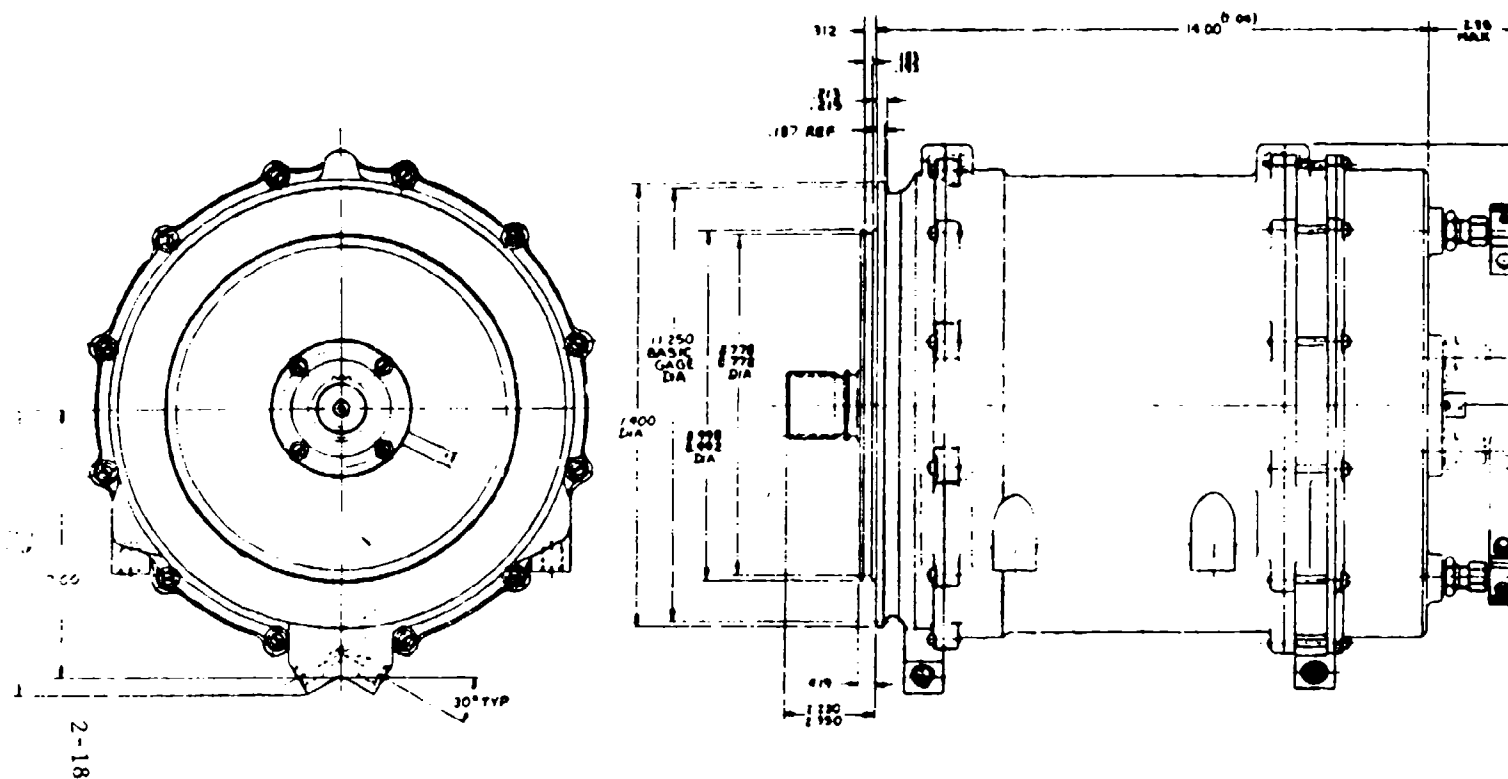
Figure 2.2.1.1-3
Generator P/N 977J333-1
Outline Reference: 977J394-1
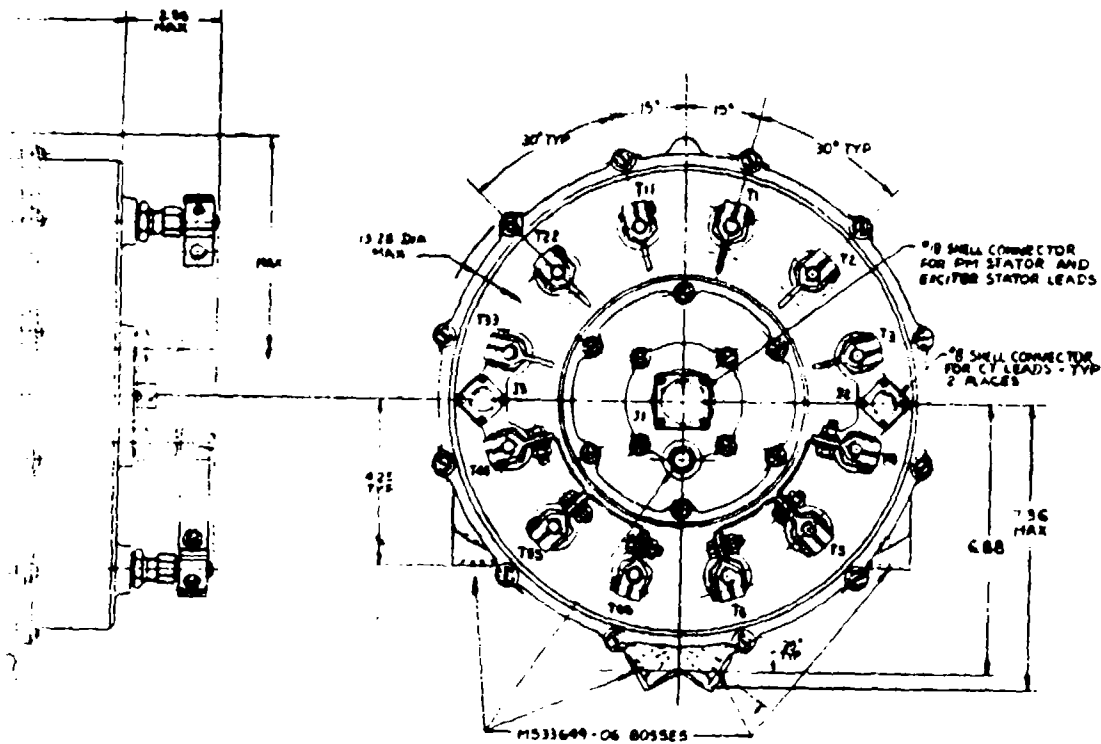
OUTLINE
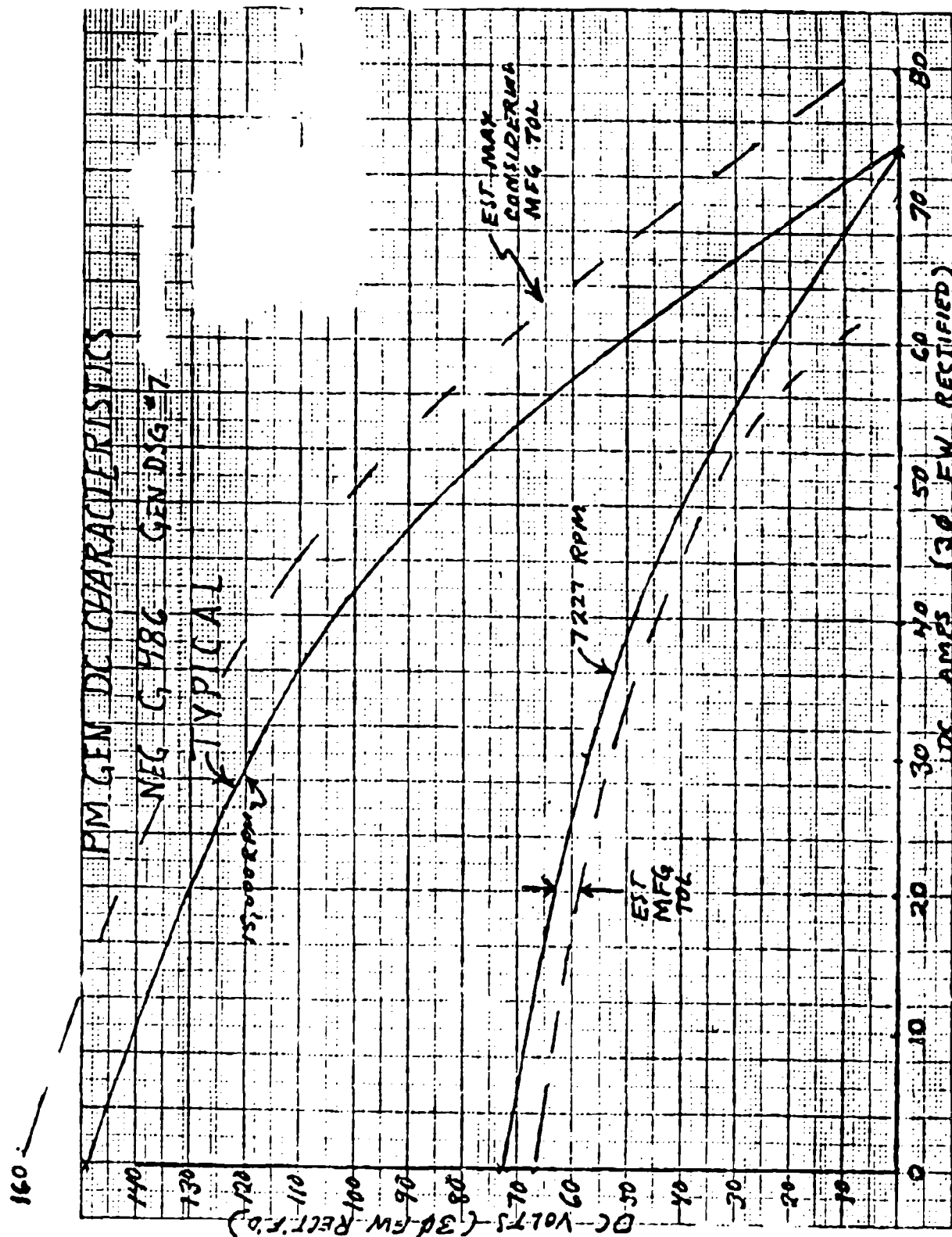
Figure 2.2.1.1-4

PM Generator DC Characteristics

2.2.2   Thermal Discussion

2.2.2.1   Shared-Oil Configuration

The generator cooling system is configured for "shared-oil operation" as illustrated in Figure 2.2.2-1. This subsystem requires 12 GPM of MIL-L-7808 oil at a temperature equal to or less than 120°C from the cooling system. The oil subsequently divides at point A into two circuits.

The first circuit of 8 GPM passes through the coolant jacket which is around the stator. Positive circulation of this oil is maintained by a constant displacement pump (B). A filter (C) on the return side of this loop precludes contamination of the shared-oil system from the generator. The second circuit receives oil by way of a pressure control valve (D), which maintains a supply pressure of 30 psig above the pressure within the rotor compartment.

Internal metering orifices within the rotor flow circuit produce the 4 GPM flow required for spray-cooling of rotor components. When this oil leaves the exit ports it appears as a mixture of air and oil. A scavenge pump (E) with a capacity greater than the supply rate of solid oil is required to keep the air gaps between the rotor and stator clear of oil. This mixture is delivered to sump (F), which is equipped with an air/oil separator (G). Air from the separator is discharged into the generator and the oil from the sump is removed by a scavenge pump (H) and returned to the system by way of filter (I) and check valve (J). A solid-state oil level sensor (K) is used to switch the electrical power for pump (H) and control the amount of oil in the sump.

2.2.2.2   Thermal Conditions

The most severe thermal conditions from the standpoint of cooling the generator, occur between 83% and 110% speed with an output of 532 kVA at a .79 power factor. The losses in the generator for these conditions are defined in Table 2.2.2-1. These heat loads are illustrated schematically in Figures 2.2.2-2 and 2.2.2-3. The most severe condition for the rotor occurs at 532 kVA at .79 power factor at 11,318 rpm. An average temperature of 190°C is calculated for the copper in the field winding. The resulting maximum temperature in the center of the winding is about 260°C. The most severe thermal conditions for the stator occurs at full load at 15,000 rpm. An average temperature of 205°C is calculated for the copper conductors. The resulting end turn temperature is about 245°C.
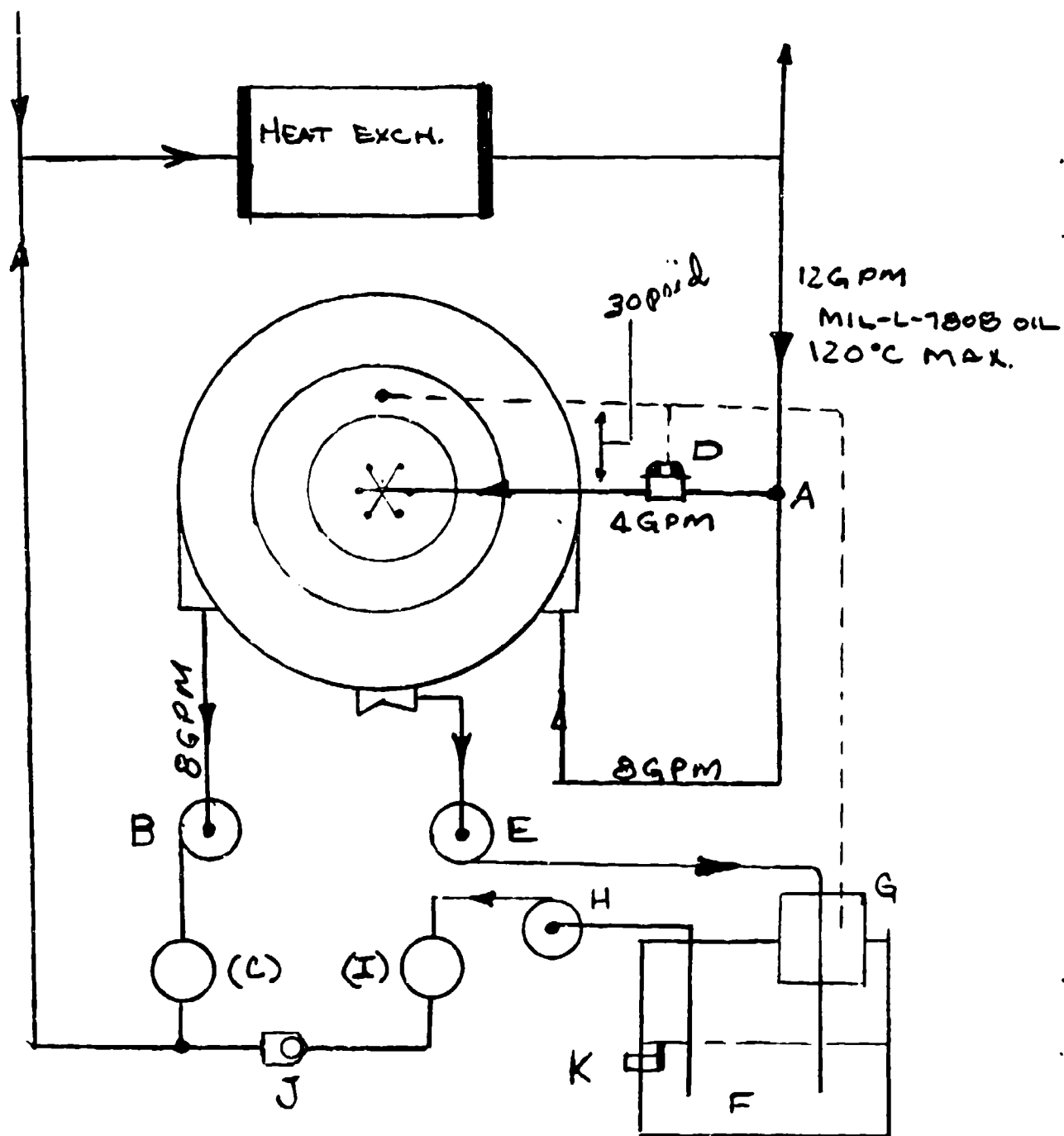
Figure 2.2.2-1

Schematic of Generator Cooling System

Table 2.2.2-1 - Heat Load Losses of Generator
(See Figure 2.2.2-2 and -3).

Loca-tion	Source	Heat Sink
1.	Copper and Iron Losses in Stator	Cooling jacket around stator.
2.	Windage Losses in Air Gap	50% into cooling jacket ; 14.4% into oil in hollow shaft; 35.6% into oil spray on the ends of the rotor.
3.	Windage Losses on Ends of Rotor	Oil spray on the ends of the rotor.
4.	Copper and Pole Face Losses for the Rotating Field	28.8 into oil in hollow shaft; 71.2 into oil spray on the ends of the rotor.
5.	Copper and Iron Losses for Rotating Armature of the Exciter Generator	Oil spray on the ends of the winding from sationary locations.
6.	Copper and Pole Face Losses in Stationary Field for Exciter Generator	Oil within stationary central shaft.
7.	Copper Losses in Stator for Permanent Generator	Oil spray from a rotating sleeve under one end of the winding.
8.	Losses in Rotating Rectifier Assembly	Oil spray onto assembly from stationary locations.
9.	Windage Losses Inside of the Hollow Shaft	Oil within the hollow shaft.
10.	Oil Churning Losses	Oil from rotor.
11.	Stray Losses	Oil from rotor.
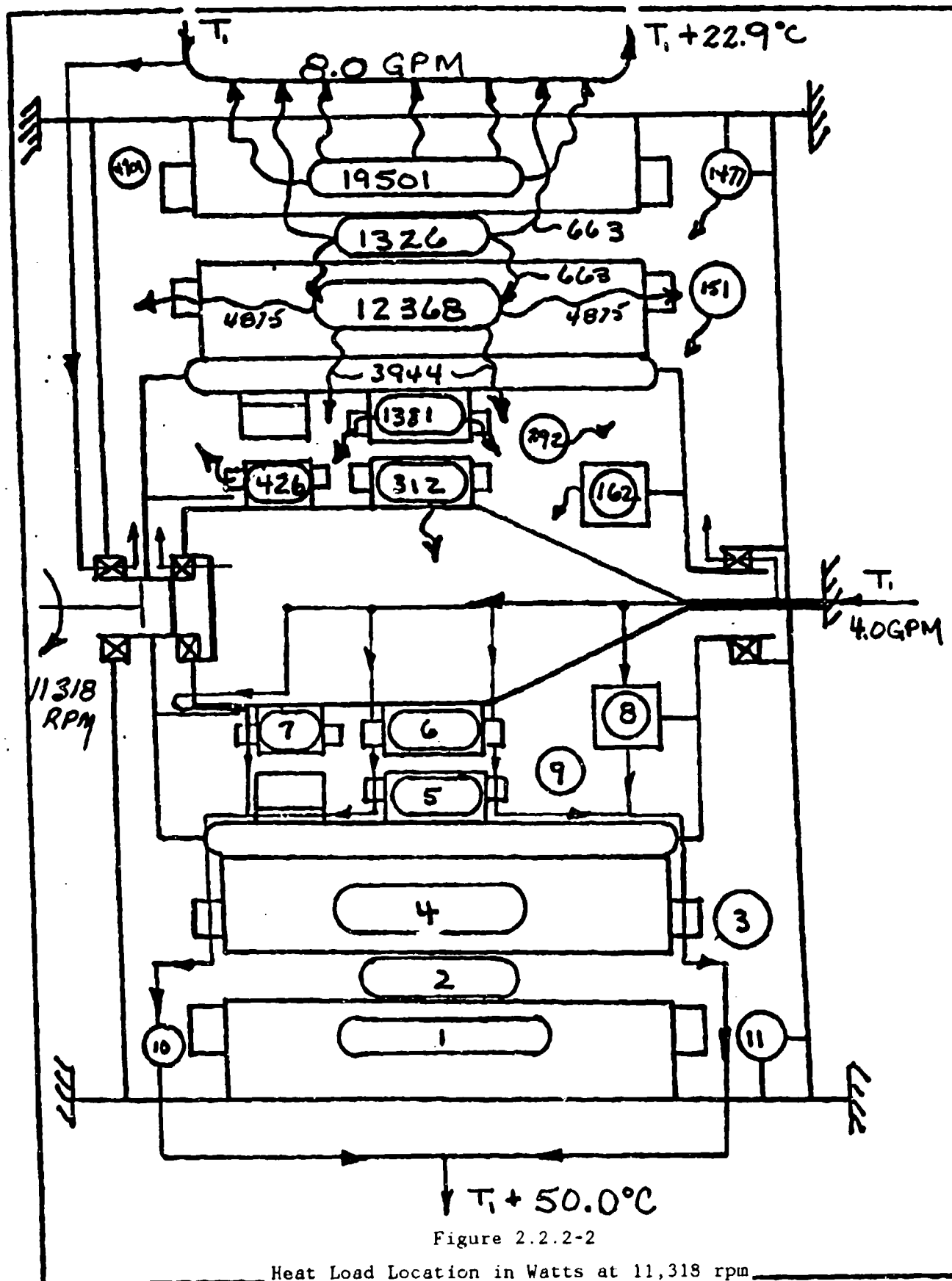
Figure 2.2.2-2

Heat Load Location in Watts at 11,318 rpm
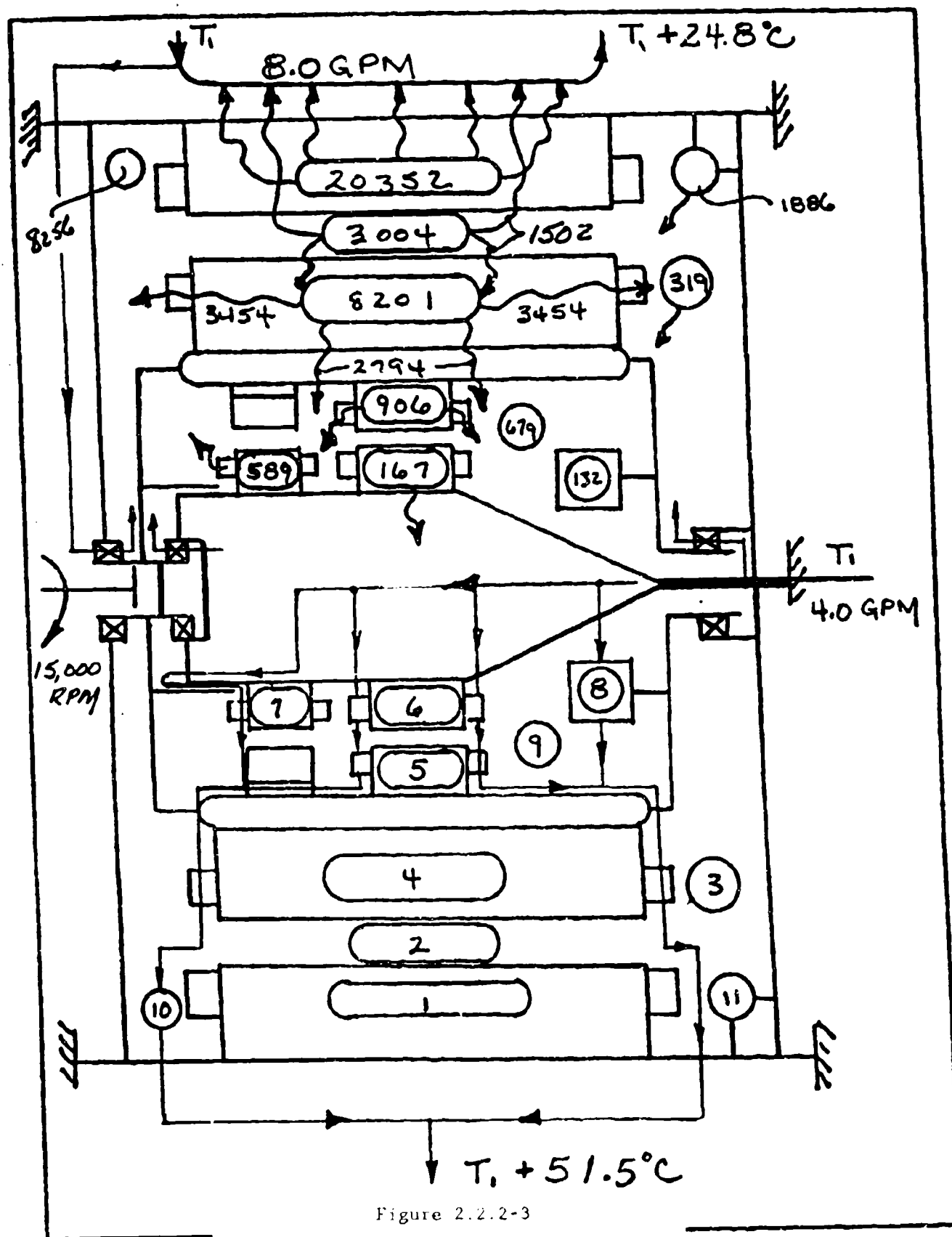
Figure 2.2.2-3

Heat Load Location in Watts at 15,000 rpm

2.2.3   Vibration

2.2.3.1   Introduction

The generator has a rotor weight of 82.6 pounds and a bearing span of 9.24 inches. The operating speeds are between 7,227 and 15,000 rpm with an overspeed capability of 15,750 rpm. Within the constraints of the electrical configuration, the shaft has a greater stiffness than the rotor support system. Thus, the undamped critical speeds depend significantly on the stiffness of the supports. A support includes a rolling contact bearing and its bracket. A practical support stiffness is in the range of 1×10^5 to 3×10^5 lbs/in., which yields a critical speed within the operating range of this generator. Safe operation of an undamped system at a critical speed with practical unbalance limits is not considered feasible. Therefore, viscous damping of the system is used.

2.2.3.2   Squeeze Film Damping

Satisfactory vibration performance is obtained by the introduction of a simple oil-filled clearance between the outer member of the rolling contact bearings and their supports as illustrated in Figure 2.2.3-1.

For short annular clearances the damping constants B_V and the spring constant B_H for orbiting motion are:

$$B_V = 2B_V' \frac{\mu D}{8C^3} L^3$$

$$B_H = 2B_H' \frac{\mu D}{8C^3} L^3$$

OIL SUPPLY GROOVE

R

L

L

D

$W = .6299$ IN
$D = 2.4409$ IN
$L = .250$ IN
$R = .039$ IN
$G = .090$ IN
$C = .00267$ IN

SQUEEZE FILM

G

W

C

$$L = \frac{W - R - G}{2}$$
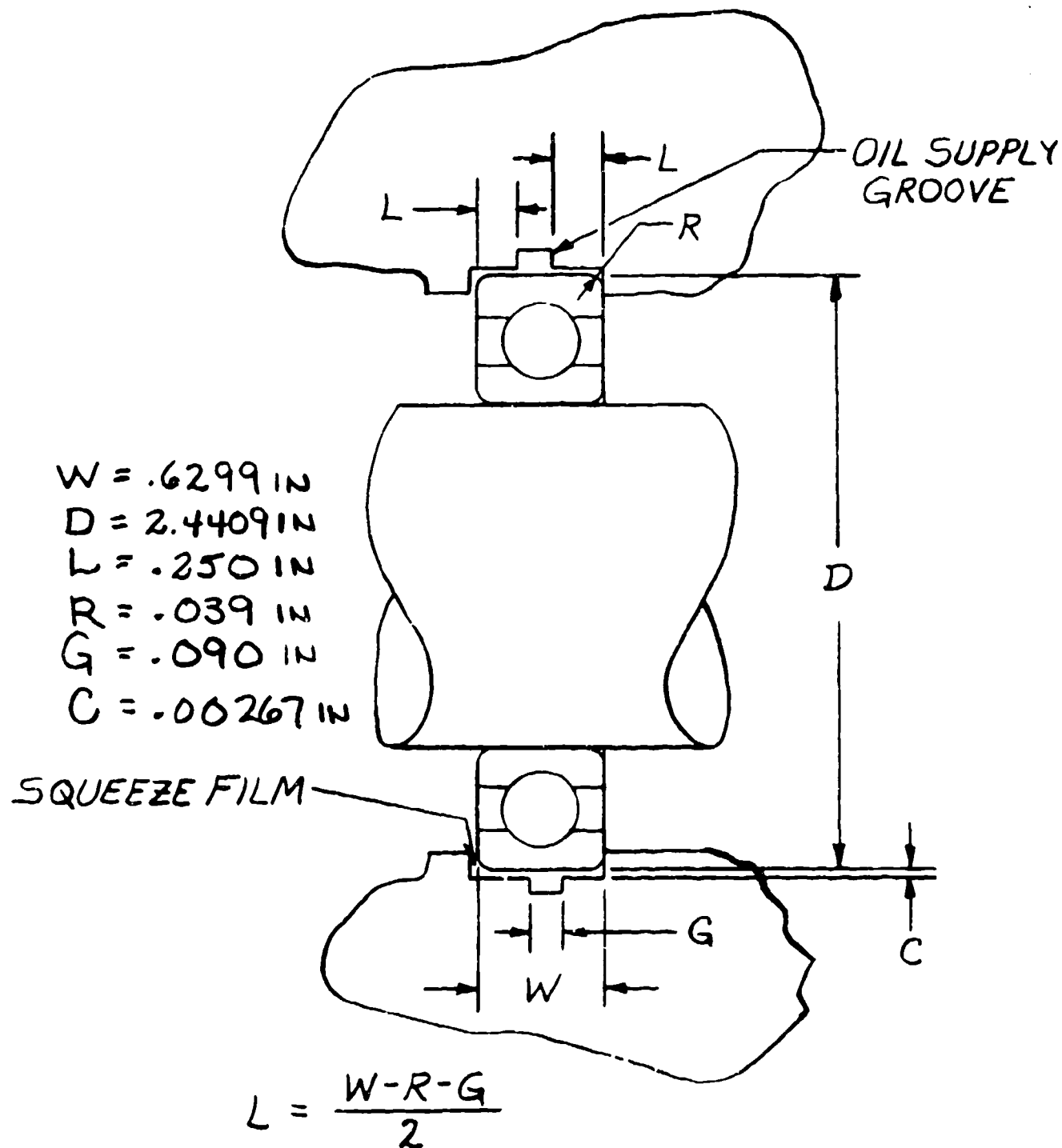
Figure 2.2.3-1
Squeeze Film Damping

2-27

2.2.3.2   Squeeze Film Damping   (Continued)

where: μ =   viscosity of the oil (lbs-sec/in^2)
         D   =   diameter at the clearance annulus (in.)
         L   =   axial length of clearance on each side
                   of the supply groove (in.)
         C   =   radial clearance

         $\dot{B}_V$

         and

         B_H' =   factors which depend on the ratio
                       of the relative displacement δ
                       between the clearance boundaries to the
                       radial clearance "C" as shown in Figure
                       2.2.3-2.

    B_V =   Damping constant acting normal to the displacement within
              the clearance, lb-sec/in.

    B_H =   Spring constant acting parallel to the displacement
              within the clearance, lb-sec/in.

The instantaneous forces generated by the orbiting motion are:

    F_N = B_V δW (includes both sides of oil groove)
    F_P^N = B_H^V δW (includes both sides of oil groove)

Where δ =   Displacement within the oil film (in.)
         W   =   Orbiting rate (radians/sec)
         F_N =   Force acting normal to the film displacement (lbs.)
         F_P^N =   Force acting parallel to the film displacement (lbs.)

2-28

2.2.3.3   Damping Constant

The damping constant for a MIL-L-7808C oil film at 100°C around a 206 size
bearing with a 0.09 inch-wide oil supply groove is given in Figure 2.2.3-3 as
a function of the radial clearance. It should be noted from Figure 2.2.3-2
that damping constant and the stiffness of the oil film are weak functions of
the ratio of the displacement and the clearance. A value of S/C = 0.5 was
used for Figure 2.2.3-3. The impact of radial clearance is shown in Figure
2.2.3-4. However, the damping constant and stiffness are strong functions of
the oil viscosity or the temperature of the oil within the clearance. Table
2.2.3-1 shows the impact of temperature on the viscosity of MIL-L-7808C oil.
Also, the instantaneous temperature of the damper has impact upon clearance
between the boundaries. For these reasons, a steel insert is used in each of
the ring brackets to minimize the expansion or contraction of the clearance.

2.2.3.4   Damped Rotor System

The damped rotor system used in the calculations is shown schematically in
Figure 2.2.3-5. The parallel spring damper separates the oil-filled clearance
between the outer member of a rolling contact bearing. The spring in series
with the parallel spring damper represents the bearing and its bracket. The
equivalent rotor unbalance has been calculated using this figure. The value
is .082 inch/lbs.

Figure 2.2.3-6 shows the vibration magnifications as a function of the damping
constant. The vibration responses are given for 7,000 and 15,000 rpm and for
a critical speed that occurred within a range of damping constant from 40 to
1000 lb-sec/in. The magnification factor is based upon the ratio of the
amplitude vibration and the amount of concentricity (E) of the rotor mass used
to drive the vibration.

Where $E = \dfrac{\text{in-lbs (unbalance)}}{\text{weight of the rotor}}$

$E = \dfrac{.082 \text{ in-lbs}}{82 \text{ lbs}} = .001$ in.

Table 2.2.3-1
Temperature Impact on Viscosity of MIL-L-7808C Oil

Temperature °C °C	Oil Viscosity Lb-Sec/In.^{2}
-30	500 X 10^{-7}
0	60 X 10^{-7}
22	23 X 10^{-7}
100	3 X 10^{-7}
120	2.2 X 10^{-7}
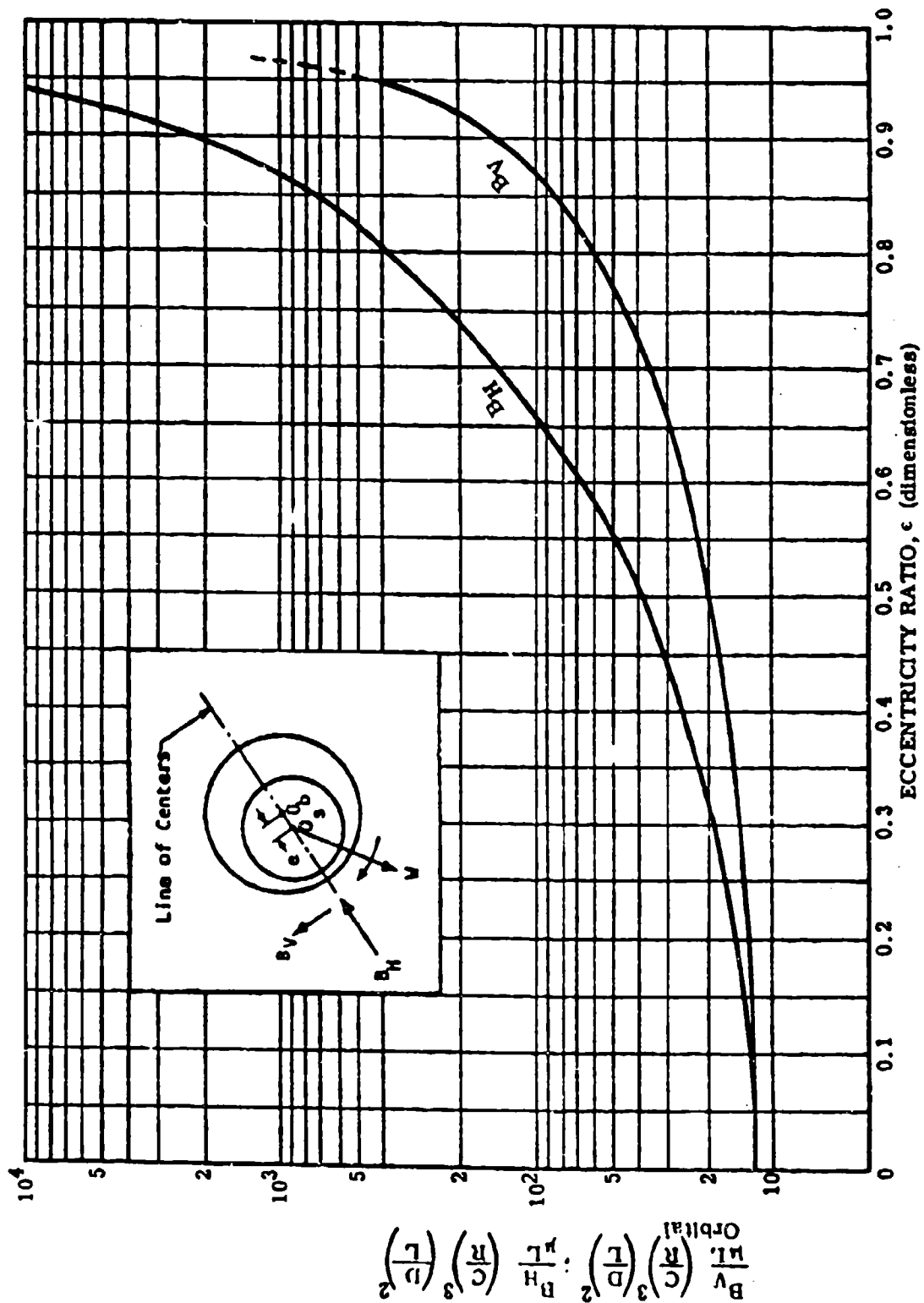
Figure 2.2.3-2

Chart for Determining Instantaneous Damping Constants
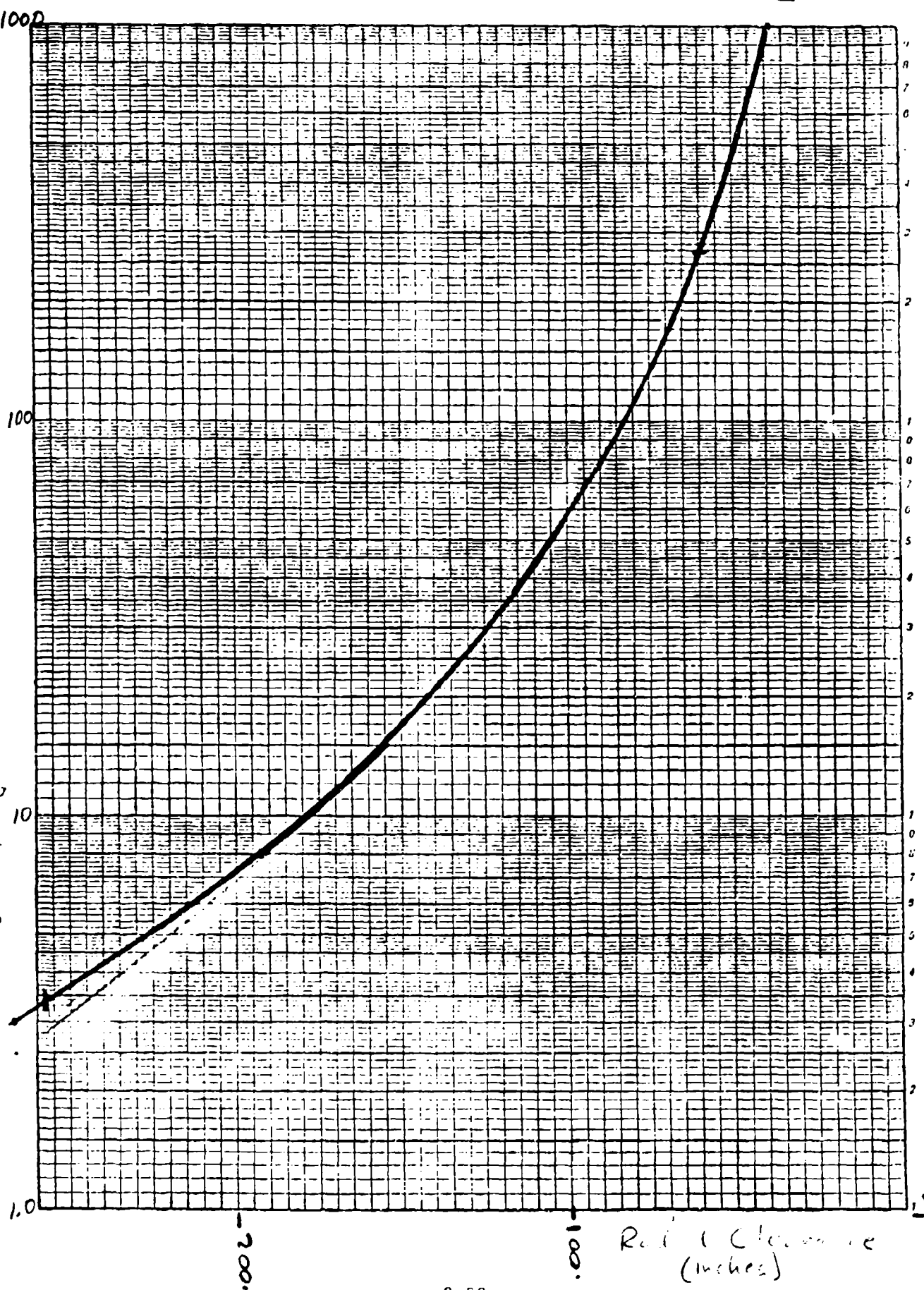
Figure 2.2.3-3

Radial Clearance Versus Damping Constant for a 206 Bearing
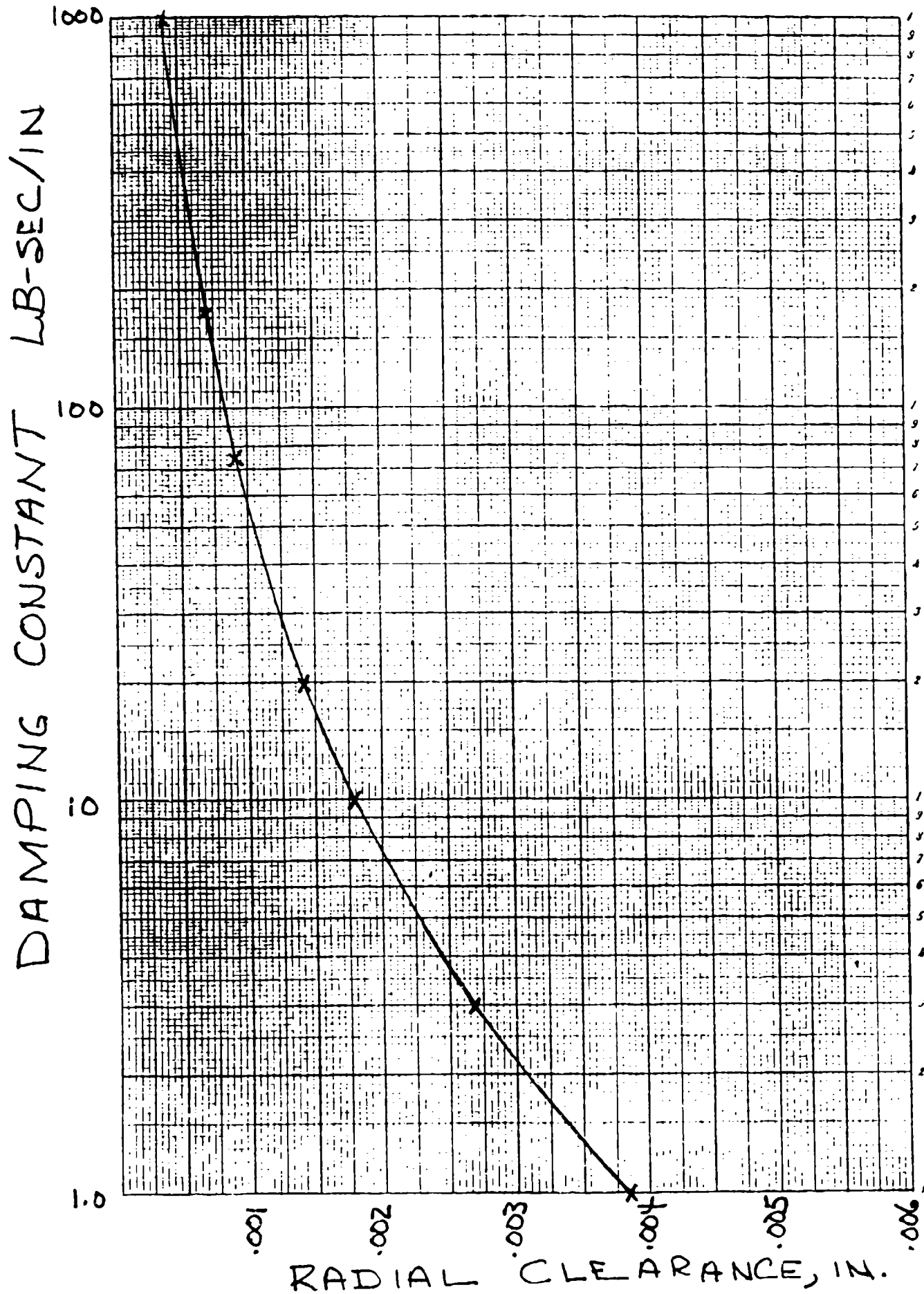
Figure 2.2.3-4

Damping Constant as a Function of Clearance
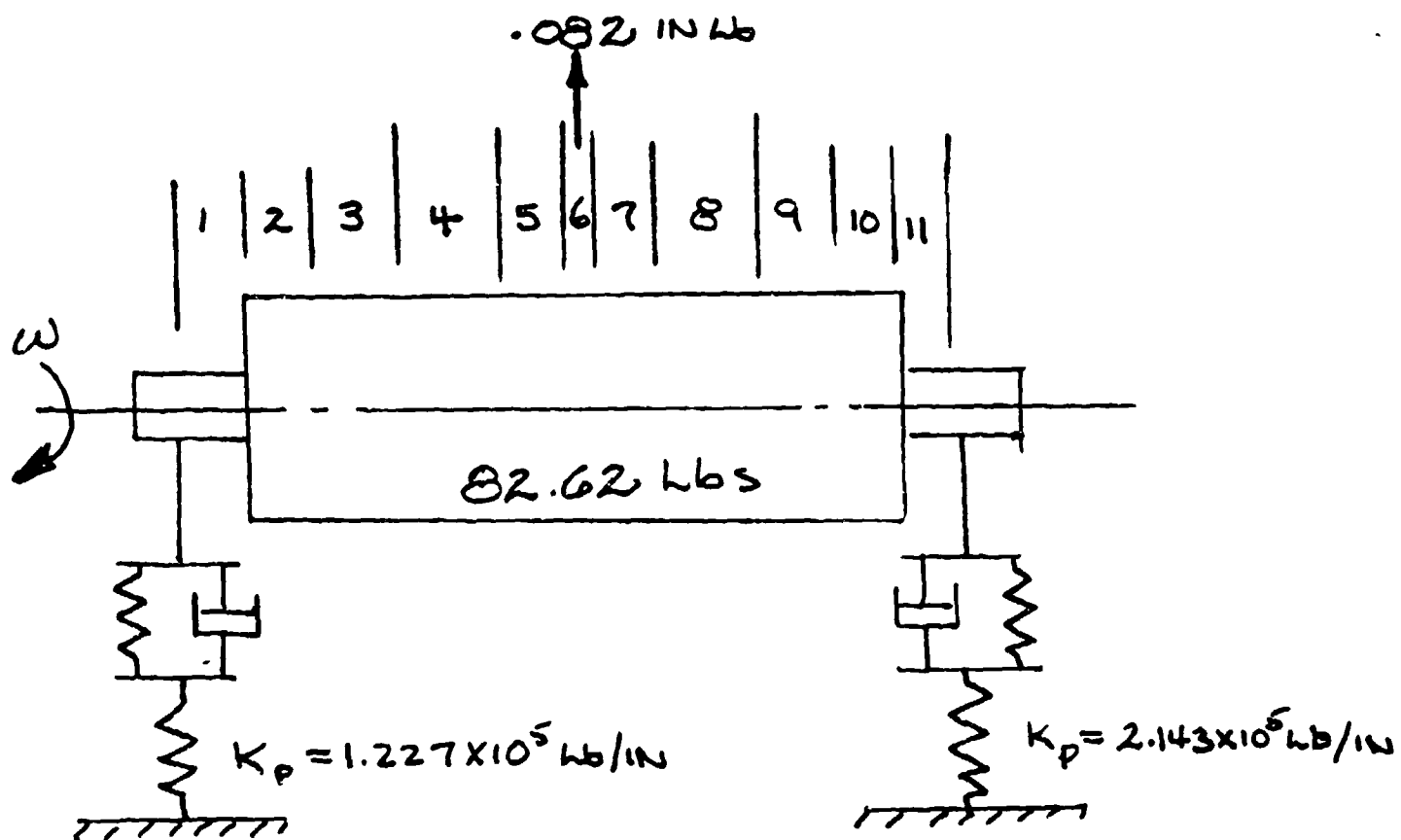
Figure 2.2.3-5
Rotor System
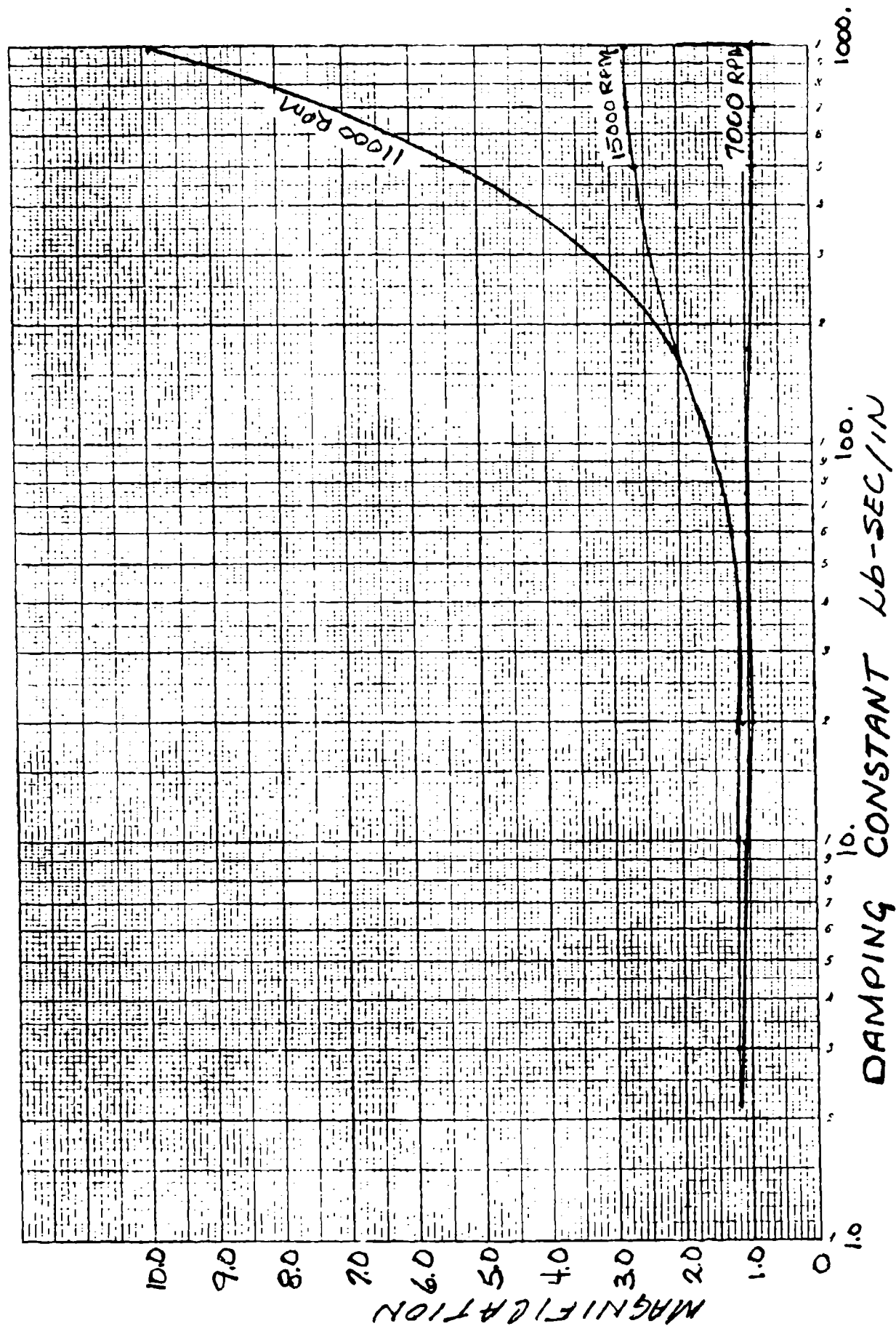
Figure 2.2.3-6

Vibration Magnification versus Damping Constant

2.2.3.4   Damped Rotor System (Continued)

It can be noted from Figure 2.2.3-6 that a significant magnification of the
unbalance driving motion does not occur until the instantaneous damping
constant approaches 40 lb-sec/in. At this point, vibration at approximately
11,000 rpm shows a magnification factor approaching 10 as the damping constant
approaches 1000 lb-sec/in.

The critical speed of 11,000 rpm appears because the stiffness of the damper
clearances are approaching the stiffness of the bearings and their brackets.

Table 2.2.3-2 give the rotor vibration for a range of damper oil temperatures
based upon a steady state damper constant of 3 lb-sec/in. at 100°C. The other
parameters of interest for these calculations are:

$$W = \quad .6299 \text{ in.}$$
$$D = \quad 2.4409 \text{ in.}$$
$$L = \quad 0.250 \text{ in} \qquad \text{Reference Figure 2.2.3-1}$$
$$R = \quad 0.039 \text{ in}$$
$$G = \quad 0.090 \text{ in.}$$
$$C = \quad .00267 \text{ in.}$$

2.3   Generator Control Unit

The (GCU) provides control and protective functions for the generator. The
control functions include voltage regulation, paralleling, and circuit breaker
control. The protection functions include overvoltage, undervoltage,
overfrequency, current limiting, and differential protection. Figure 2.3-1
shows a logic diagram for the GCU.

Power for the GCU is derived from the Permanent Magnet Generator (PMG) in the
alternator. PMG power is rectified for use directly by the voltage regulator
and regulated to +24 and +15 volts for circuit breaker power and logic.

The alternator exciter field current is controlled by a half bridge switching
regulator consisting of Q1 and Q2. This configuration allows both positive
and negative forcing of the field for improved voltage regulator response.

Table 2.2.3-3
Estimated Rotor Vibration for Various
Temperatures of the Damper Oil

Temperature °C	B_V lb-sec/in.	B_H lb-sec/in.	Maximum Vibration Single Peak, In. 1,000 to 15,000 rpm	rpm
-30	500	900.	5.21×10^{-4}	11,000
0	60	108	1.22×10^{-4}	15,000
22	23	41.4	1.17×10^{-4}	15,000
100	3.0	5.4	1.19×10^{-4}	15,000
120	2.2	4.0	1.19×10^{-4}	15,000

ENCO 2389 Turbo Oil
Unbalance is .0082 lb-in

Figure 2.3-1
GCU Logic Diagram

2-38

2.3   Generator Control Unit   (Continued)

Output of the alternator is controlled by sensing the 13.2kv-dc output when
the HVDC system is actuated, or by sensing the alternator output at the
generator breaker to the HVDC system (GBC). When the GBC is open, the output
of the alternator is regulated to approximately 140v L-N. When the GBC is
closed, and after a 0.1 to 0.2 second delay, the sensing is transferred to the
13.2kv-dc output. The reference voltage ramps smoothly up to the reference
level, providing a soft start for the high voltage system. If the GBC opens,
the process reverses, but with no time delay. This method provides the least
system disturbance.

Current limiting is provided at both the high voltage and 400-Hz breakers by
current transformers connected to the GCU. The current signals limit
generator excitation to a safe level.

Alternator speed is sensed from the PMG frequency. Generator Underspeed 2
(GUS2) is set at 83% speed and allows the GBC to close at this point if the
high voltage switch is ON. Generator Underspeed 1 (GUS1) is set at 53% speed
and trips the system off below this point.

Generator Differential Protection (GDP) trips the system if there is a feeder
fault between the alternator and the 400 Hz or HVDC systems. Generator
Overfrequency (GOF) provides the same action above 110% speed.

Generator Overvoltage and Generator Undervoltage (GOV and GUV) sense the
alternator output voltage at the input to the 400-Hz system (GBA). The
overvoltage function provides an inverse time delay, while the undervoltage
time delay is fixed at 5.5 to 7.5 seconds. Level of GOV and GUV is dependent
on whether the GBC (HVDC) contactor is closed or open.

Exciter field current (EFA) is monitored and limited to a safe value by the
EFAHI circuit. Excess field current will trip off the system.

2.3   Generator Control Unit   (Continued)

If the generator control and high voltage switches are left in the ON
position, the system will start up automatically at 53% speed and close the
GBC at 83% speed. The system will shut down below 53% speed but will not lock
out. This allows for automatic restart if the speed increases above 53%.

Load division during parallel operation is provided by biasing the HVDC
sensing with a differential load signal. Load current is sensed by a current
transformer at the HVDC input. Differential load current is measured across a
load division loop connection between paralleled channels. Over and under
excitation (OE and UE) are developed by a similar circuit biasing the over and
under voltage circuits.

Figure 2.3-2 is a complete schematic of the GCU.

2.3.1   Printed Wiring Board 1

PWB1 provides sensing of the alternator voltage from GBA. The three sensed
phase voltages are rectified and divided down to a low level. Analog switch
U101 selects the sensing level depending on the mode of regulation. The
output of U101 is buffered by U102A and applied to the overvoltage circuit
around U102D and the undervoltage circuit around U103C. Both protective
circuits provide instantaneous outputs (GOV and GUV) before their respective
time delays (GOVTD and GUVTD).

The undervoltage time delay is inhibited by underspeed signal GUS1 to prevent
undervoltage trips for normal system shutdown.

Differential protection sensing is provided by rectifying the voltage of all
six differential protection current transformer (DP CT) loops. The voltage is
limited by VR101 and the GDP output is produced after a time delay of
approximately 75 milliseconds controlled by R130 and C105.
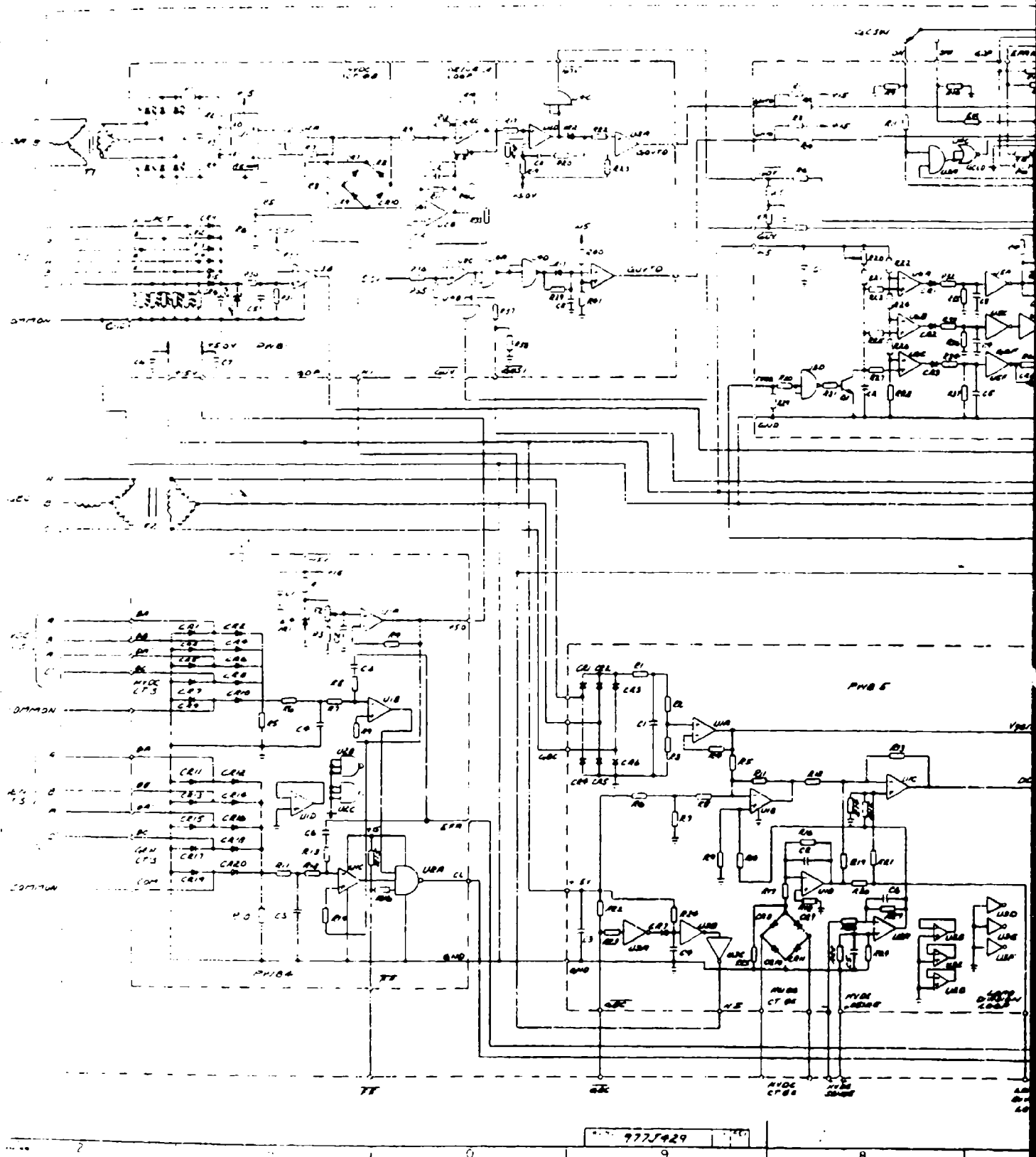
Figure 2.3-2

Generator Control Unit Schematic

SCHEMATIC DIAGRAM
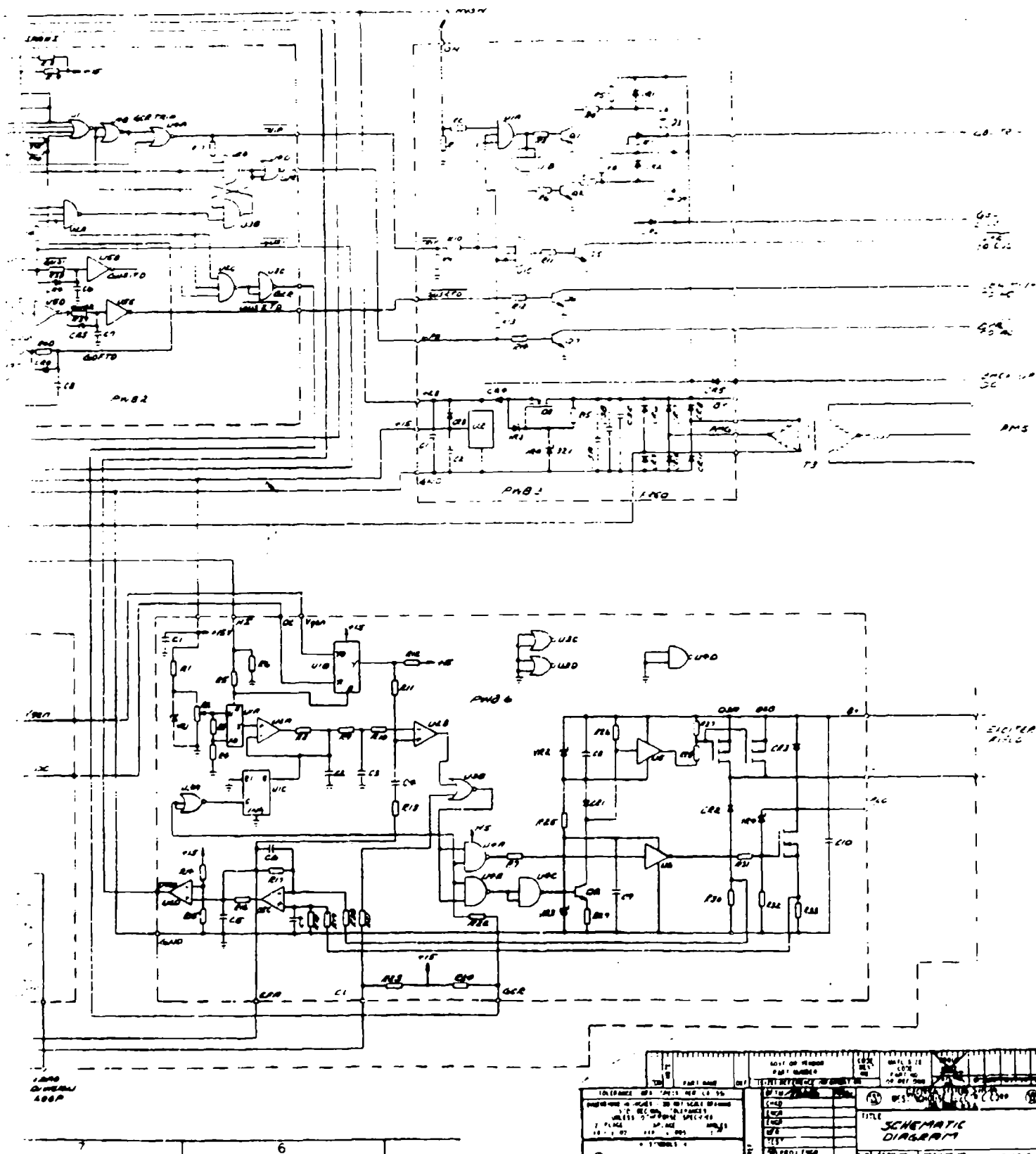
2.3.1 Printed Wiring Board 1 (Continued)

Over and under excitation bias is developed by sensing the AC current into the HVDC system. The current transformer output is rectified and develops a voltage across R108. This signal is filtered by U102B to form a DC voltage proportional to load current. The output of U102B is connected to the same point in the parallel channel through R116. The voltage across R116 is thus proportional to the unbalance in load current. This unbalance signal is added to the HVDC sensing signal by U102C to bias the over and undervoltage circuits to provide selective tripping during parallel operations.

2.3.2 Printed Wiring Board 2

PWB2 combines random system logic functions with speed sensing circuits. The logic circuit implements the operation of the logic diagram previously described. CMOS logic gates are used throughout the design.

The speed sensing circuit monitors one phase of the PMG output. When the frequency signal is high, transistor Q201 is turned off, allowing C202 to charge. At high speeds, C202 reaches a lower peak voltage, while at low speeds C202 charges higher. Amplifiers U206A, B, and C compare the peak voltage with a preset level and produce a pulse if the voltage exceeds that level. These pulses are averaged by C203, C204, and C205 to develop the GUS1, GUS2, and GOF signals at 53%, 83%, and 110% speed. The GUS1 and GUS2 signals are delayed by 0.1 to 0.2 second to form GUS1TD and GUS2TD. The GOFTD delay is 0.5 to 1.0 second.

2.3.3 Printed Wiring Board 3

PWB3 contains the GBC circuit breaker driver circuit, output interface circuits, and the PMG power supply. The PMG output is rectified, filtered, and connected directly to the voltage regulator circuit. This voltage varies from 70 to 140V DC over the operating speed range of the system. The DC voltage is further regulated to 28V DC by Q308 to supply external switches and power for the circuit breaker driver circuits. Control power (+15V DC) is regulated down from the +28V DC by U302. All regulators in the power supply circuit operate in the linear mode.

Circuit breaker drivers Q303 and Q304 are P channel FETs that can easily handle the peak currents required by the circuit breakers while minimizing drive components. Heat sinking is not required for Q303 and Q304 due to the short pulse (25 msec) required to operate GBC. The low average power dissipation of the GCU makes the linear power supply design practical.

2.3.4 Printed Wiring Board 4

PWB4 provides current limiting for the alternator and the HVDC system. In addition, a 5.0V DC reference voltage is provided by VR401, buffered by U401A, and supplied to the other circuits in the GCU.

Excess current into the HVDC transformer is sensed by current transformers and rectified. A voltage signal developed across R305 is filtered by R306 and C304 and compared to the 5.0V reference. Excess current generates a current limit (CL) signal. Alternator current is sensed in the same fashion. A signal proportional to the EFA is added to the current sensing signal to provide stable operation during current limiting.

A separate input is provided into the board for field forcing (FF) to generate a CL signal. This input allows the converter controls to momentarily force the alternator field current down during a transient.

2.3.5 Printed Wiring Board 5

PWB5 contains sensing circuits for the voltage regulator and circuit breaker status sensing. An auxiliary contact on GBC provides a grounding signal when the breaker is closed. This signal, after a 0.1 to 0.2 second time delay, generates the HI signal, commanding the voltage regulator to begin sensing the HVDC output, rather than the alternator output.

Alternator output voltage is sensed at the GBC breaker, rectified and divided down. The buffered signal, Vgen, is supplied to the voltage regulator.

The HVDC voltage is sensed by a high voltage divider connected directly to the HVDC output. Sensing is differential so that either end of the HV supply may be grounded, as long as one end of the divider is at ground potential. The sensed voltage is filtered by U502A and buffered by U501C to become the DC signal applied to the voltage regulator.

The DC signal is biased by means of a load division circuit similar to the OE/UE bias circuit to provide current sharing during parallel operations. Channels operating in parallel communicate through the load division loop connection.

During no load, parallel operation U501B adds a bias to the DC sensing voltage to keep all the alternators near the proper voltage. Without this bias, all but one of the alternators would shut down. System output voltage would be normal, but the remaining alternator capacity would not be available on a transient basis nor would outputs be available for the 400 Hz and the 28 volt DC systems. The U501B circuit keeps the alternator output within 90% of the normal level.

2.3.6 Printed Wiring Board 6

PWB6 contains the alternator voltage regulator. Sensing signals Vsgen or DC are selected by analog switch U601B and compared to the reference voltage derived from VR501, a temperature compensated zener diode. The output of U502B consists of a pulse width modulated waveform. This waveform is combined with the current limiting and GCR signals, amplified, and ultimate are used to drive the half bridge formed by Q503A, B, and Q504. This amplifier controls the voltage and current applied to the alternator exciter field winding.

EFA is sensed by R530 and R533 and filtered by U502C, producing the EFA signal. Amplifier U502D provides an EFAHI output when the EFA exceeds a safe level.

Analog switch U501A selects the proper reference voltage level for AC or DC regulation and U2A provides a controlled ramp for the reference when switching between operating modes.

Analog switch U501B shorts out the reference when the GCR is tripped and releases to provide a soft start at system startup.

2.4 Converter - Inverter

The 400 Hz AC output is derived from the variable frequency, variable voltage input from the generator source. The converter portion is controlled by what is defined as a preregulator to maintain the 400 Hz system output. The power output of the converter feeds the inverter which is controlled by the Inverter Control Unit.

The preregulator controls are new to the DC-link type VSCF system. The theory of operation of this means of controlling the DC-link voltage is first discussed, followed by the theory of inverter operation.

2.4   Converter - Inverter   (Continued)

The power stage for the DC link is shown in Figure 2.4-1. The output power
devices are SCR1 through SCR12 which receive power from the two sets of
three-phase windings from the generator. The outputs of the two SCR bridges
are combined feeding into the output filter. The filter output then is fed to
the inverter.

The SCR driver circuits are controlled by the preregulator. The schematic for
the preregulator is shown on Figure 2.4-2.

2.4.1.   Preregulator Circuit Description

2.4.1.1   Preregulator Input Circuitry

The three-phase generator output voltages are reduced by a factor of 100 at
the input to the preregulator circuit. The three phases are summed together
in U1A to form a neutral. This formed neutral is summed with each phase to
form the three-phase voltages with respect to neutral at the output of U1B,
U1C, and U1D. These signals are then used in the SCR timing circuit and the
input level detector circuit.

2.4.1.2   Input Level Detector Circuit

The input three-phase voltage level must be known to calculate a maximum
permissble demand signal. If a higher DC voltage is demanded than can be
formed with a particular AC three-phase input, the SCR timing circuit will
advance the firing angles of the SCRs beyond the point that will create
maximum DC output. This will result in unstable system operation.

A maximum permissible demand signal is created by measuring the amplitude of
the AC input and calculating the equivalent DC output this AC input can
sustain. This maximum permissible demand is substituted for the actual demand
when it is lower than the actual demand.

2-47

Figure 2.4-1

Pre-regulator Power Stage
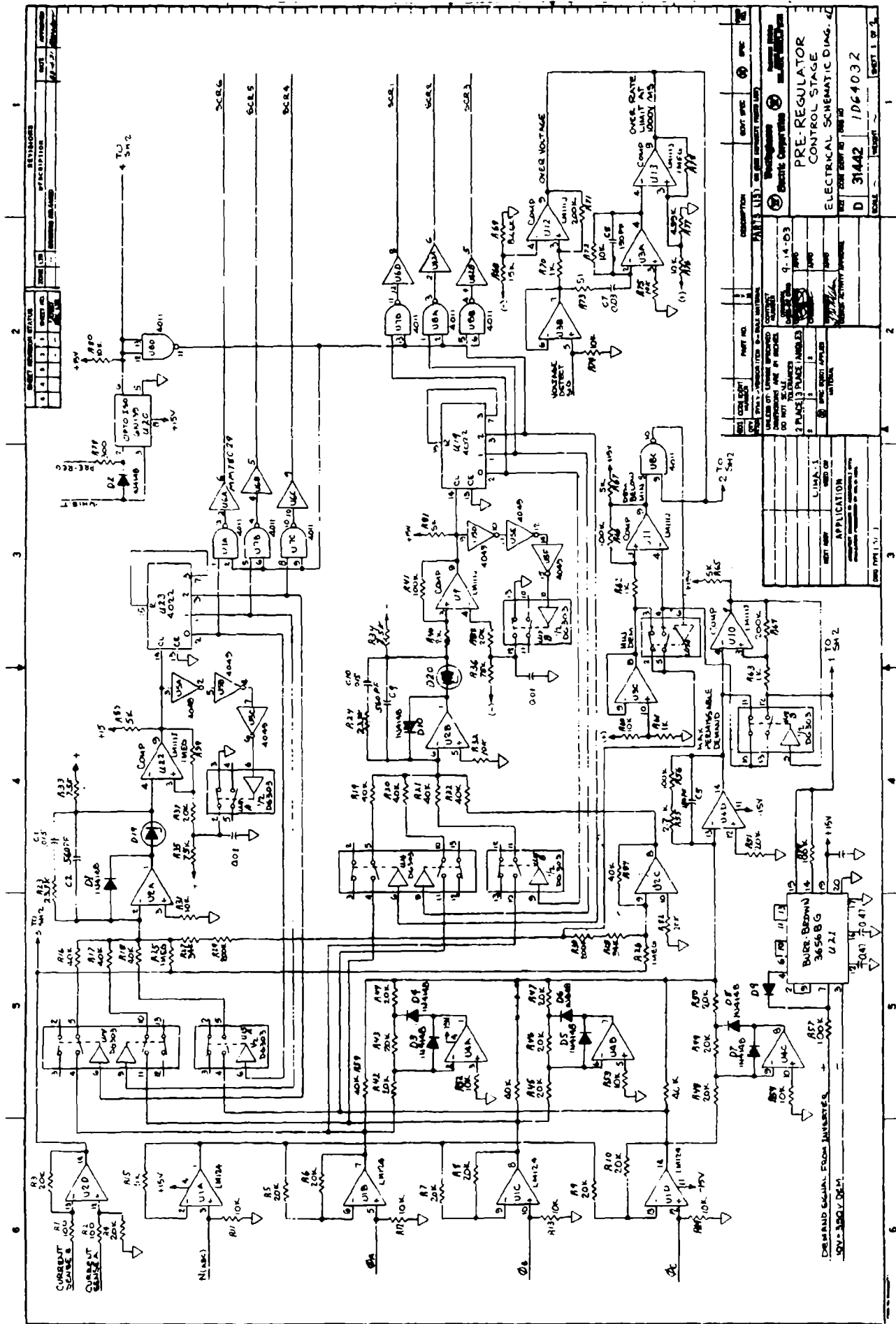
Figure 2.4-2   Pre-regulator Control Stage
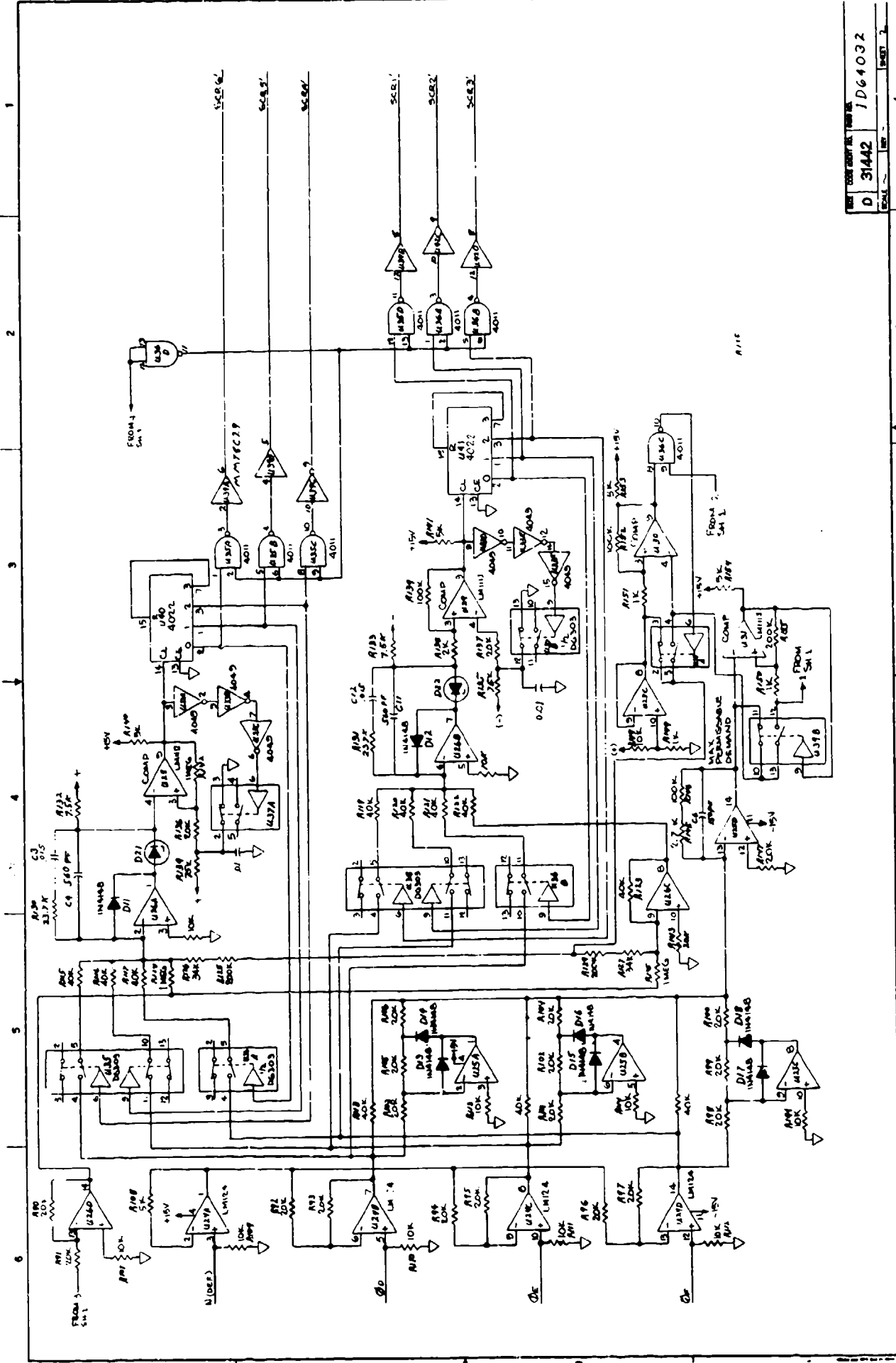
Figure 2.4-2 (Continued)
Pre-regulator Control Stage

2-50

2.4.1.2   Input Level Detector Circuit   (Continued)

Each phase of the three-phase input is rectified in U4A, U4B, and U4C. The three rectified signals are summed and scaled in U4D. The output of this amplifier (U4D) represents 95% of the highest attainable DC output with the available input voltage. This provides a 5% system safety margin.

2.4.1.3   Controller Demand System

The demand signal from the 400 Hz inverter is scaled for ten volts demand to be equal to 350 VDC out of the preregulator. This demand signal from the inverter is isolated from the preregulator system using an isolation amplifier. In order to assure correct operation of the SCR control system the demand signal's magnitude must be limited. If the demand signal exceeds the maximum permissible demand signal out of U4D, the comparator U10 switches the demand signal to this value. If the demand signal is lower than the minimum demand at U3C the comparator U11 switches the demand to this minimum demand signal. At minimum demand the preregulator's DC output will be approximately 50 VDC. The maximum permissible demand is a function of the three-phase AC input voltage.

2.4.1.4   SCR Timing Circuit

A simplified SCR timing circuit with timing diagrams is shown in Figure 2.4.1.4-1 A Johnson counter provides that one, and only one, of the three input switches is closed. In the timing diagram when S1 is closed and V_A is more negative than V_{dem} the integrator's output goes positive. If V_A is more positive than V_{dem} the integrator's output goes negative. When the output of the integrator (V_A) becomes more negative than the voltage accross the capacitor (V_C) the comparator's output changes state and advances the Johnson counter one count and momentarily shorts V_C to ground. The Johnson counter's output also goes to the SCR firing circuit which turns on the SCR connected to the same phase as the turned on control switch. Each SCR is turned on for 120°.

Johnson Counter
CD4022   CL

"0"   "1"   "2"

To Φ_A SCR
To Φ_B SCR
To Φ_C SCR

Φ_A/N S1

Φ_B/N S2

Φ_C/N S3

OP/amp

V_A

V_C Comp V_B

(+)

S4

Demand V_{DEM} (-)

Φ_A/N Φ_B/N

Reduced Input

V_{DEM}

S1 Control   CLOSED

S2 Control   CLOSED

S4 Control   closed

V_A

V_C

O Volts T_2 T_1

Figure 2.4.1.4-1
Simplified SCR Timing Circuit

2-52

2.4.1.4   SCR Timing Circuit   (Continued)

The dotted lines on the timing diagram illustrate what happens if the input voltage to the controller drops. Without a change in the SCR firing angle the preregulator DC output will drop. When the input voltage drops the control integrator's output (V_A) drops and becomes lower than V_B at a time T2 which is earlier than the normal firing time T1. The earlier firing of the SCR will hold the output voltage at a constant level, even though the input AC voltage dropped.

The controller as illustrated would provide the timing of the three SCRs in the negative line of one three-phase system. A second circuit using inverted demand and control voltages will be used to control the three SCRs in the positive line. These two circuits would provide the SCR timing for all six SCRs in a three-phase system.

The preregulator system is connected to two three-phase generator windings with a phase separation of 30°. Two three-phase/six SCR controllers are used to make up the total preregulator. An interphase transformer is used to connect the negative leads of the three-phase systems together. Controller circuit ground is referenced to the positive side of the output.

2.4.1.5   SCR Triggering

The trigger circuit for SCRs must provide a steep gate current and must hold substantial gate current for 65° at the lowest frequency. The SCRs are triggered through a transformer. The circuit is shown in Figure 2.4.1.5-1.

During off-time, a positive voltage pulse is applied to the gate of Q1. Transformer T1 saturates, the current being limited by R4. To turn the SCR on, the pulse is terminated and Q1 serves as a switch to block further current in the primary of T1. The secondary will now conduct with an initial current of $I_2 = I_1 \times ([N_1]/N_2)$ and a time constant of L/R where "R" equals the total load seen by N2.

2-53
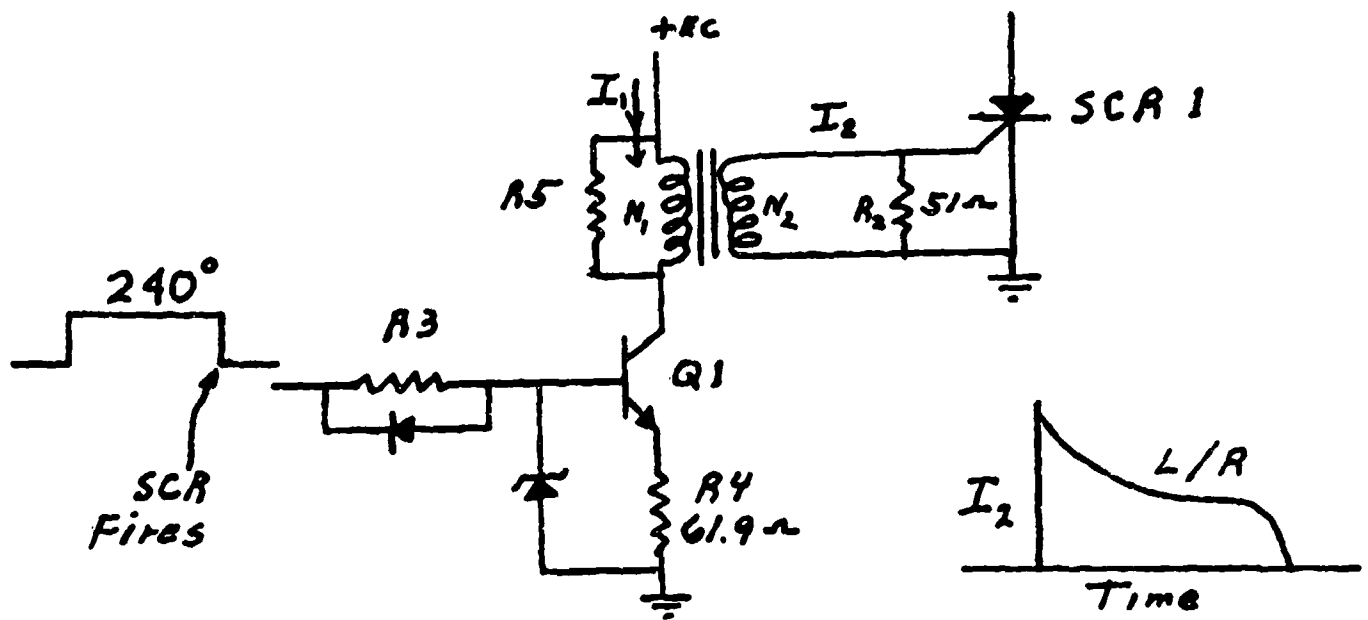
Figure 2.4.1.5-1
SCR Trigger Circuit

2.4.1.6   Preregulator Output Volgage Safety Circuits

The preregulator system contains circuits to detect potentially destructive (to the 400 Hz inverter) output voltage magnitude and output voltage rates. When these undesirable conditions are detected, the demand to the control system is automatically switched to the minimum demand signal which will reduce the output to a safe level.

One of the output voltage safety circuits is the DC-link output overvoltage trip circuit. The DC output voltage is sensed and scaled in amplifier U3B. The comparator U12 compares the output voltage with a reference and changes state when the output voltage exceeds 336 volts. The controller demand is then switched to the minimum demand signal.

A second safety circuit is the output voltage rate trip circuit. The scaled output from U3B is connected to the rate sense circuit of amplifier U3A and comparator U13. If the DC output voltage rate exceeds 1,000 volts per millisecond this circuit switches the controller demand to the minimum demand signal. This circuit contains a single pole breakpoint at about 100 KHz to help prevent trips caused by noise pulses.

2.4.1.7   Preregulator Inhibit System

All SCRs can be prevented from being fired by an inhibit signal sent from the 400 Hz inverter. This digital signal is optically isolated from the preregulator power system. A five volt high on this inhibit line will permit normal operation of the SCR and a zero volt signal will prevent SCR firings.

2.4.1.8   Interphase Transformer DC Sharing Loop

The DC current from each three-phase section of the preregulator passes through the interphase transformer. These DC currents must be near the same level to prevent the interphase transformer from saturating.

2.4.1.8　　　　Interphase Transformer DC Sharing Loop　(Continued)

The DC current from each three-phase section is passed through a 50 millivolt shunt in the positive side of each circuit. The difference voltage from the shunts is applied to amplifier U1. This amplifier will have one volt output for a 40 amp difference in current between the two three-phase systems. This error voltage is scaled and added to the demand signal for one three-phase system and subtracted from the demand of the other three-phase system, to equalize the system currents. The system is scaled such that a 40 amp difference in currents will result in a 16 volt differential in the DC demand out of each system.

2.4.1.9　　　　The Interphase Transformer

To increase the ripple frequency of the net output, the two sections furnish DC with ripples that are 30° apart. In order that each section operates in a manner not to adversely affect the other, an interphase transformer is used. This allows each section to furnish current simultaneously, improving the efficiency.

From a previously run computer simulation it was determined that the interphase transformer inductance leakage should be 4.0 microhenries. This is shown below.

The coefficient of coupling may be found as follows:

$$E_1 = I1sL - I2sM$$
$$E_2 = -I1sM + I2sL$$

$$M = k \sqrt{L \times L}$$

From these equations we get:

$$I1 + I2 = \frac{E1 + E2}{sL(1-k)}$$

If E1 = E2, $\frac{2E}{I1+I2} = sL(1-k)$

or the effective inductance is $(L/2) \times (1-k)$.

Assuming the coefficient of coupling to be .95 then $L(1-.95) = 2 \times 4 \times 10^{-6}$ Hy

and $L = 1.0 \times 10^{-6}$ Hy.

A Spice program was run using $L = 160 \times 10^{-6}$ Hy to determine voltage ripple on the DC-link.

Parameters for this analysis include:

f = generator frequency

Vgen = L-N volts RMS

VL-L = $\sqrt{3}$ Vgen

VL-L(Peak) = $\sqrt{2}$ VLL

Average rectified value for three-phase full wave voltage is:

$$EDO = \frac{3}{\pi} VLL(Peak)$$

For 300 VDC with Vgen = 146 volts RMS, the phase back angle will be:

$$COS\alpha = \frac{VDC}{EDO} = \frac{300}{342} = .877$$

2.4.1.9   The Interphase Transformer   (Continued)

In the program $\alpha = 30°$ (angle between sets of generator voltages). The schematic and program were included in section 1. Since the objective was to study the interphase transformer, transistors could be used as switches to simulate SCRs. Diodes were included to prevent reverse current through the transistors.

The generated voltages A, B, and C are three-phase with 120° phase separation. Initial conditions are voltages on C1 and C2 and C-load. These voltages drive the top six SCRs in a "Y" connection. A delta connection is used for the lower six SCRs to get 30° phase shift relative to the top bridge. The 30° phase-back is obtained by the timing of I1, I2, etc., at Q1, Q2, etc. (SCRs). The period of the input was taken as 900 microseconds to simplify the current pulse timing diagram. The results show the ripple is slightly larger than 1% but was still decreasing when the computer run terminated. Also, note that each generator leg contained only 0.001 ohm. The source induction is 12 microhenries including the line impedance. Including this value should reduce the ripple further.

The flux which is produced in the interphase transformer core by the volt-second differential was simulated. Variation of "B" was approximately 2,200 gauss. The absolute value will depend on the initial conditions assumed.

Except for the .95 coupling factor the values defined should not be difficult to attain in a relatively small package. If this coupling factor cannot be attained, but is smaller, "L" will be found to be smaller.

2.4.1.10   The Thyristors

Westinghouse Type T627 SCRs were chosen. These are a fast switching type and are rated at 1,200 volts. Using 12 microhenries as the source impedance and a maximum voltage of 600 volts and using $di/dt = E/L$, $di/dt = 50$ amperes per microsecond. For this SCR under these conditions the charts indicate a dissipation of 0.1 joule per pulse or 120 watts at 1,200 Hz, and for 2,500 Hz the values are .07 and 175 watts dissipation. Heat sinking must be chosen for this higher value.

2-58

2.4.1.10   The Thyristors   (Continued)

The snubber resistor was calculated using 20 KVA per phase, a damping factor of
.8 and line inductance of 24 microhenries. The worst case dissipation in "R" was
calculated to be approximately 20 watts.

2.4.2   DC to AC Conversion (400 Hertz Inverter)

The inverter is the second of two power conversion elements required to
accomplish the function designated as the AC conversion device (AC1 - AC4). This
element converts the controlled level of DC provided by the AC to DC preregulator
into precision three-phase 400 Hertz power. The power rating for each individual
element is 90/120 kVA. Figure 2.4.2-1 represents a block diagram of the
sub-elements making up the inverter and its interfaces.

The block diagram illustrates the DC-link VSCF type conversion system used on
three aircraft now flying. They are:

1.   McDonnell Douglas AV-8B Harrier
2.   Northrop F-20 Tigershark
3.   General Dynamics F-16 Fighting Falcon

The rating of the F-20 is the highest of the three at 30/40 kVA, but development
is underway for a 75 kVA system for other applications. The rating for the
Wright Patterson Air Force Base system is 90/120 KVA. As such, the currents
switched and controlled are much higher, necessitating design concepts which
limit the connection path lengths for all power conversion devices to an absolute
minimum. Coupling between off-going and on-coming devices has been coordinated
in the mechanical design.

The following paragraphs provide the requirements and design rationale for each
of the sub-elements shown on the block diagram.
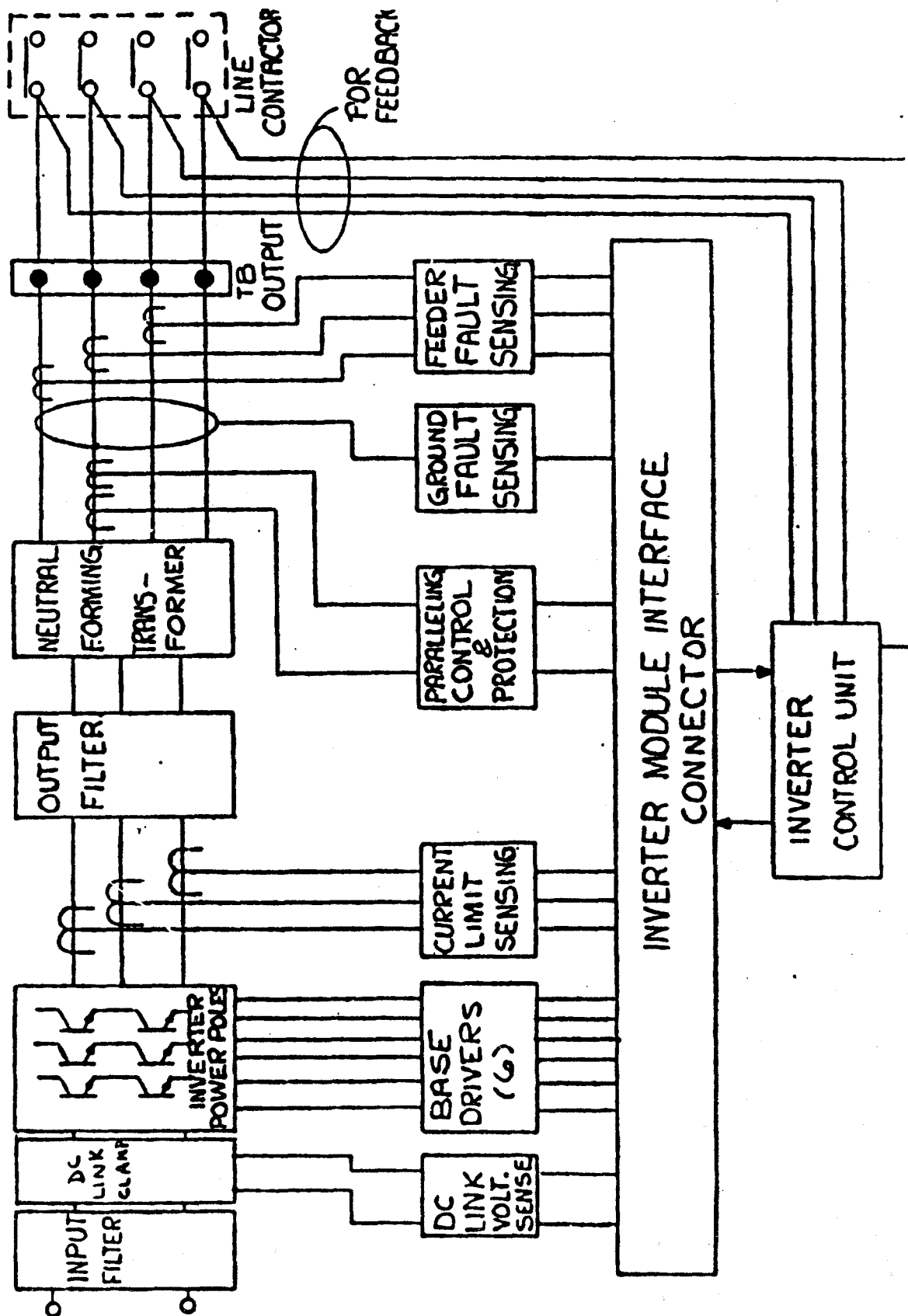
Figure 2.4.2-1

Inverter Power Stage Block Diagram

2-60

2.4.2.1   Input Filter (DC-link Filter)

The input filter for the inverter element is actually a predominant part of the AC-DC preregulator. It serves several important functions for the inverter as well.

The filter capacitor is composed of 13 discrete capacitors each rated 50μf, 400 WVDC. Since power flow is uni-directional from the preregulator, these capacitive storage elements not only filter the preregulator ripple voltage, but also serve as temporary energy storage during transient loadings. In addition to providing the filtering for the preregulator, this capacitor bank acts as a low impedance for the circulating harmonic currents produced by the inverter power stage switching. These ripple currents are relatively high, necessitating high quality AC type capacitors rather than electrolytic type (See Table 2.4.2.1-1) A second filter function located on the DC-link bus is an 800 Hz trap filter, which will provide a low impedance for the 800 Hz circulating current generated by unbalanced loads. The input filter is shown on Figure 2.4.2.1-1

The DC-link voltage and current parameters into the inverter are shown on Figures 2.4.2.1-2 and 2.4.2.1-3

2.4.2.2   DC-Link Clamp

A DC-link clamp precludes an overvoltage on the DC-link. The reasons for implementing the clamp circuit are:

1. Protection of the power transistors in the inverters (high cost devices).

2. A failure or misfiring of the AC-DC preregulator can produce high DC-link voltage.

3. Unknowns relative to paralleling of systems.

4. Overvoltage transients due to overload "off" switching.

Table 2.4.2.1-1
DC-link Ripple Current Produced By Inverter

(HZ) FREQUENCY	NO LOAD		120 kVA 1.0 PF		DC-LINK CAPACITOR = 650 mfd (C1)
	AMP-RMS RIPPLE	VOLT-RMS RIPPLE	AMP-RMS RIPPLE	VOLT-RMS RIPPLE	
2,400	17.8	1.79	26.6	2.68	(L2-C2) Note: 800 Hz trap current
4,800	7.4	.37	35.8	1.80	is 70 amperes (worst case)
7,200	28.1	.93	15.2	.50	at a 2/3 load unbalance on system output.
9,600	55.7	1.37	42.9	1.06	
12,000	22.3	.45	26.8	.54	
12,800	----	----	17.6	.32	
13,200	9.6	.18	----	----	
14,400	29.2	.49	27.8	.46	
16,800	25.0	.36	28.8	.41	
19,200	24.2	.30	14.3	.18	
21,600	4.0	.04	2.9	.03	
24,000	21.0	.21	14.8	.15	
26,400	7.6	.07	13.1	.12	
28,800	9.6	.08	11.1	.09	
31,200	6.2	.05	6.0	.05	
33,600	14.5	.10	10.9	.08	
36,000	6.6	.04	7.1	.05	
40,800	10.8	.06	2.4	.05	
43,200	5.0	.03	10.0	.06	
45,600	4.2	.02	4.2	.02	
48,000	4.4	.02	7.4	.04	
Total RMS	94.2		94.5		

L1 - 4μhy (LEAKAGE INDUCTANCE AS NOTED ABOVE)
C1 - 650μFD (RECOMMEND 13 OF COR. DUB. KBSF37US060P1-50μFD, 370VAC)
C2 - 150μFD - 800 Hz TRAP-(RECOMMEND 3 OF COR.DUB. " " ")
L2 - 265μhy - 800 Hz TRAP- (ESD LIMA TO PROVIDE)

WPAFB 90/120 kVA DC LINK SYSTEM - CONVERTER/INVERTER INTERFACE

DL STECHSCHULTE 2/18/83
ENGRG - ESD LIMA

Figure 2.4.2.1-1
WPAFB 90/120 kVA DC-link System
Converter/Inverter Interface

2-63

WPAFB DC LINK SYSTEM

DC LINK AMPERES VS. LOAD AND POWER FACTOR

NOTE: 120 KVA - STEADY STATE
135 KVA - 5 MINUTES
180 KVA - 5 SECONDS

SYSTEM OUTPUT LOAD - KVA

STECHSCHMUP 2/18/83
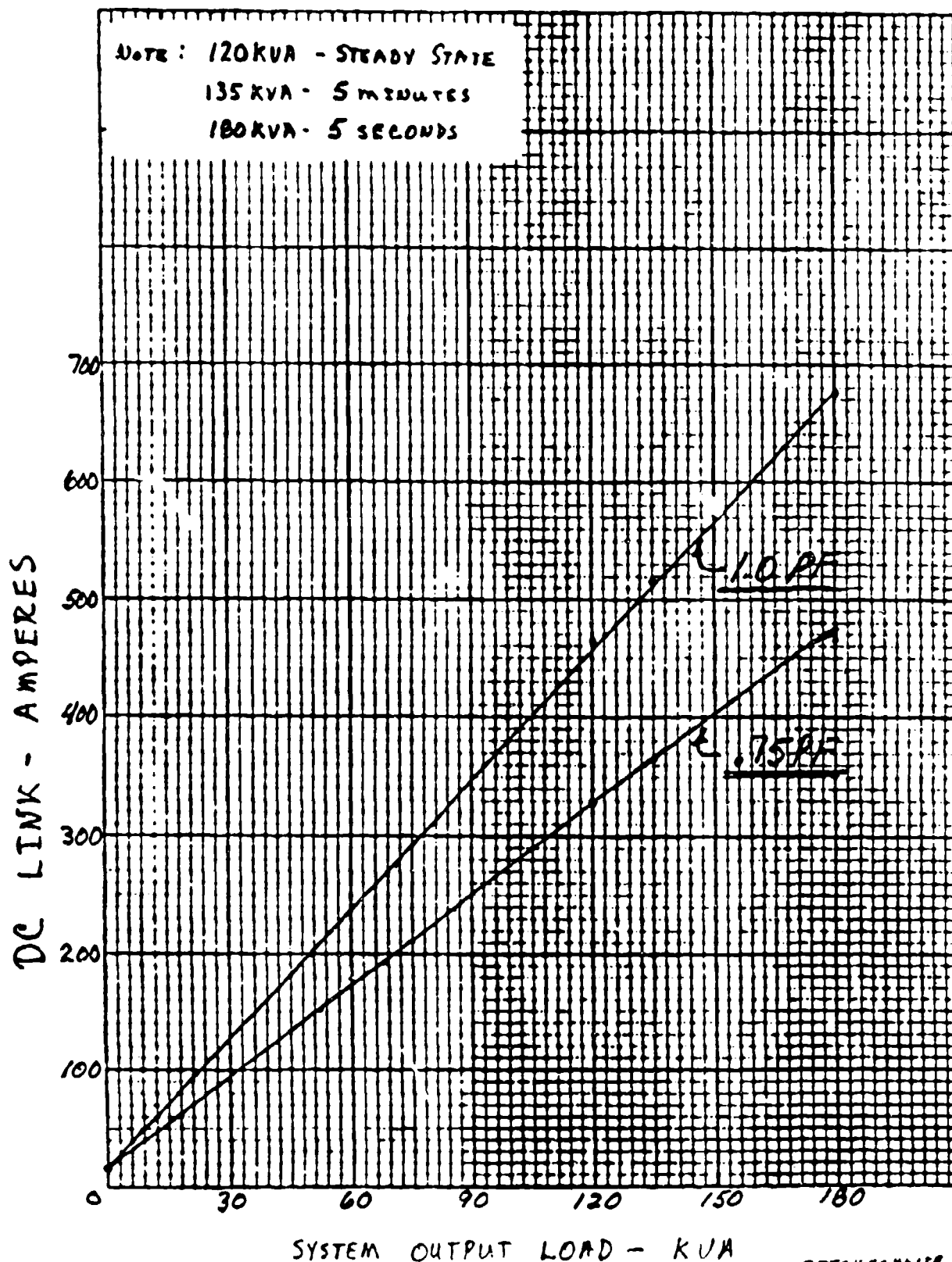
Figure 2.4.2.1-2
DC-Link Amperes vs. Load

2-64

1279R

WPAFB DC LINK SYSTEM

DC LINK VOLTAGE VS. LOAD AND POWER FACTOR
(BASED ON 1 VOLT FEEDER DROP FROM SYSTEM OUT TO POR AT 120KVA.

NOTE: 120KVA - STEADY STATE
135KVA - 5 MINUTES
180KVA - 5 SECONDS

DC LINK - VOLTS

SYSTEM OUTPUT LOAD - KVA

STDC HICHULJE 2/18/83
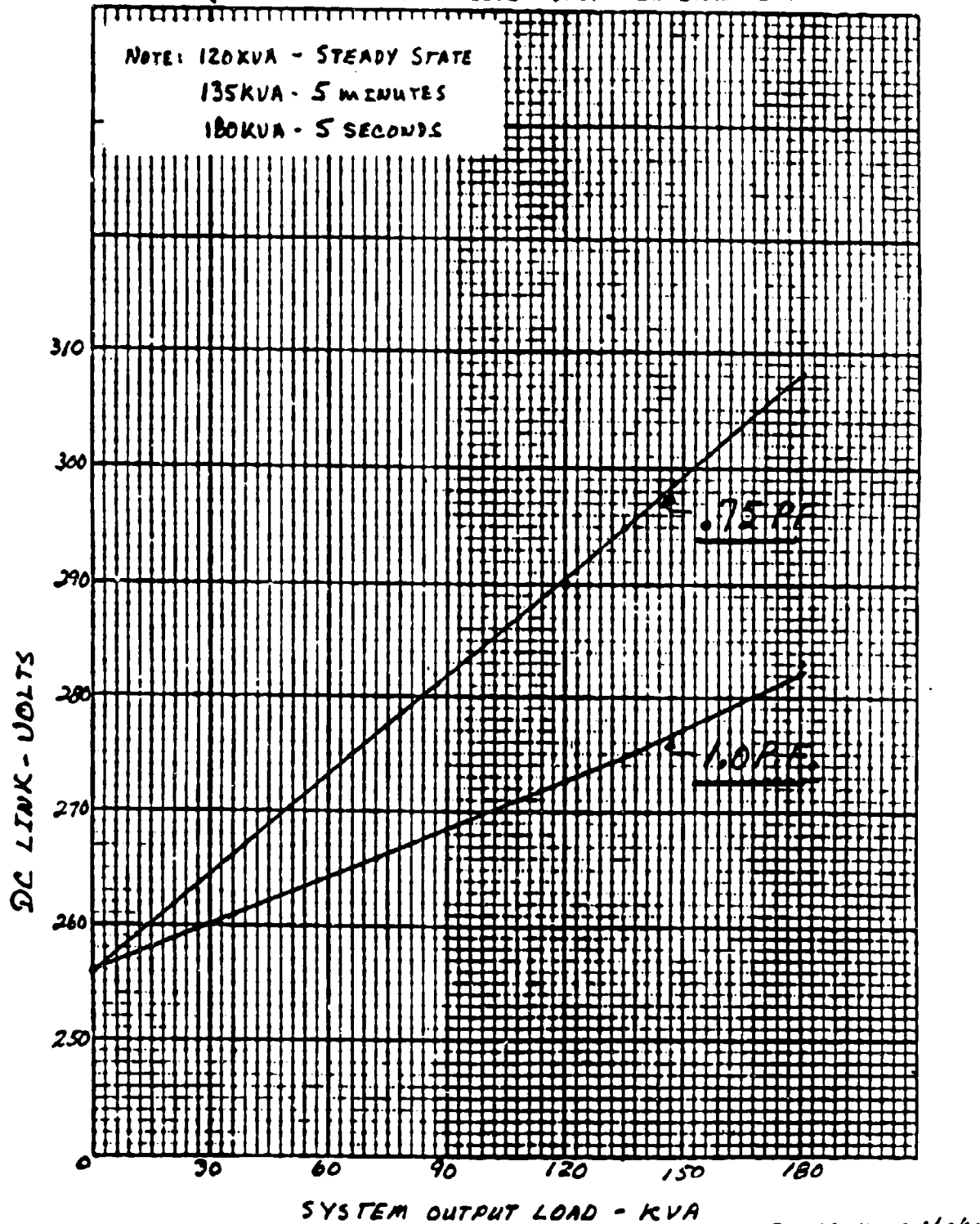
Figure 2.4.2.1-3
DC-link Voltage vs. Load

2-65

1279R

2.4.2.2 DC-Link Clamp (Continued)

The clamp circuit is shown in Figure 2.4.2.2-1

Turn-on of power transistors QS1-QS2 is initiated at approximately 340 volts on the dc-Link. The load resistance RS1, RS2 is .5 ohm total and rapidly decreases the link to below 340 and the transistors turn off. If the voltage climbs above 340 again another power pulse is applied. An integrator is used to accumulate the total "on" time. If "on" time adds to 100 milliseconds in a 5-second period, a sustained DC-link overvoltage signal is developed and sent to the protection circuit, which initiates a system shutdown.

This function as designed is not a finalized version. Because of the experimental nature, the resistors are oversized in this preliminary design. As actual requirements are developed, the size of these components will decrease.

2.4.2.3 Inverter Power Poles

The most critical item in the inverter design is the power pole or the power switching elements. Figure 2.4.2.3-1 is a simplified schematic of the proposed power pole dealing only with the power switching elements.

As noted earlier, the design for the WPAFB 90/120 kVA 400 Hz conversion element is based on prior designs, uprated to this power level.

There are three power poles required to generate the pulse-width modulated output which is then filtered. The fourth wire is established by the neutral forming transformer.

In each pole, there are two active switching elements comprised of an upper set of three power transistors and two commutating diodes and an identical lower set.

Figure 2.4.2.2-1

DC-link Suppressor for WPAFB 90/120 kVA VSCF

2-67
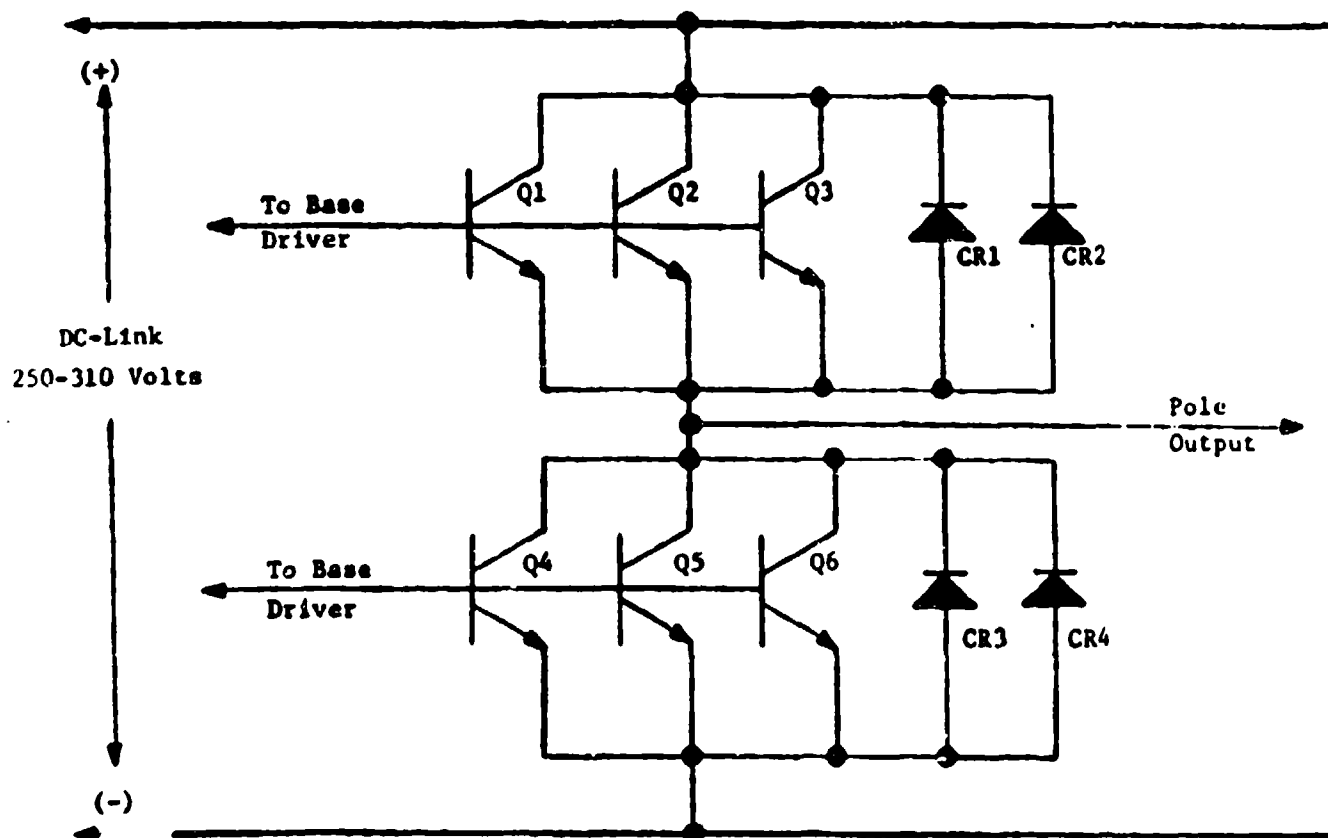
Figure 2.4.2.3-1
Simplified Power Pole

The power transistors are of primary concern as they alternately connect the
pole output to the dc-Link. All power flow to the load is through these
devices. Rated load current at 120 kVA is 348 amperes per phase. In
addition, the output filter capacitor circulates 156 amperes fundamental,
which is a quadrature component. At 120 kVA unity power factor load, the
total fundamental current is 384 amperes RMS. At 180 kVA unity power factor,
the current is 543 amperes. The peak current for this condition is nominally
1.414 times the RMS current. To account for the harmonic currents, this
factor is approximately 1.5 times the RMS current, or 815 amperes peak.

2.4.2.3   Inverter Power Poles (Continued)

If consideration is given to faults, the short circuit current is to 1 : three
times the rated current at 90 kVA, which is 783 amperes RMS. Short c: -cuit
current will not be sinusoidal, but will revert to a fundamental trapezoidal
current, which will have an RMS content of at least 783 amperes, but 1,200
amperes peak as seen by the power switching elements. The basic
voltage-current-time relationship for the power switching elements is shown in
Table 2.4.2.2-1

There are presently a number of semiconductor manufacturers which can
manufacture power transistors with high power ratings. There are none, which
combined with the cooling temperature requirements, can switch and handle the
total current with a single device. Therefore, this dictates paralleling or
greater circuit complexity. To make up a switching element with the current
and voltage requirements shown in Table 2.4.2.2-1 requires the paralleling of
transistors. The alternative to this is a great increase in circuit
complexity, which will have an adverse effect on reliability, size, weight,
and cost. It is the goal to maintain the configuration shown (i.e., three
power switching poles made up of six power switching elements). Table
2.4.2.2-2 shows ratings for various sizes of devices, all of which are
commercially available. The Size 9 is the preferred device for this effort.
This particular device is under evaluation in test circuits to characterize
performance.

Paralleling of power transistors and the effect on current sharing, especially
during the switching interval has been extensively evaluated the results of
which have been well documented. A brief summary of the conclusions of these
studies are as follows:

1. Power transistors can be operated in parallel.
2. The power transistors used in parallel must be matched if the total load
   current is a high percentage of the combined capability of the paralleled
   devices or suitable means must be incorporated into the circuit to force
   current sharing.

2-69

Table 2.4.2.2-1
Switching Element Operating Parameters

	DC-link Volt	IRMS (Pole)	IRMS (SW Element)	IPK	Time
120 kVA, 1.0 PF	276	384	270	576	Cont
180 kVA, 1.0 PF	291	543	387	816	5 Sec.
180 kVA, .75 PF	310	432	306	660	5 Sec.
Short Circuit	100	786	555	1,200	5 Sec.

Table 2.4.2.2-2
Power Transistor Ratings

Size	Westinghouse Part No.	V_{CER} (SUS) Min.	I_C Max.	I_C (SW)	HFe Min.	V_{CE} (SAT) Max.	No. in Parallel for 90/120 kVA SW Element
6	934A106	500	100	75	6	0.8	16
7	934A111-1	500	300	150	8	1.1	8
7X	934A111-3	500	300	200	12	1.4	6
Super 7		500	300	250	10	1.4	5
8		500	450	300	6	1.4	4
9	934A666	500	600	400	10	1.1	3

2.4.2.3   Inverter Power Poles (Continued)

3. The matching criteria are:

   a. V_{CEO} (SUS) - matched within specified limits per specification control drawing.

   b.   HFe at X% of peak current matched within specified limits per specification control drawing.

Figure 2.4.2.3-1 illustrates diodes (CR1-2 and CR3-4). They are connected in anti-parallel with the power transistors and are used to commutate reverse current flow. The selection of these devices is based on the following criteria.

1. <u>Vrb</u>:   Reverse blocking voltage which for this inverter will be 600 volts minimum.

2. <u>Iavg</u>:   The average forward current capability of this device; for this application - 400 amperes.

3. <u>Trr</u>:   Reverse recovery time; for this device - approximately 0.7 microsecond.

4. <u>Tj</u>:   Maximum junction temperature for this device is 175°C.

5. <u>Package</u>: For this application, the "hockey puck" package.

The reverse blocking voltage must be equal to or greater than the transistor voltage. The current requirement is dictated by the fault current capacity as related to the thermal excursion during the fault duration. The Trr is important in inverters because when factored with the reverse current in the device during this recovery period, the product represents trapped energy which must be dissipated. This recovery characteristic can be a source of EMI and must be accordingly handled. They are, therefore fast recovery devices.

2.4.2.4   Base Drives

The base drives (current) for the power transistors utilize controlled current feedback transformers (CCFTs). These transformers provide base current in proportion to collector current, thereby allowing very efficient control of the power transistors with a very low power and small-size drive circuit.

2.4.2.4 Base Drives (Continued)

This circuit is located in close proximity to the power transistors because of the high currents involved. The major functions performed by this circuit and its associated controls in the ICU are:

1. Turn the power transistors on and off.
2. Provide a base current to the power transistors that is proportional to the collector current, and determined by the minimum HFe (gain) of the power transistors.
3. Provide an effective means of shorting the CCFT at turn-off to quench the feedback ampere turns.
4. Provide a means to sweep the carriers from the base emitter junction at turn-off.
5. Provide a reverse bias to the base emitter junction during the "off" period of the power transistors.
6. Reset the CCFT during the "off" time to ensure adequate volt-second capability when the CCFT is driving the transistors.
7. Provide a clamp for the leakage reactance of the primary winding of the CCFT.

8. Provide an interlock between the upper and lower switching elements of the power pole to inhibit turn-on of a switch element until the off-going device has been cleared of carriers in the base junction and is totally off.
9. Provide a CCFT that has very good coupling between the base winding and the control windings.

2.4.2.5 Output Stage

The output stage is the passive interface between the inverter switching elements and the user bus. The several key power handling elements in this stage are the output filter and the neutral forming transformer. These elements convert the inverter pole outputs into quality four-wire output power.

2.4.2.6   Inverter Waveform and Output Filter

The three power poles utilized in this design produce a pulse width modulated
waveform that is very rich in the fundamental or 400 Hz, but since it is a
non-linear output, contains harmonics that must be filtered.

The pulse-width modulated waveform is generated by use of a programmed
waveform, generated on the inverter drive logic PC board located in the ICU.
This approach is used because the waveform is fixed and does not need to vary
since system voltage regulation is achieved by control of the DC-link voltage
and not within the inverter itself. In addition, it has been found that
programmed waveforms exist that have superior characteristics than those
generated by an analog method.

Before a particular switching or carrier frequency is selected, there are
certain constraints which must be considered. Among these considerations are
the following:

1. What switching speed and storage times do the power transistors have?
2. What percentage of full load kVA will be circulated in the output filter
   capacitor?
3. What impedance does the filter choke present to the power switches when
   the output is faulted, and what switching frequency will the power poles
   run at during a fault?
4. What minimum switching or carrier frequency will generate a waveform
   devoid of low order harmonics, and which the filter can adequately
   attenuate?

There is a trade-off between switching frequency and filter size. As the
switching frequency increases, the harmonics that are present become higher
frequency and can thus be attenuated with a smaller filter. However, due to
the imperfections in translating from the signal level to the power transistor
level, low order harmonics are reintroduced. Experience has shown that the
delay that must be placed between the off-going transistors and the on-coming

2.4.2.6   Inverter Waveform and Output Filter   (Continued)

transistors (to prevent overlap shoot-through currents) will also reintroduce
these low order harmonics. Therefore, the higher the switching frequency, the
more low order harmonics are introduced. To minimize these effects, a
proprietary circuit has been introduced to compensate for these errors. For
this application, a 3600 Hz switching frequency for the power transistors was
selected. A computer program was utilized to derive the most effective
switching points to minimize the lower order harmonics. This derived program
is stored in PROMS and read out as the basic switching pattern. The projected
(and verified by test on the F-20) system harmonic analysis is given on Table
2.4.2.6-1

2.4.2.7   Neutral Forming Transformer

Inverter systems using a three-phase, full-wave bridge configuration produce
only line-to-line voltages with no neutral available. To obtain a four wire
system with a neutral, a transformer system is required to provide the neutral.

Under balanced loading, no current is supplied by the transformer. With
unbalanced loads, however, load current flows in the system neutral and thus
in the transformer windings. The unbalanced component of the three-phase load
current (neutral current) flows back to the transmission lines through the
transformer windings, dividing nearly equally in each phase winding. It is
necessary to rate the transformer based on the amount of unbalanced load the
system is required to handle. The short term rating must be based on the
single phase short circuit current requirement. The continuous rating of the
transformer must be based on the continuous current unbalance required by the
system. The greater the continuous unbalance requirement, the larger the
transformer rating will be. Therefore, in a system that is weight sensitive,
maintaining balanced loading is quite important.

Table 2.4.2.6-1
90/120 kVA Harmonic Analysis of Inverter Programmed Waveform

F_0 = 400 Hz
Filter Resonance = 4.5 $*F_0$

	UNFILTERED		FILTERED	
N	Amplitude	Percent	Amplitude	Percent
1	1.1812	100.00	1.2420	100.00
3	.1957	16.57	-	-
5	.0006	.05	.0019	.16
7	.0005	.04	.0004	.03
9	.0574	4.86	-	-
11	.0730	6.18	.0147	1.18
13	.0078	.66	.0010	.08
15	.1008	8.53	-	-
17	.1712	14.49	.0129	1.04
19	.1402	11.87	.0083	.67
21	.0098	.83	-	-
23	.1527	12.93	.0001	.49
25	.2597	21.99	.0087	.70
27	.2628	22.25	-	-
29	.1828	15.48	.0045	.36
Total Harmonic Content (Filtered) =			.0242	1.95

Note: All tripleen harmonics
are theoretically
cancelled.

2.4.2.7   Neutral Forming Transformer   (Continued)

In addition to supplying the neutral current, the transformer system tends to balance the line-to-neutral voltage under unbalanced loading. The voltages produced at the converter bridge are generally well balanced. Unbalance in the load terminal voltages will, therefore, be a function of impedance through which unbalanced currents flow to the loads. Aside from the transmission line impedance, the two major components of impedance are the system filter inductor and the transformer impedance (leakage inductance and winding resistance). Here again, the system requirements have a profound effect on the system weight. Because of the impedances of the filter and the transmission lines, a transformer system can only partially balance the voltages owing to load unbalance. Design of the transformer system and the filter thus becomes a compromise depending on the system specification.

Analysis of three transformer systems have been made for comparison. The "T" connected auto-transformer, the "Y" connected transformer with a delta tertiary winding, and the zig-zag connected transformer. All provide similar performance characteristics. Comparison of the kVA requirements of each system determines the best system for use. In each case, the current carried in each phase winding is one-third of the single phase load current.

By mathematical analysis, the three types yield the following kVA factors.

1. "T" Connected Auto-Transformer: Total VA = 1.233 VI_{LOAD} (UNB)

2. Wye Delta Transformer: Total VA = 2 VI_{LOAD} (UNB)

3. Zig-Zag Auto-Transformer: Total VA = 1.155 VI_{LOAD} (UNB)

Comparing the three transformer systems, it is evident that the zig-zag connection requires the lowest volt-ampere rating. Furthermore, the zig-zag connection may be applied using a three-phase core whereas the "T" connection requires the use of two single phase transformers of different designs. The lightest weight system can be obtained using the zig-zag connection.

2.4.2.7   Neutral Forming Transformer   (Continued)

As noted in the above paragraph, the neutral forming transformer can only partially balance the voltages owing to load unbalance. This presents a problem relative to maintaining the voltage within the prescribed levels for a 1/3 load unbalance, as specified in paragraph 3.3.1.1 of MIL-E-23001B. This problem can best be understood by putting it in the proper perspective. MIL-E-23001B is a specification which covers a type of VSCF system, namely a cycloconverter. Due to the nature of cycloconverters, they are individually phase regulated and as such can control each phase voltage as well as angle. The DC-link VSCF as embodied in this design (and the designs now being used on the referenced airplanes) is the simplest embodiment of a three-phase inverter. That is to say there are but three power poles switching at predetermined points which create balanced three-phase voltages at the pole outputs.

These patterns never change. If the load currents drawn by individual phases vary, then the drops in the filter inductor and neutral forming transformer become unbalanced. When these drops are considered we see that the output voltage is unbalanced, and the degree of unbalance is based on the internal impedances. This is a direct analogy to a standard rotating generator system.

There have been studies conducted to try to overcome this problem in these simple three-phase inverter designs. Such things as modification of switching pattern and addition of a fourth pole have been conceived. Performance and complexity plague these concepts as solutions. It must be pointed out that to accomplish individual phase regulation with a DC-link system of the type presented would require an almost doubling of complexity; (i.e., it would require six power poles with all their control and protection). It is felt that the increase in size, weight, and complexity far outweighs the penalty associated with the unbalanced voltage.

The specification which is in use for new aircraft power systems is MIL-G-21480A. The following table (Table 2.4.2.7-1) gives voltage balance and phase angle requirements for unbalanced and balanced load requirements.

2.4.2.7   Neutral Forming Transformer (Continued)

Therefore, the typical range of voltages for a 1/3 load unbalance might be
112.7, 115, 117.3.

It is seen that this exceeds the specification limits of MIL-E-23001B which
has a range of 114 - 116.5 volts.

A change in specification requirements relative to load unbalance is
recommended, and that it be in line with the requirements of MIL-G-21480A as
listed above.

2.4.2.8   Inverter Sensing Circuits

Included in the power stage are sensing elements required for inverter control
and protection, as well as system protection. These elements and their
functions are listed below.

1. DC-link Voltage Sensing: This voltage is sensed so the DC-link
   overvoltage protection can be implemented, and as a sensing input control
   of the DC content in the inverter output.

2. Pole Output Current Sensing: This is provided by a double core current
   transformer and included in the output of each power pole. The burden and
   associated components are also located in the inverter. This current
   transformer output is used to limit the peak current provided by any power
   pole, and is supplied to the controls, such that an instantaneous reversal
   of polarity at the pole output is achieved when current limit is reached.

3. Feeder Fault Sensing: The outputs of these three CTs when combined with
   the outputs from the remotely located CTs provide information to the
   controls so that a feeder fault is recognized and protective action can be
   taken.

Table 2.4.2.7-1
Voltage Balance and Phase Angle Requirements

LOAD	PHASE VOLTAGE BALANCE	ANGLE
Balanced	±.5% of 3-Phase Average	120 ±.6°
1/6 UNB	± 1% of 3-Phase Average	120 ± 1°
1/3 UNB	± 2% of 3-Phase Average	120 ± 2°
2/3 UNB	± 4% of 3-Phase Average	120 ± 4°

2.4.2.8   Inverter Sensing Circuits   (Continued)

4. Generator-Inverter Ground Fault Sensing: This current transformer is coupled by all three lines feeding the load.   If a fault occurs within the pre-regulator-inverter system, this device will transmit a voltage to the proper protective function.

5. Paralleling Control and Protection: Current and potential transformers are included in the output stage so that paralleling of individual systems can be accomplished.   Separate sets of components are provided for protection when paralleled.

6. Pole Waveform Sensing: Each pole is sampled by resistor feedback and sent to the inverter drive logic to make waveform correction changes to limit DC content and eliminate errors generated by delays in switching in the power poles.

The inverter output voltage is sensed at the point-of-regulation (POR) and is thus not one of the internal feedbacks.

2.5   Inverter Control Unit (ICU)

The inverter control unit includes the controls and logic for the 400 Hz system.   It monitors the input and output power quality and takes appropriate action when limits are exceeded.   The ICU is composed of the following four modules:

    1.   Protection Module
    2.   Inverter Drive Logic Module
    3.   Link Regulation Drive Module
    4.   Power Supplies

2.5.1 Protection Module

The protection module supervises the operation of the input contactor (GBA), monitors input power quality, provides a run signal to the inverter, detects faults and takes action to minimize system disturbances, regulates the output voltage, .itors the output power quality, and supervises the operation of the 400 Hz output contactor (LB).

2.5.1.1 Input Contactor Control (Refer to Figure 2.5.1-1)

The control switch is used to control the input contactor. The switch has three positions. When the switch is set to OFF, the input contactor (GBA) will not close because gate U5D does not provide a logic "1" input to gate U4C.

If GBA was closed when the control switch was moved to OFF, gate U4B provides a logic "1" to U18E, which causes transistors Q13 and Q14 to conduct and trip GBA.

The GCU provides a grounding signal to the ICU via input 68 when conditions are correct for closing GBA. This sig.il is inverted by U5A and presented to one input of gate U4C. If the control switch is in the TEST or ON position and no faults exist, gate U5D supplies a logic "1" to the other input of gate U4C. Gate U4C provides a logic "0" signal to gate U4D, which inverts the signal to cause transistors Q1 and Q2 to conduct and close GBA. Although the inverter is now receiving power, its drive circuits are inhibited until the input voltage has been checked.

2.5.1.2 Input Undervoltage

All six phases of input power must be present for the inverter to function properly. This is accomplished by the input undervoltage circuit. Transformers T1, T3, and T5 sense the line-to-line voltage of one three phase input. Transformers T2, T4, and T6 sense the line-to-line voltage of che three-phase input that is displaced by 30°. The output of each transformer pair (T1-T2, T3-T4, and T5-T6) are summed, rectified, and filtered.

INPUT UNDER VOLTAGE

VOLTAGE REGULATOR SENSING

LINK SUPPRESSION

POR SENS

SOFT REFE

INPUT FAULT PROTECTION

DC CONTENT

EXTRANEOUS FREQUENCY

FROM INVERTER OUTPUT
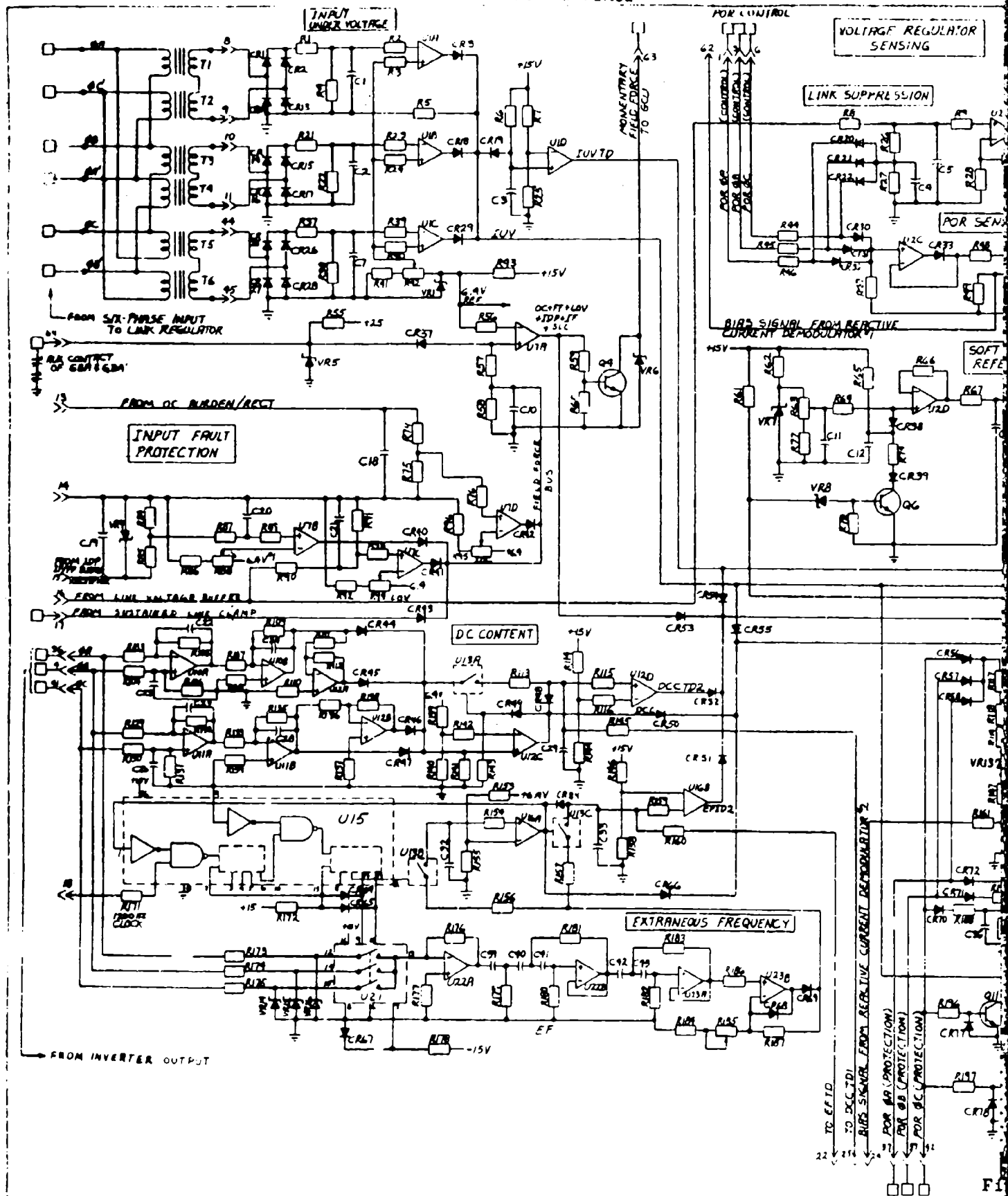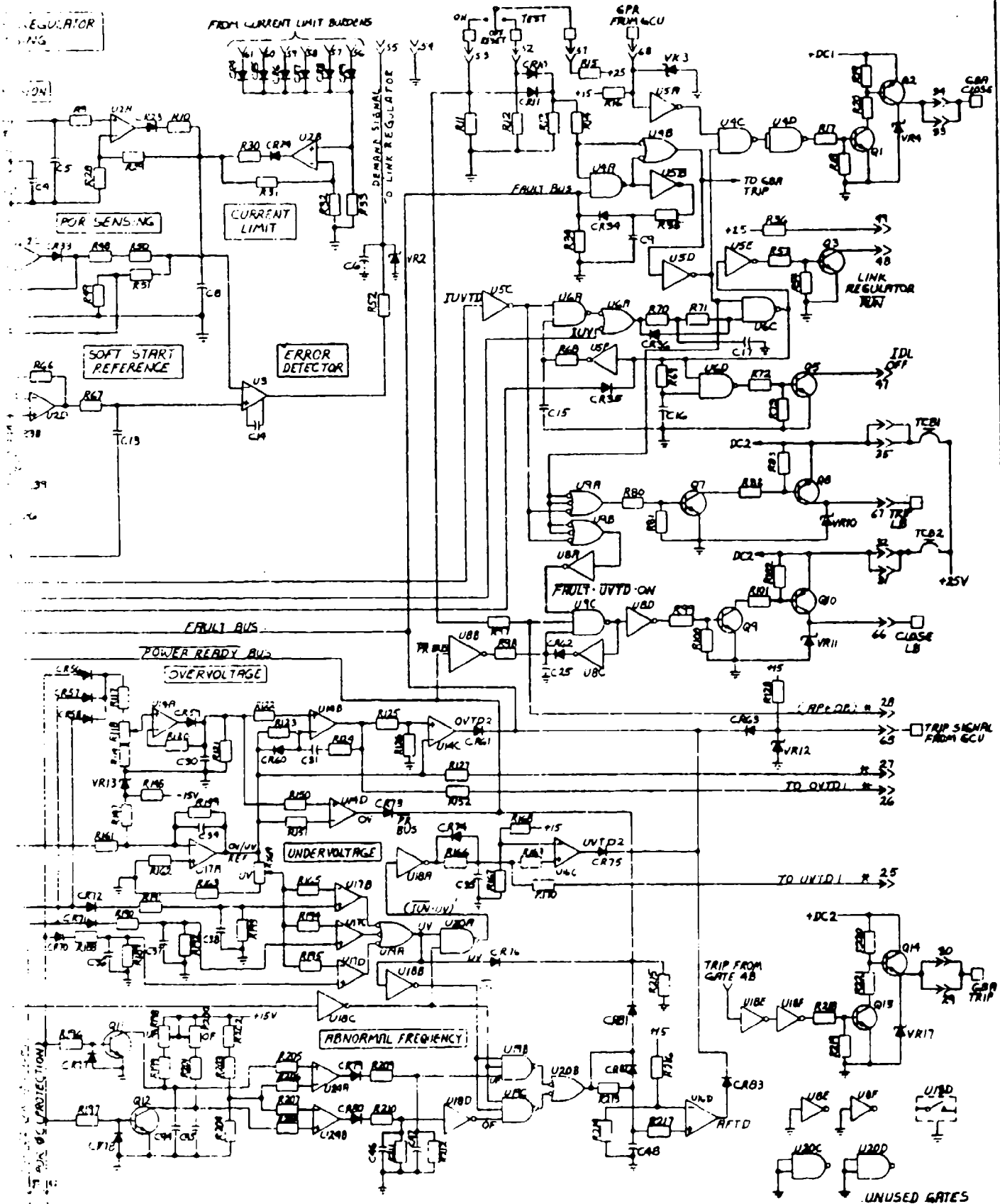
Figure 2.5.1-1

ICU Schematic

* SIGNALS FOR CONTROL & PROTECTION OF PARALLEL CHANNEL

SCHEMATIC FOR 400 Hz CONTROL & PROTECTION, ICU

449E259

2-83/2-84

2.5.1.2   Input Undervoltage   (Continued)

The resulting dc voltages that appear across C1, C2, and C7 are compared to a reference by U1A, U1B, and U1C. The reference is developed by the circuit composed of R41, R42, R43, and VR1, a temperature compensated zener diode. If all six phases are greater than 130 volts L-N, a logic "0" will be present at the outputs of U1A, U1B, and U1C. These outputs are "OR-ED" by CR3, CR18, and CR29. This signal is routed to gate 6A. If the IUV signal is a logic "0", gate 6A will initiate a 150 ± 50ms time delay. The time delay is composed of R70 and C17. After the time delay has elapsed, a logic "1" will be presented to one input of gate 6C. The other input of gate 6C is already at a logic "1" if no fault signals exist and if the control switch is in either the TEST or ON position.

Three events occur after normal input voltage has been sensed by the inverter for 150 ± 50ms:

1. The link regulator gate drive is enabled.
2. The inverter drive logic is enabled.
3. The "soft-start" voltage reference is initiated.

The signal to initiate these events is a logic "0" at the output of U6C. The delay is provided to allow time for the link regulator controls to initialize. The link regulator is enabled when Q3 conducts. The LED of a photo transistor in the link regulator controls is connected between output terminal 48 and 49. Isolation is required since the power supplies of the link floats with respect to the power supplies of the control and protection module.

The "soft-start" reference is initiated when VR8 stops conducting. When transistor Q6 stops conducting, current through R64 and R65 charge C12 towards 15 volts. Thus the voltage at the (+) terminal of U2D ramps up. Diode CR38 is back biased when the C12 voltage exceeds the reference level set by R64. The "soft-start" circuit reduces build-up transients.

2.5.1.2   Input Undervoltage   (Continued)

The inverter drive logic is initiated when Q5 conducts.

To prevent normal input voltage transients from starting and stopping the
inverter, a "seal-in" connection is made from the output of gate U6C via gate
U5F to an input of gate U6A. The "seal-in" is broken by an output from the
input undervoltage time delay (IUVTD).

2.5.1.3   Voltage Regulator

The voltage regulator senses the three-phase to neutral voltages at the
point-of-regulation, compares these voltages to a fixed reference level, the
output being used to control the DC-link regulator.

2.5.1.3.1   Point-of-Regulation (POR) Sensing Voltage

The three-phase line-to-neutral voltage from the POR is applied through three
isolating resistors (R44, R45, R46) to the rectifier (CR30, CR31, CR32). The
voltage across R47 is proportional to the three-phase average voltage at the
POR. This voltage is applied through a voltage follower (U2C) to an
averaging-type R-C filter. At nominal voltage, the output of the filter is 5
volts dc with approximately 100 mv of 1200 PPS ripple superimposed upon it.
This is applied to the (-) input of comparator U3. The ripple voltage is used
to establish voltage regulator gain.

2.5.1.3.2   Voltage Reference

Reference voltage for the regulator is obtained from a temperature-compensated
zener diode (VR7). An internal multi-turn potentiometer (R63) is used for
adjustment of the reference voltage to obtain a dc voltage equivalent to 115
volts L-N. The soft-start feature was discussed in paragraph 2.5.1.2.

2.5.1.3.3   Voltage Comparator

The dc voltage from the sensing circuit is compared with the reference
voltage. The output of comparator (U3) is a pulse-width-modulated (PWM)
square wave-voltage operating at 1200 PPS. The duty cycle of this square wave
is a function of the error between the POR voltage and the reference voltage.
When the sensed voltage decreases, the duty cycle increases toward 100%. This
signals the link regulator to increase its voltage output. A nominal 20ms
filter composed of R52 and C6 averages the PWM signal and sends it to the
analog voltage isolater in the dc-link regulator control module via terminals
54 and 55.

2.5.1.3.4   DC-Link Voltage Suppression Circuit

If a fault condition occurs on the system output that results in line current
exceeding two per unit, the inverter logic limits the maximum output current
from the inverter. The POR voltage will be determined by this current and the
fault impedance and will result in a POR voltage of less than 115 volts. A
lower dc-link voltage is needed to maintain this system output voltage. To
reduce stress on the inverter power transistors in this operating mode, a
dc-link voltage suppression circuit is included in the voltage regulator. For
normal operating conditions this circuit output (U2A) is below the POR sensed
voltage at the voltage regulator comparator input, so it has no effect on
operation. When the dc-link voltage exceeds 300 volts and the POR is 115
volts L-N, a signal is supplied through an OR-ing diode (CR23) to reduce the
voltage regulator output and the dc-link suppression circuit through a
three-phase half-wave rectifier circuit (CR20, CR21, and CR22). The dc-link
voltage is decreased proportional to the POR voltage down to a minimum value
of 100 volts dc on the link for a short circuit condition on the system output.

In addition, the dc-link voltage suppression circuit suppresses the link if a
POR sensing lead opens.

2.5.1.3.5   Output Current Limiting

The inverter senses output current with center-tapped current transformers.
The rectified currents develop three full-wave voltage signals proportional to
output line current. These signals are used by the inverter to maintain the
output transistors in their safe operating area until the link voltage can be
controlled at a lower level.

The voltage signals from these current limit burdens are "OR-ED" by CR4, CR5,
CR6, CR7, CR8, and CR9 and applied to the peaking amplifier (U2B). When the
output current exceeds 550 ± 25 amperes per phase, a limit signal is "OR-ED"
into the signal proportional to POR voltage by CR24. This signal then
maintains the short circuit current at 550 ± 25 amperes by decreasing the
demand signal to the link regulator.

Computer simulation indicates that the voltage regulator will assume control
of the current within eight cycles. During the first eight cycles, the
inverter drive circuit will keep the output transistors within the
safe-operating area.

2.5.1.3.6   Reactive Load Division

A signal proportional to differential reactive current is impressed across
R49. This signal modifies the demand signal to balance reactive current when
the channel is paralleled with another channel.

2.5.1.4   Output Power Ready

Before the line contactor (LC) can be closed, the power quality must be within
specified limits. This condition is signaled by a logic "0" at the input to
U8B. The power ready (PR) bus collects this information. The power quality
signals are collected from extraneous frequency (EF) sensing by CR66, direct
current content (DCC) sensing by CR50; input undervoltage (IUV) sensing by
CR55; overvoltage (OV) sensing by CR73; undervoltage (UV) sensing by CR76; and
abnormal frequency (AF) sensing by CR81. The output of all these sensing
circuits must be a logic "0" before the LC can be closed.

2.5.1.4   Output Power Ready (Continued)

Gate 9C must have all its inputs at logic "1" before the LC can be closed. These three inputs are: power ready from gate 8B; FAULTS' and IUVTD' and control switch ON from U8A; and ON from the control switch. It should be noted that the ON signal is inhibited by a grounding signal from terminal 28 unless the load bus is dead or conditions exist for paralleling.

Once the proper conditions have been established for closing the LC, the power ready input is sealed in via U8C. This seal-in is provided to prevent the LC from responding to normal transients. The seal-in is broken when a fault is sensed or when the control switch is moved from ON.

After all conditions have been established, gate U8D inverts the output of U9C. Transistors Q9 and Q10 close the LC.

2.5.1.5   Faults

The fault bus is an input to gate U4A. If a fault signal appears while the control switch is in the ON or TEST position, an output (logic "1") is present at the output of gates U4B and U5B. The output of gate U5B seals in the fault signal to provide the required anit-cycling feature. The signal at the output of gate U4B trips GBA if it is closed or inhibits its closure if it is open via the connection to U4C. The fault signal inhibits the link regulator by reducing the output of U5E to a logic "0". The fault signal also reduces the power demand signal to zero via CR35.

Gate U6C also initiates turn-off of the inverter drive logic (IDL) when a fault is present. The turn-off is delayed by 150 ± 50 ms by R69 and C16. This delay allows the inverter to run until the dc-link is discharged.

Gate U9A responds to the fault signal by tripping the load breaker (LB). Gate U9B inhibits the closure of the LB via gates U9C and U8D.

2.5.1.5.1 Fault Current Protection Sensing

Figure 2.5.1-2 shows the current transformer/burden resistor/rectifier configuration used to selectively clear input and output faults in the 400 Hz system and its feeders. The current transformer loop from the input side of GBA and GBA' to the converter/inverter input is used to sense input differential protection and input overcurrent. The voltage proportional to input current is developed across R1 through R6 and rectified by diodes CR1 through CR6.

The signal proportional to input differential current developed across R7 through R12 is rectified by diodes CR7 through CR12. If the differential fault is between GBA/GBA' and the converter/inverter, the ICU will open GBA/GBA' before the GCU senses the fault and de-excites the generator. The GCU will de-excite the generator if the fault is before GBA/GBA'.

The zone for output feeder fault protection is from the inverter output to the load side of the LC. The signal proportional to output feeder fault current developed across R19, R20, and R21 is rectified by CR12, CR13, and CR14.

The current in the four output lines of the inverter is summed to detect ground faults in the converter/inverter package. The current signal proportional to inverter ground fault current developed across R22 is rectified by CR13.

The dc signals proportional to fault current are routed to the control and protection printed wiring assembly (PWA) via terminals 1 and 2.

These signals enter the control and protection PWA (Figure 2.5.1-1) on terminals 13 and 15. The overcurrent signal is peak filtered by C18 to obtain highest phase sensing. When the overcurrent limit is exceeded, the output of comparator U7D goes to a logic "1" and changes C10 rapidly. When the (+) input of U7A exceed 6.4 volts, U7A has a logic "1" output, which is "OR-ED" into the fault bus by CR53.
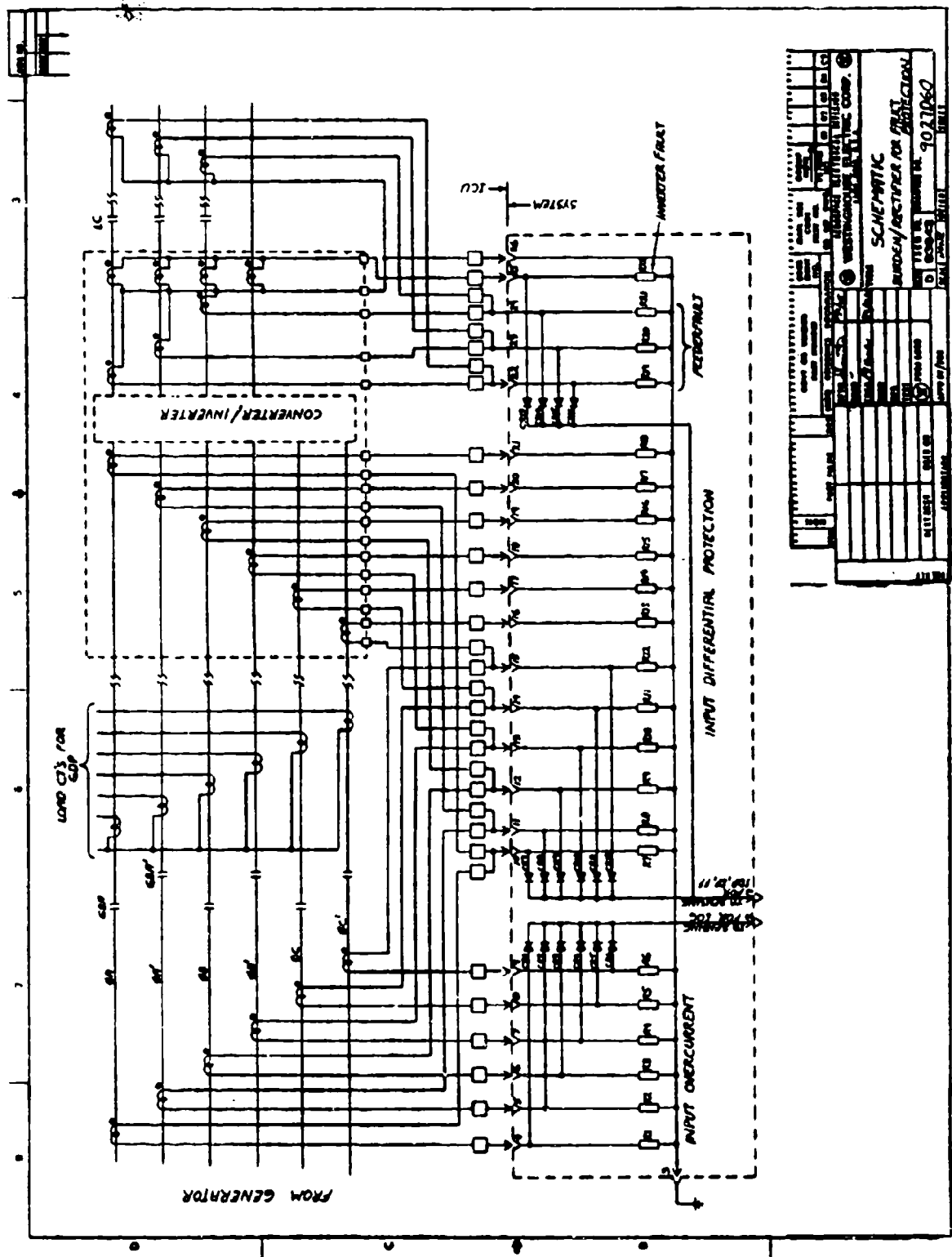
Figure 2.5.1-2

Current Transformer Loops and Burden Impedances

2.5.1.5.1   Fault Current Protection Sensing   (Continued)

Input overcurrent is one of a class of faults that must be cleared very
rapidly to prevent system and component damage. The other faults which fall
into this classification are input differential protection, inverter fault,
feeder fault, link overvoltage, and sustained link clamp. In a conventional
system with a dedicated generator, the fault would be de-exciting the
generator. In this system, the generator cannot be de-excited to clear the
fault since it supplies other loads. The fault is cleared after approximately
20 milliseconds by opening GBA/GBA'. In order to get a faster reaction to
this class of faults, a momentary field force signal is sent to the GCU.
Capacitor C10 is charged when any of these faults is sensed. The output of
U7A causes Q4 to conduct. This initiates field forcing of the generator.
Field forcing is terminated when GBA and GBA' are both open. This does create
a 20ms disturbance on the system which, while not desirable, is preferable to
damaging system components.

Capacitor C19 is charged to a level proportional to the highest fault current
sensed for input differential protection, inverter fault, or feeder fault.
Comparator U7B has an output when the highest fault current exceeds 10 ±5
amperes. This signal is "OR-ED" into the field force bus by CR40.

2.5.1.5.2   Sustained Link Clamp

The inverter includes a circuit that clamps the link voltage to less than 340
volts during normal transients resulting from load switching or fault
removal. It also clamps the link voltage if the link regulator fails in the
maximum demand mode. If the link is clamped for a period exceeding 100
milliseconds, the inverter sends a signal to the ICU that is "OR-ED" into the
field force bus by CR43.

2.3.1.5.3   Link Overvoltage

This protection is included to prevent further system damage if the link regulator fails in the maximum demand mode and the link clamp allowed the voltage to exceed 340 volts. A differential amplifier located on the inverter drive logic (IDL) PWA with a gain of 1/50 converts the link voltage to a dc signal that is referenced to sensing ground. When the magnitude of the link voltage exceeds 350 ± 10 volts dc, comparator U7C has an output that is "OR-ED" into the field force bus by CR41.

2.5.1.5.4   DC Content

To obtain selective tripping of a parallel channel that has a dc content error, the point of sensing is at the inverter terminals rather than at the POR. Because of the DC resistance in the feeders and synchronizing bus, the magnitude of the sensed signal will be greater at the terminals of the faulted channel than it will be at the terminals of the properly functioning inverter. Inverse time delays will isolate the faulted channel.

Two integrating circuits are used. The balanced integrator composed of U10A and associated components sense the line-to-line dc content of phase A and phase B. The second stage integrator is composed of U108B and associated components. The AC gain of the two stage integrator is 174×10^{-6} while the dc gain is 27. The phase B-to-phase C line voltage is integrated by U1A/U11B and associated components. Unity gain amplifiers U12A and U12B invert the outputs of the integrators to obtain the absolute magnitude of the fault. Diodes CR44, CR45, CR46, and CR47 apply the highest signal to comparator U12C.   When the dc content exceeds 0.200 ± .050 volt, the output of U12C turns on analog gate U13A. This applies a voltage proportional to the fault magnitude to charge C29 through R113.

2.5.1.5.4   DC Content (Continued)

The voltage across C29 is an inverse time function of the absolute magnitude
of the fault. This capacitor voltage is compared to two different references
by the DCCTD1 and the DCCTD2 comparators. DCCTD1 (located on the paralleling
PWB) has a threshold that is 50% of the threshold of DCCTD2. Thus, it will
provide a trip signal to the bus tie breaker before DCCTD2 supplies a signal
to the fault bus via CR52. After the faulted channel trips off-line, the BTB
will reclose.

2.5.1.5.5   Extraneous Frequency

Extraneous frequency is sensed at the inverter terminals rather than at the
POR so selective isolation of a faulted parallel channel can be achieved. A
multiplexed five-pole high-pass active filter attenuates the fundamental
frequency. In the pass band, the filter gain approaches unity.

Integrated circuit U15 is a dual binary counter. It is driven by a 1200 Hz
clock from the IDL PWA. The counter drives a four-channel analog multiplexer
(U21). The three channels used have the binary addresses (0,0), (1,0), and
(0,1). The unused channel has the binary address (1,1). Each channel is
selected for 0.107 second. After the third phase has been sampled, the
counter advances to the state where pins 13 and 14 of U15 are both at a logic
"1". Diodes CR64 and CR65 are back biased. This applies a reset signal to
the counter that sets up the multiplexer to sample phase A.

As the multiplexer steps from phase to phase, it takes a finite time for the
switching transients to subside. Analog switch U13B is maintained in the open
state for 0.053 second after a phase is selected. During the remainder of the
period, the output of the filter is connected to capacitor C32. If the
voltage on C32 exceeds the threshold of comparator U16A, the phase scanning is
terminated and the multiplexer locks onto the phase that has an extraneous
frequency signal. The lock-on signal goes to pin 1 of U15.

2.5.1.5.5   Extraneous Frequency   (Continued)

The output of the multiplexer is isolated from the filter by the unity gain
amplifier composed of U22A and associated resistors. The five-pole, high-pass
active filter is composed of U22B, U23C, C39 through C43, and R179 through
R183.

A precision half-wave rectifier composed of U23B and associated components
develops a dc signal proportional to the magnitude of extraneous frequency.
Analog gate U13B allows this voltage to charge C32 through R156 during the
last half of the sampling period. Comparator U16A will have an output when
the sensed voltage exceeds the threshold. When a fault is sensed, analog
switch U13C starts to charge time delay capacitor C33 through R157. The rate
at which the capacitor charges will be proportional to the fault magnitude.
The capacitor voltage is compared to two thresholds by EFTD1 (located on
paralleling PWA) and by EFTD2. The threshold for EFTD1 is 50% of the
threshold for EFTD2. Thus, EFTD1 will reach its threshold and trip the BTB
before EFTD2 shuts down the 400 Hz channel. If the fault exists after the
channel is isolated, EFTD2 will time out and energize the fault bus via CR51.
After the LC opens, the BTB will reclose.

The response of the extraneous frequency sensing circuit is shown on Figure
2.5.1-3 The filter passes all frequency components in the pass band so the
resulting output is the algebraic sum of all components. Since total harmonic
content is defined as the square root of the sum of the squared magnitudes, a
circuit that is calibrated by a single pure harmonic will be more sensitive to
the total harmonic content of a waveform that contains two or more harmonics.
This must be taken into consideration when the calibration procedure is
established.
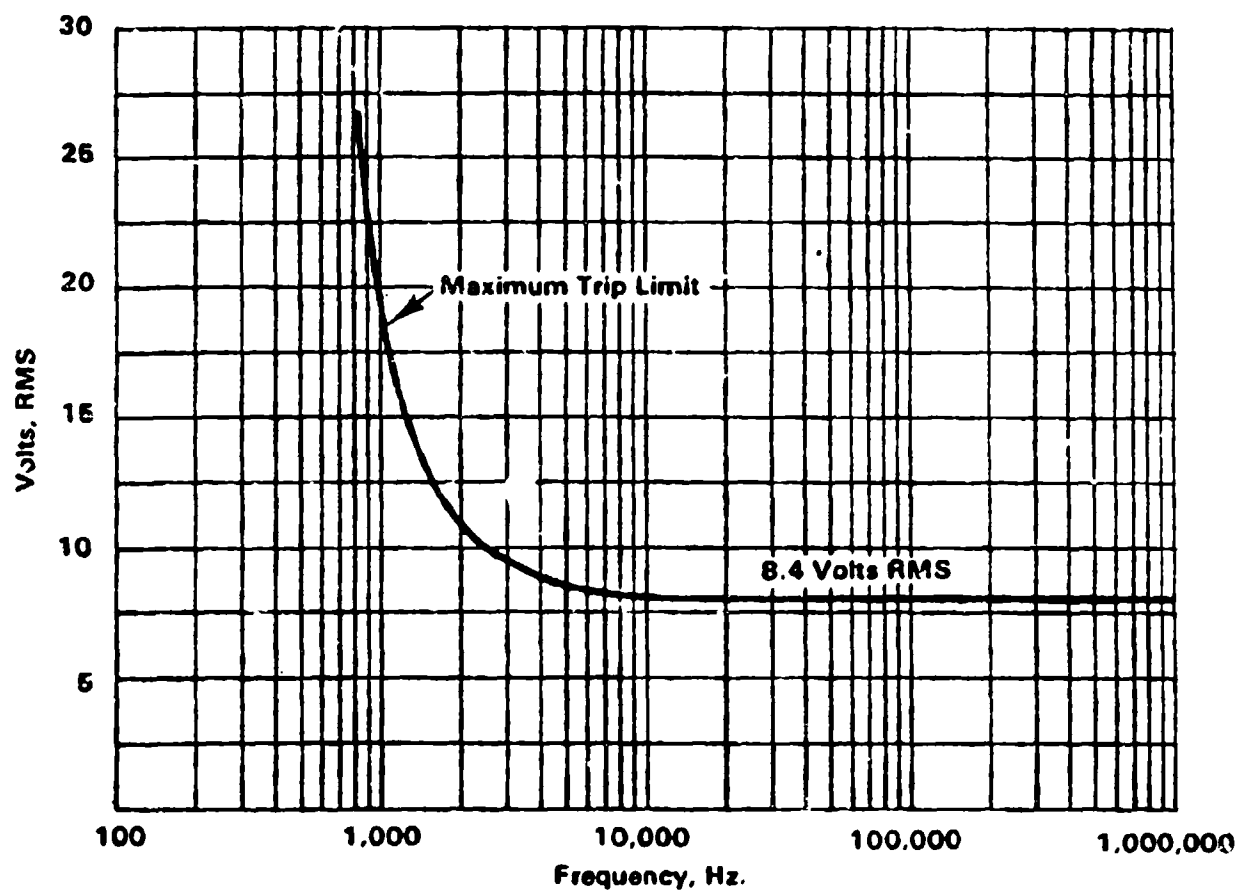
Figure 2.5.1-3

Response of Extraneous Frequency Sensing Circuit

2.5.1.5.6   Overfrequency Frequency

Resistor R197 and transistor Q12 discharge C45 during the positive half cycle and allows it to charge through R200 and R201 during the negative half cycle. At normal frequency, the capacitor voltage exceeds the threshold at the (-) terminal of comparator U24B near the end of the negative half cycle. Capacitor C46 is charged through CR80 and current limiting resistor R210. The ratio of R210/R211 gives the circuit a short charge time constant and a long discharge time constant.

If the frequency increases to the overfrequency trip limit, the capacitor (C46) does not charge to a value which is high enough to exceed the U24B threshold, so capacitor C46 does not get refreshed each cycle. The capacitor discharges until it is below the threshold of U18D, and an overfrequency (OF) signal is present at an input to U19C. The other inputs to U19C lock out OF protection unless input and output voltages are normal. If all three inputs are present at U19C, the OF time delay capacitor C48 is charged through R213. After the time delay, comparator U16D puts a signal on the fault bus via CR83.

2.5.1.5.7   Underfrequency Protection

The underfrequency sensing is similar to the overfrequency sensing circuit described in the preceeding paragraph. During conditions of normal frequency, the voltage on capacitor C47 does not reach a high enough value to exceed the threshold at the (-) input of U24A during the negative half cycle. When the frequency drops to the underfrequency limit, comparator U24A charges C47 and initiates the abnormal frequency time delay.

2.5.1.5.8   Undervoltage

Diodes CR70, CR71 and CR72 half-wave rectify the voltage from the POR. Three voltage dividers/filters develop scaled dc voltages that are proportional to the line-to-neutral voltages at the POR. These scaled voltages are compared to a reference by U17B, U17C, and U17D. When any or all of the three phases

2-97

2.5.1.5.8   Undervoltage (Continued)

drop below 107 ± 2 volts L-N, gate U19A presents a logic "1" to an input of
U20A. If there is no input undervoltage, gate U18A charges time delay
capacitor C35 through R166. The voltage across C35 is compared to two
thresholds by UVTD1 (on paralleling PWB) and UVTD2. The threshold of UVTD1 is
50% of the value of the threshold of UVTD2. Thus, UVTD1 will operate before
UVTD2 and isolate the faulted channel by opening the BTB. If the fault
persists, UVTD2 will time out and shut down the faulted channel. The BTB will
then be reclosed.

It should be noted that the reference amplifier composed of U17A is biased by
a signal from the reactive current demodulator located on the paralleling
PWB. This bias signal lowers the reference on the faulted channel and raises
the reference on the unfaulted channels. Thus, the faulted channel can be
selectively isolated.

2.5.1.5.8   Overvoltage

The three phase voltage from the POR is half-wave rectified by CR56, CR57, and
CR58. After the voltage is scaled by R117 and R119, it is peaked by U14A,
CR59, R119, and C30. A portion of this voltage is applied to the (+) inputs
of comparators U14B and U14D. When the voltage at the (+) input of U14D
exceeds the reference voltage, a signal is "OR-ED"into the PR bus by CR73.
When the voltage at the (+) input of U14B exceeds the reference voltage, the
output of U14B begins to rise at a rate that produces a current in C31 that is
equal to the current through R122. The current through R122 is proportional
to the magnitude by which the sensed voltage exceeds the reference voltage.
Thus, the time required to get an output from U14C is inversely proportional
to the magnitude of the overvoltage. The minimum pick-up of overvoltage is
122.5 ± 2.5 volts. The inverse time delay responds to the fault within the
maximum time voltage characteristic of MIL-E-23001B, Figure 2.

2.5.1.5.8   Overvoltage (Continued)

The paralleling PWA includes a time delay comparator (OVTD1) that is designed to trip the BTB before OVTD2 energizes the fault bus via CR61.

2.5.1.6   Parallel Protection (Refer to Figure 2.5.1.6-1)

2.5.1.6.1   Reactive Load Division (Control)

A signal proportional to differential current is impressed across burden resistor R1 and the primary of transformer T1. Gates U4A and U4B, in conjunction with analog switch U1, demodulate the signal proportional to differential current. Since the switching signal lags the current signal by 90°, a voltage signal proportional to the imaginary component (reactive) of current appears at the output of integrater U3A. This signal biases the voltage sensing circuit on Figure 2.5.1-1 in a manner that will reduce the reactive load division error toward zero.

2.5.1.6.2   Reactive Load Division (Protection)

A circuit identical to the control circuit is used to bias over/undervoltage protection. This circuit is composed of R2, T2, U4C, U4D, U2, and U3B. The gain of the protection circuit is matched to the gain of the control circuit. As a result, the unfaulted channel senses an apparent normal voltage while the faulted channel senses a voltage error and will trip its BTB via overvoltage protection (OVTD1) or undervoltage protection (UVTD1).

2.5.1.6.3   Dead Bus/Auto Paralleling

This circuit inhibits the closing of LC unless the synchronizing bus is dead or the slip frequency is less than 3 Hz. If the synchronizing bus is dead, transistor Q2 is on continuously. Thus, capacitor C5 does not charge and comparator U5A has continuous output.

REACTIVE DEMODULATORS

FROM DIFFERENTIAL REACTIVE CONTROL LOOP

FROM DIFFERENTIAL REACTIVE PROTECTION LOOP

REACTIVE BIAS FOR CONTROL

REACTIVE BIAS FOR PROTECTION

DEAD BUS / AUTO PARALLELING

PHASE ANGLE ERROR DECTECTOR

FROM REAL CURRENT ERROR DETECTOR

FROM ANGLE ERROR DETECTOR
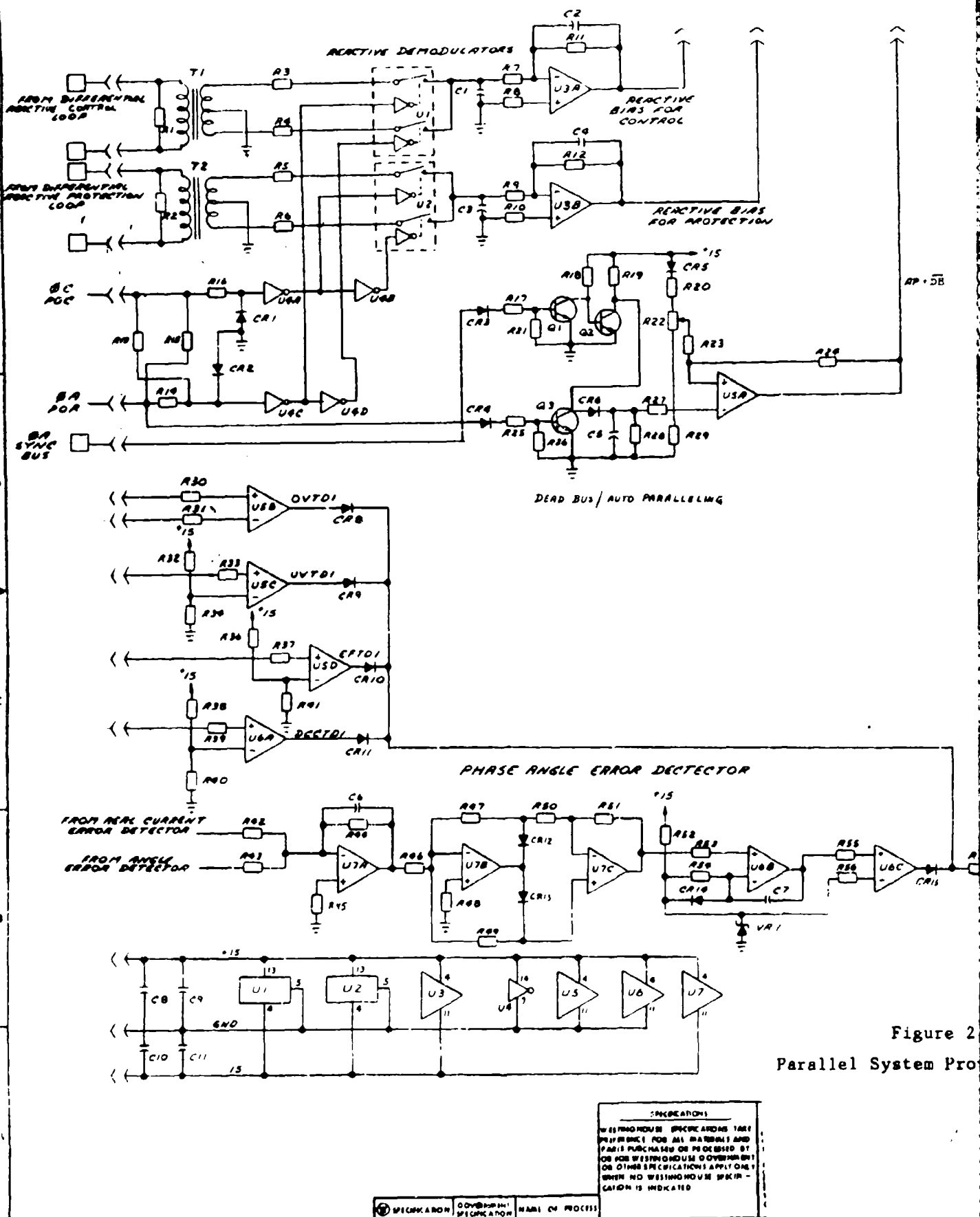
Figure 2

Parallel System Pro

1012
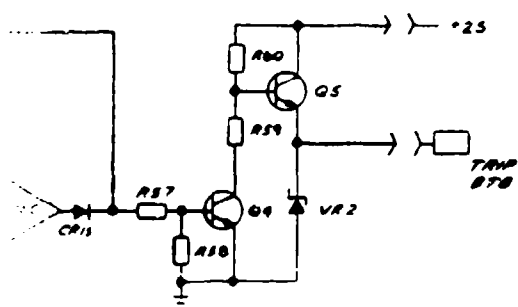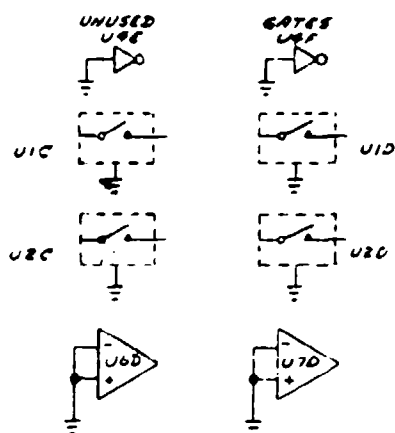
Figure 2.5.1.6-1
stem Protection, 400 Hz AC

2.5.1.6.3   Dead Bus/Auto Paralleling (Continued)

The R19/C5 time constant is designed so that if the slip frequency exceeds 3 Hz, the voltage at the (-) input of U5A remains above the (+) reference and a paralleling output is not produced at the output of U5A. If the slip frequency is less than 3 Hz, the (-) input to U5A drops below the reference, and a paralleling output is produced at the output of U5A. The pulse occurs when the phase angle difference between the two sources is near zero. The network composed of R22, R23, and CR5 lengthens the output pulse to ensure that the paralleling signal is long enough to close the LC.

2.5.1.6.4   Phase Angle Error Detector

In constant speed drive systems, selective isolation of a parallel channel not dividing real load properly is achieved by biasing abnormal frequency with a signal proportional to differential real current. In the VSCF system this approach is not effective because all channels in the system are controlled by the same frequency reference. Selective isolation in a parallel VSCF system is achieved by detecting phase angle error. This is accomplished by summing the phase angle error and the differential real current error by U7A. Amplifiers U7B and U7C and associated components develop the absolute magnitude of the phase angle error. Amplifier U6B and comparator U6C form a time delay that has an inverse time-voltage characteristic.

2.5.1.7   BTB Trip Circuit

Five time delays (OVTD1, UVTD1, EFTD1, DCCTD1 and the phase angle error time delay) provide a signal to trip the BTB by making Q4 and Q5 conduct. The first four of these time delays have a complementary time delay for isolated control and protection. The time delays to trip the BTB have thresholds that are 50% lower than the complementary time delays that trip the LC. This allows the BTB to trip before the LC trips. If the channel still exhibits an abnormal condition after the BTB trips, the LC will trip. The BTB is reclosed to supply power to the load.

2.5.2 Inverter Drive Logic Module

The inverter drive logic module used for this system was developed for the F-20, 40 kVA VSCF system. The circuit provides the three-phase pulse-width modulated signals that control the inverter output transistors. The number and width of the pulses was chosen to minimize inverter dissipation, distortion, and output filter weight.

The program to generate the waveform is stored in a read-only-memory. The counters that decode this waveform are driven from a voltage controlled oscillator (VCO) rather than from the crystal controlled clock used in the F-20 system. The VCO is required because the phase angle must be controlled to balance real load between paralleled channels. In addition, this system is required to slave to an external source so that momentary paralleling can be achieved without losing power to the load.

In addition to providing the waveform during normal operation, this module must modify the waveform to control direct current content and protect the power transistors during the first few cycles of short circuit current.

2.5.3 Link Regulator Drive Module

The dc link regulator drive module provides the demand signal to the dc link pre-regulator. The various sensing elements that generate the demand signal were presented in Section 2.5.1.3 (Voltage Regulators).

The sensed signals, compared to a reference provide the output to which the pre-regulator circuit responds to provide 400 Hz system output control.

2.5.4 Power Supply

The ICU requires two power supplies. The power supply for all functions except the link regulator is shown schematically on Figure 2.5.4-1. The power supply for the link regulator is identical, except that it is isolated from logic ground, requires a 32 volt rather than a 25 volt output, and does not require the 5 volt supply.

Figure 2.5.4-1

Schematic Diagram of ICU Power Supplies

25 Volt DC Regulator

The 25-volt regulator consists of the input transformer T1, rectifier bridge CR501; input filter L501, C501, C502, C503, and C504; switching transistors Q501, Q502 and Q503; free-wheeling diode CR502; and output filter L502, C505, and C506.

U501 is an LM10 operational amplifier configured to keep the pulse-width modulated voltage regulator (U502) shut down until the rectified voltage exceeds 37 volts. Once the 25-volt regulator is running, a 15-volt signal through R511 provides hysteresis so that U502 does not shut down until the rectified voltage drops below 32 volts.

Transistor Q505, in conjunction with VR503, provides a regulated voltage to U501 and U502 during start-up. After the 25-volt regulator is running, U501 and U502 are powered from the 25-volt bus through CR505.

The LM1524 (U502) has an internal voltage reference that is adjusted by selecting the value of R533. The switching rate is fixed by the values of R524 and C517. Resistor R523 and capacitor C527 are the compensation components. The voltage sense feedback is developed by the voltage divider consisting of R518 and R526. Shunt resistors R561 and R562 provide the current limiting signal to pin 5 of U502.

When a voltage error is sensed, transistors Q501 and Q502 start switching with a maximum duty cycle of 90°.

Filter capacitors C505 and C506 charge until the sensed voltage exceeds 25 volts, at which time Q501 and Q502 stop switching. Free-wheeling diode CR502 provides a path for inductor L502 current while the switching transistors are off. The 10% minimum off time prevents inductor saturation. If a switching transistor fails, or the controls fail to regulate voltage, zener diode VR501 (36v) protects the utilizing circuits from excessive voltage.

15 Volt Regulated Supply

The +15-volt dc bus is provided by VR502. This three-terminal linear regulator receives its power from the 25-volt dc bus. This regulator has built-in current limiting as a function of internal temperature.

Power Supply for -15 Volt

The -15-volt chopper regulator consists of transistors Q104 and Q105; free-wheeling diode CR103; inductor L104; capacitors C136, C137, and C138; and the pulse-width modulated regulator U102 (LM1524). Resistor R129 provides the sensing for current limiting.

Power Supply For +5 Volts

This power supply is used only for the inverter drive logic module. This chopper regulator consists of transistors Q507 and Q508, free-wheeling diode CR508, inductor L506, capacitor C546, and integrated circuit U505. U505 is a µA723. The µA723 includes a temperature-compensated reference amplifier, error amplifier, power series pass transistor, and a current limiting circuit. The reference voltage is connected to pin 5 through a voltage divider. Capacitor C542 is used to compensate the circuit. Output current is sensed by R545. Zener diode VR506 is provided for overvoltage protection.

2.6 High Voltage Power Supply

The high voltage power supply (HVPS) is a conventional three-phase full wave bridge rectifier with a step-up transformer and LC filter. The schematic for the HVPS is shown in Figure 2.6-1. The fundamental theory of operation of three-phase rectifiers is not discussed, however the impact of the dc voltage, the dc current, and the source frequency on this transformer and rectifier is discussed. The means of selection of the values for the inductor and capacitor is also discussed. The final subparagraph discusses some particular examples of the high voltage design in this power supply.

2.6.1   Transformer

The transformer is typical of a three-phase step-up transformer with a delta primary and wye secondary. Because of the voltage and frequency, special attention was paid to the insulation of the windings, core loss, leakage inductance, and copper loss.

Four mil grain oriented silicon steel cores are normally used for larger transformers at 400 Hz. The cores are normally operated at a flux density of 16000 gauss. At this flux density, the core loss is 15 watts/lb. Twelve mil cores at 60 Hz have about one-half of the core loss of 4 mil cores at 400 Hz.

Grain oriented silicon steel is available down to 1 mil thick. The core loss curves show that there is no advantage in using a silicon steel core material less than 2 mils thick at 2 kHz.

Figure 2.6.1-1 is the core loss for 2 mil grain oriented silicon steel for various frequencies and flux densities. To limit the core loss to 15 watts/lb requires that the flux density be limited to 6500 gauss at 2 kHz. The core required for this flux density would have to have either a large cross section or the number of turns would be so large that the leakage inductance would be excessive. A value of core loss of 30 watts/lb was chosen. At 30 watts/lb., the core loss is much greater than the copper loss. By the use of conductive cooling, the core can be kept to safe operating temperatures. The final design is therefore a compromise among core loss, core area, and number of turns.

Leakage inductance causes a voltage drop in the dc output. The percentage of voltage drop in the output is approximately equal to the impedance of the leakage inductance at the power frequency, divided by the total impedance of the output circuit. The inductance used in this calculation is the leakage inductance in two legs of the transformer in series. For each transformer, the load impedance is 1320 ohms. For 5% reactance, the impedance per leg would be 33 ohms at 2500 Hz (highest frequency). A leakage inductance of 2.1
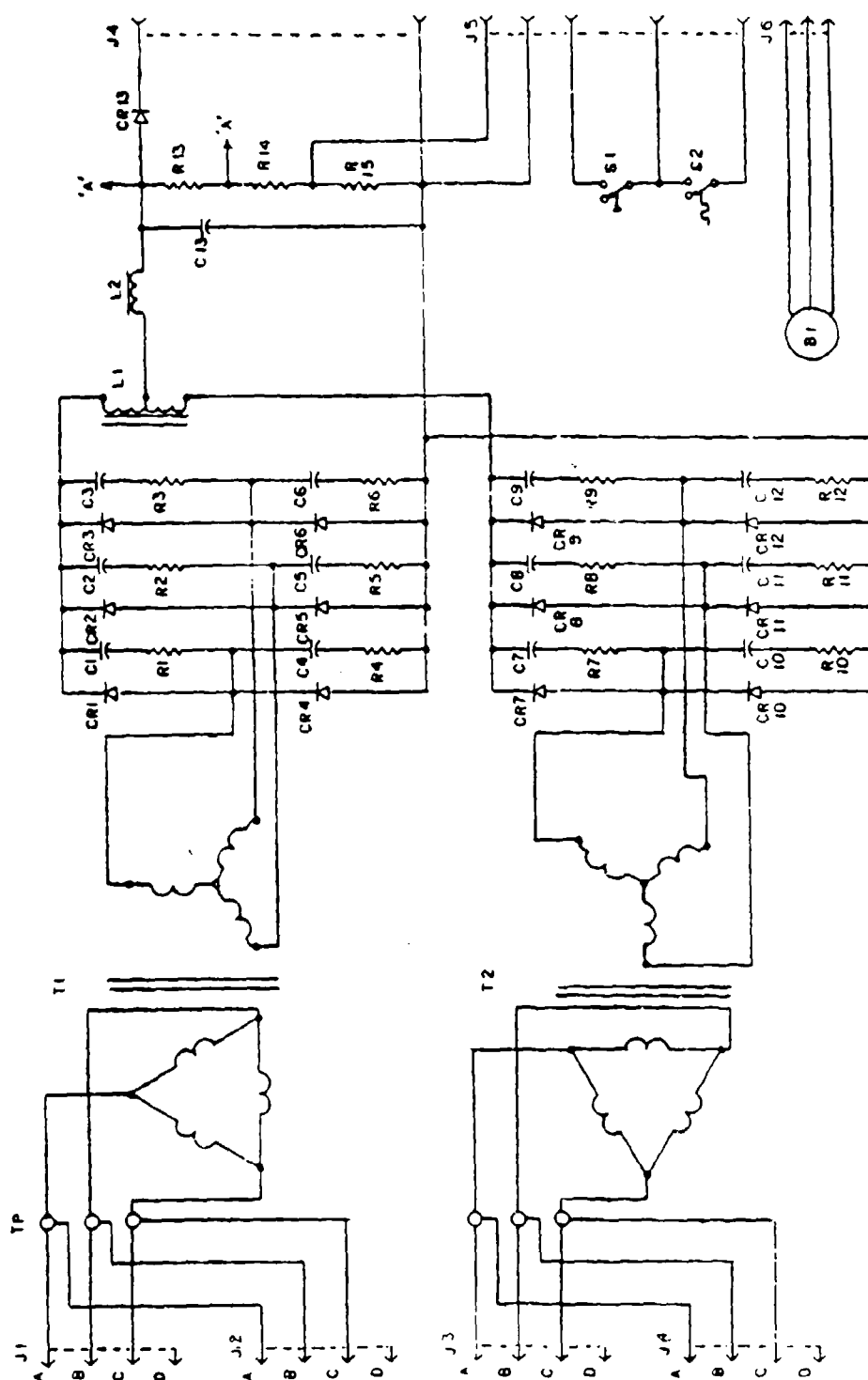
Figure 2.6-1

HVPS Schematic

2.6.1 Transformer (Continued)

mh/leg referred to the secondary would give 5% regulation. The voltage distortion caused by the phase back power supply, will increase the regulation. A smaller leakage than the value calculated above is desirable.

The number of turns, mean length of turn, length of the winding and the insulation space between windings all contribute to the leakage inductance.

It is also necessary to keep the primary to secondary capacitance to a minimum. AC can couple through this capacitance and through the load and cause ripple, which is difficult to filter. At 400 Hz, the effect of this capacitance can usually be ignored. The operating frequency of this power supply is 1886-Hz minimum. At this frequency, the current through the capacitance is 4.5 times as great as it is at 400 Hz. This could cause ripple problems.

The factors affecting capacitance are mean turn, length of winding, thickness of insulation, and dielectric constant of the insulation.

One of the factors controlling both the leakage inductance and capacitance of the transformer is the thickness of insulation between the windings. For low leakage inductance, the insulation space between the windings should be kept as small as possible commensurate with the voltages involved. This spacing can be kept small by using a high electric strength material such as Kapton between windings.

A small spacing between windings increases the capacitance. The relatively high dielectric constant of Kapton further increases capacitance. To keep capacitance low, the primary insulation between the primary and secondary is SF6.

To keep the leakage low, a core of relatively large cross section is used. This increases the mean turn but reduces the number of turns. Since leakage varies as the turns squared, the leakage is reduced. The core is heavier than would normally be used but the total transformer weight does not increase.
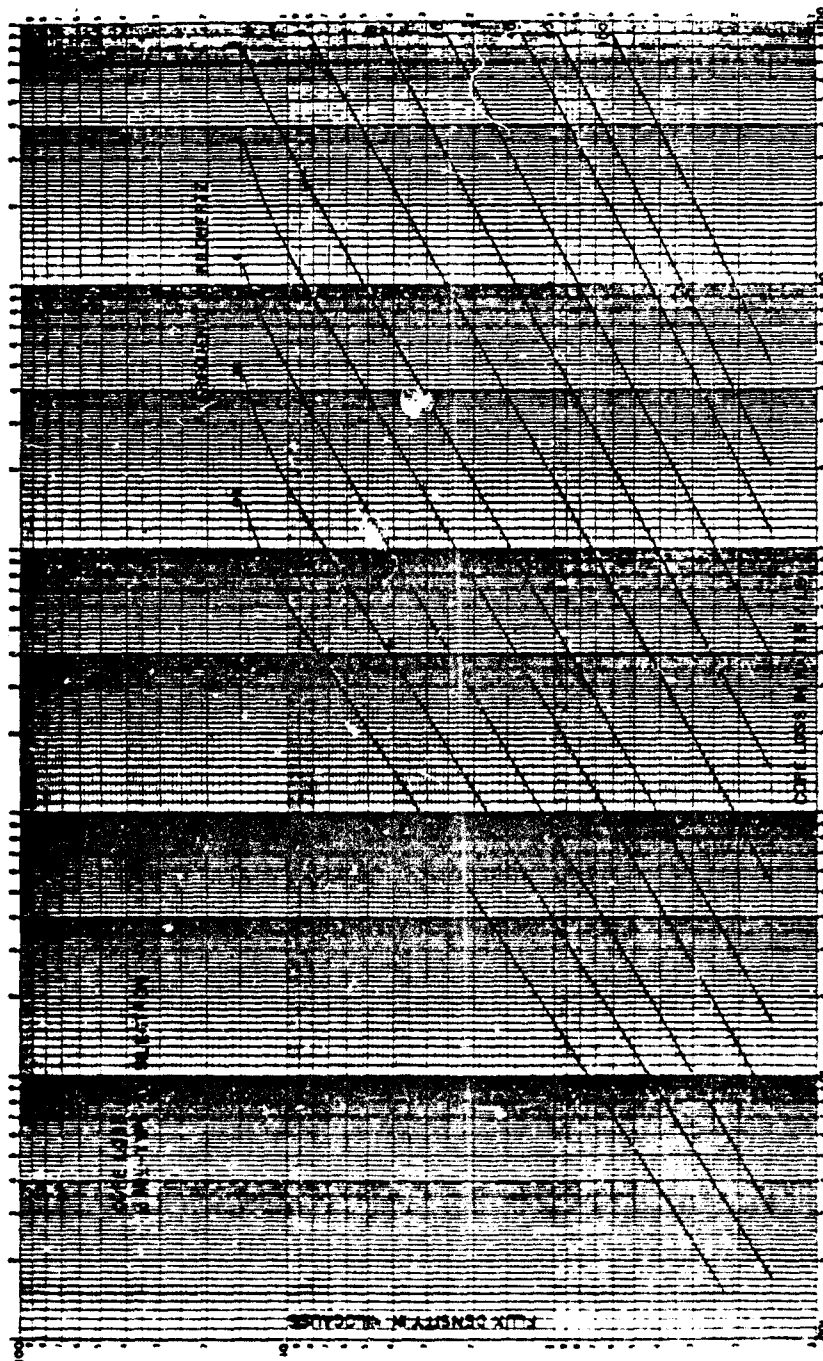
Figure 2.6.1-1

Core Loss, 2 mil Grain Oriented Silicon Steel

2.6.1   Transformer (Continued)

The core and coil assembly is shown in Figure 2.6.1-2. The arrangement is conventional for a three-phase transformer. The major insulation between primary and secondary is SF6. The coil form, wire enamel, and layer insulation are all capable of operating continuously at 200°C. The operating hot srot temperature of the transformer is 150°C.

Cooling of the transformer is both by conduction and forced convection. SF6 is forced through the space between coils and between the core and coils. The core is mounted to a structure that is in thermal contact with the tank wall in the area of the liquid cooling pipes.

2.6.2   Diodes

In a perfect three-phase rectifier, when the applied voltage has the polarity to transfer conduction from one diode to another, the transfer takes place in zero time. Solid state diodes do not recover from the conducting to the blocking state in zero time. When one diode in a rectifier starts conducting, the diode that was conducting continues to conduct for a finite time. During this time, two phases of the transformer are working into a short circuit. The current is limited only by the leakage inductance of the transformer. When the one diode does recover its reverse blocking capability, the current through the inductor is suddenly interrupted. This can cause a very high voltage transient, along with a loss of energy and increased dissipation in the diode.

The magnitude of this transient can be reduced by reducing the value of leakage inductance and/or using fast recovery diodes. It is good practice to select diodes with peak inverse voltage (PIV) ratings of several times the expected peak inverse voltage of the power supply.

The diodes selected have a PIV rating of twice the expected voltage. The reverse recovery time of the diodes is 500 nsec. Additional protection for the diodes and EMI reduction is accomplished by adding an RC network around each diode. The value of the resistor is chosen to critically damp the transients generated. The capacitor is chosen to limit the power in the resistor.
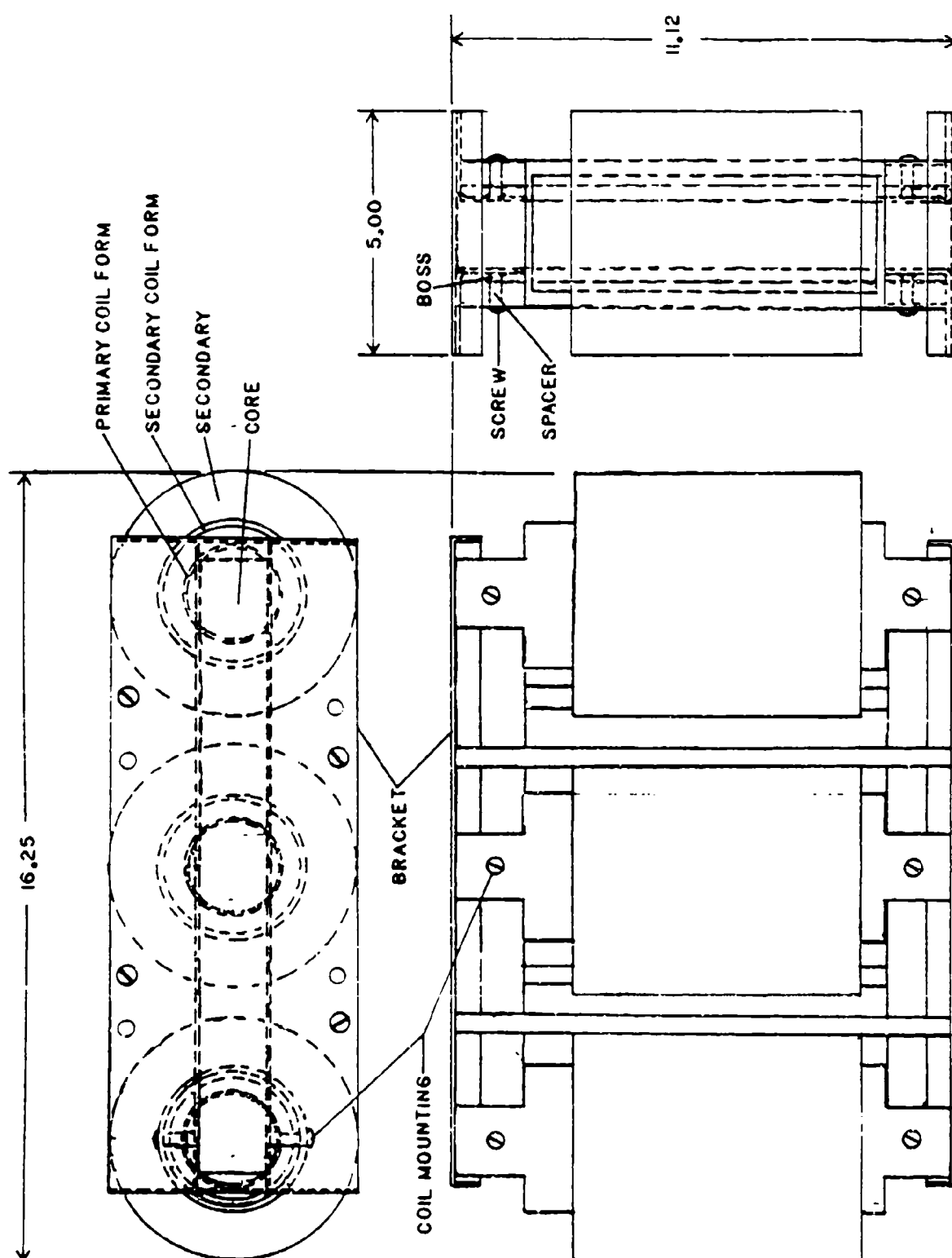
Figure 2.6.1-2
High Voltage Transformer

2.6.3   DC Filter

The unfiltered ripple from a power supply with a sine wave input is easy to calculate. If the input ripple and the desired ripple is known it is a simple matter to select an LC filter to provide the required attenuation.

The unfiltered ripple for this system is not so easy to calculate. The distorted input waveform and the interaction between the two power supplies makes direct ripple calculation difficult. The unfiltered ripple for a single three-phase full wave power supply operating in the system was calculated using a computer program. The ripple under this condition is shown in Figure 2.6.3-1 The output ripple is the vectorial sum of the ripple of two identical power supplies, phase shifted by 30°. This ripple was not computed but was estimated by overlaying the ripple from the two power supplies. The combined ripple is shown in Figure 2.6.3-2

With the unfiltered ripple and the desired output ripple known the required attenuation of the filter can be calculated. The attenuation of an LC filter is the reciprocal of the capacitive reactance at the ripple frequency divided by the total circuit reactance. It is desirable in an LC filter to have the inductance large enough to maintain continuous current conduction. This minimum value is called the critical inductance. Usually a value of several times the critical inductance is chosen for a practical filter.

Once a value of inductance is chosen, the value of capacitance for the required attenuation can be calculated. This filter may not be optimum from the standpoint of size, weight, or voltage transients. There are two possible times when voltage transients can occur. First is during turn on. Depending on the ratio of L,C, and load the dc voltage can rise to twice normal. This is not a problem in this power supply since the turn-on will be a slow ramp from one-half to full voltage. A transient can also occur when a load is removed. Then the energy stored in the inductor is transferred to the capacitor. This raises the voltage on the capacitor. The ratio of stored energy between the inductor and capacitor determines how much the voltage on the capacitor is raised.
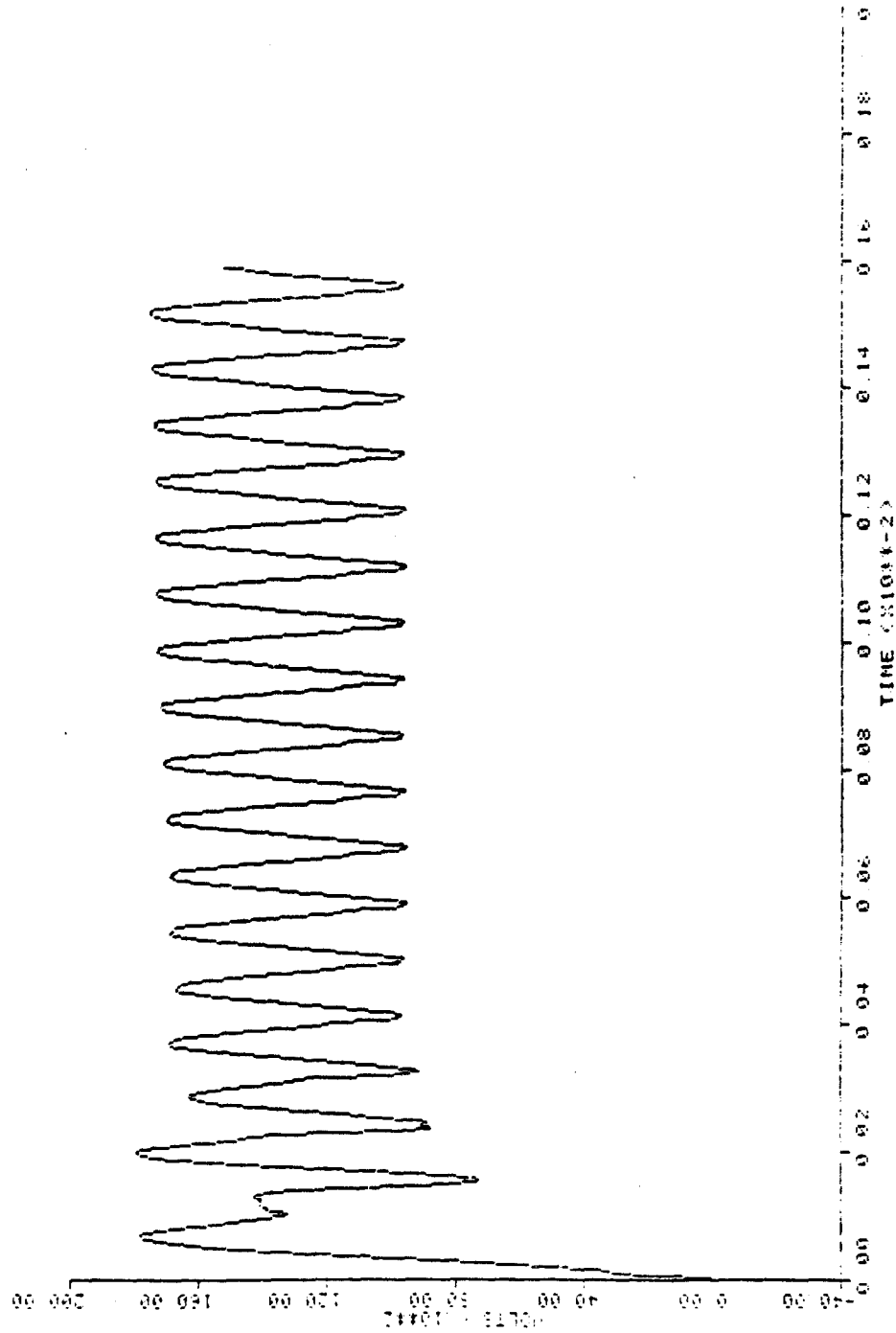
Figure 2.6.3-1

Computer Calculated Ripple, 6-Pulse Power Supply, Combined System
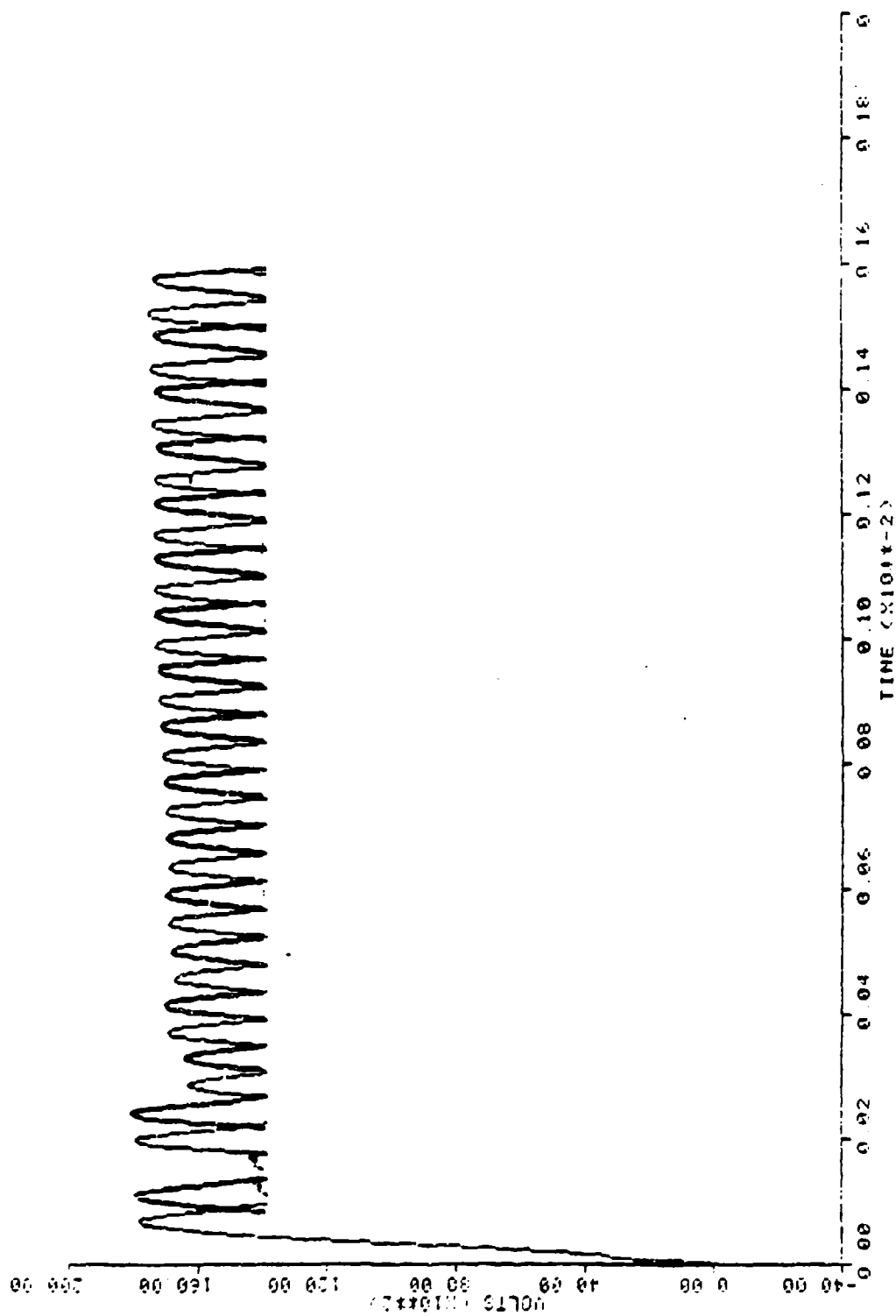
Figure 2.6.3-2

Ripple for Two 6-Pulse Power Supplies, 30 Degrees Phase Shifted

2.6.3   DC Filter   (Continued)

The original values calculated for a filter were 1 millihenry and 1
microfarad. The weight of this filter was about 3 pounds for the inductor and
10 pounds for the capacitor. The density of a capacitor is much less than the
density of the inductor, so that this filter has a capacitor that occupies
many times the volume of the inductor. The transient rise on the capacitor at
turn-off is less than 100 v.

Since the capacitor occupied so much more volume than the inductor, the values
were adjusted to equalize the volumes. This equalization did not result in a
minimum weight filter but did keep the total weight of the system to a
minimum. The inductor chosen is 10 microhenries. The capacitor is 0.1 µf.
The transient overshoot is 1300 v. The volumes of the inductor and capacitor
are approximately equal.

2.6.4   Balancing Inductor

If two power supplies are connected in parallel, the outputs may not share the
load equally. An inductor in the dc output before the filter helps to balance
the output by balancing the ripple in the two power supplies. The balancing
reactor keeps the volt seconds in each half balanced. Since the average
voltage is the dc level plus the average of the ripple, the inductor helps
balance the dc voltage.

2.6.5   Monitoring

The only monitoring function in the high voltage section is the dc voltage
monitor. This is provided by a 1320:1 resistive voltage divider. For a 13.2
kv dc level a 10.0 V monitor voltage is developed. The divider is shown with
a tap at each end (see Figure 2.6-1). The taps at the negative end are
connected to the pins of a connector. Negative ground is assumed. If the
positive end of the power supply is grounded, the monitor points at the
positive end of the voltage divider will be used.

2-117

2.6.6   Parallel System Isolation

A diode is connected in series with the output. If any one of the four power
supplies fails, this diode provides isolation of that power supply from the
others. This diode is chosen to handle the full current and voltage with
adequate deratings.

2.7   28 Volt Power Conditioner

2.7.1   Objective for 28 Volt Supply

Each 28-volt-dc supply is to provide 17-kw pulses for 1 millisecond, with a 30
millisecond off time. The objective was to design a 28-vdc switching power
supply to charge a bank of capacitors. The nominal output voltage is 28
volts; the total capacitance is equal to .3 farad; all capacitors are
paralleled. Figure 2.7.1-1 shows a simplified diagram of the circuit.
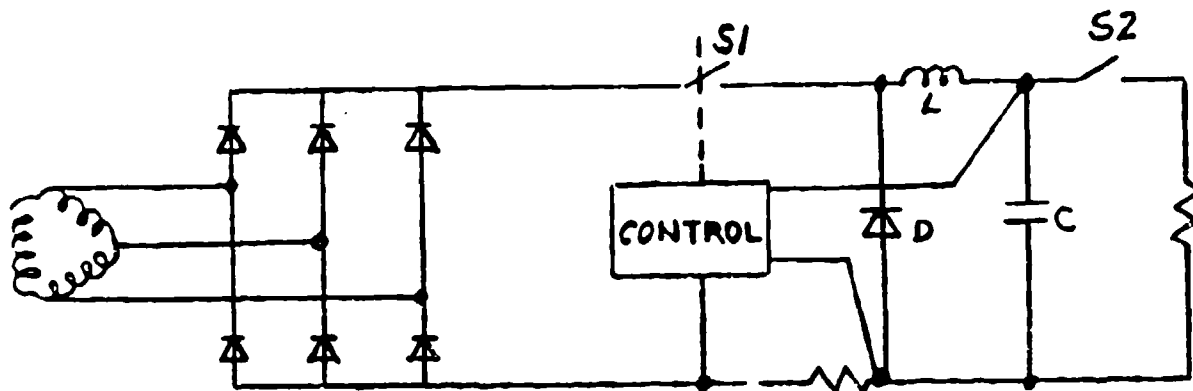
Figure 2.7.1-1
Simplified Diagram of the 28-Volt DC Power Supply

2-118

2.7.2   Operation

A brief description of unit operation follows (refer to Figure 2.7.1-1).

Starting with "C" fully charged (29 volts), S2 is closed for one millisecond and the capacitor voltage drops from 29 to 27 volts as the load draws 17 KW for the one millisecond. This drop of voltage activates the control circuitry. The controls causes switch S1 to close and open at a 20 KHz rate.

On closure of S1, current builds up in the inductance "L" and energy is supplied to "C." On opening, "L" continues to supply energy. The diode "D" completes the circuit.

On successive closures of S1, the current will climb until it reaches 24 amperes. The voltage developed across "R" then causes S1 to open and from this time on, S1 closes and opens so that current cycles from approximately 20 to 24 amperes. Within 30 milliseconds, the voltage across "C" will reach 29 volts and S1 will then stay open.

2.7.3   Detailed Circuit Description

The heart of the control system is the Integrated Circuit (IC) SG1524 (Silicon General). This IC is a pulse width modulator. When more current is required, this chip affects a closure of the series switching transistor for a longer time (see S1 of Figure 2.7.1-1 and Q1 of the schematic, Figure 2.7.3-1).

In the description that follows refer to the SG1524 circuit, Figure 2.7.3-2 and to the schematic, Figure 2.7.3-1. The selected operating frequency is 20 KHz and is established by R10 and C4 connected to pins 6 and 7 of the SG1524. T1 is the charge time during which Q1 is closed. During T2, Q1 is open. T1 + T2 is 50 microseconds as required for 20 KHz.

In Figure 2.7.3-2 the pulses at "A" from the oscillator trigger the flip-flop (F/F). On alternate half cycles NA and NB (NOR gates) outputs are high when the appropriate F/F output is low (see Figure 2.7.3-3). On alternate half cycles, therefore, QA and QB are on. If these transistor outputs are paralleled then on-time can be nearly 100%. This on-time is the time (T1)
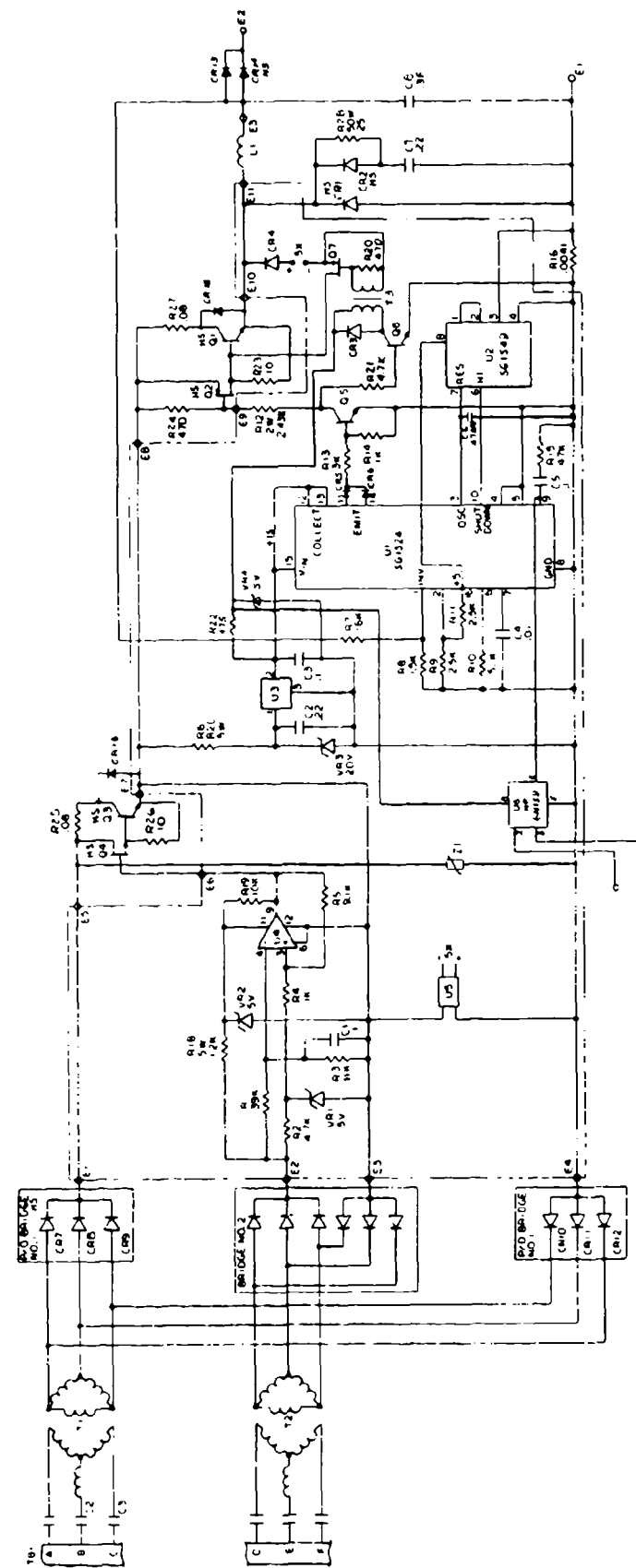
Figure 2.7.3-1

Schematic Diagram, 28 VDC Supply

Figure 2.7.3-2

SG 1524 Pulse Width Modulator

2.7.3 Detailed Circuit Description (Continued)

that the transistor Q1 is closed, and charging takes place. The short pulses at "A" (Figure 2.7.3-2) also feed directly to NA and NB. For these short intervals NA and NB will be off (low), regardless of other circuit action. This time will be referred to as dead time.

A voltage proportional to the controlled output voltage across the load capacitor is connected to the inverting input of the error differential amplifier (pin 1 of Figure 2.7.3-2). The other differential input (pin 2) is connected to 2.5 VDC derived from the internal reference voltage. The output of the error amplifier is compared with the sawtooth signal "B" from the oscillator (see Figure 2.7.3-3). When the sawtooth voltage exceeds the error amplifier's output, the comparator output goes high (Figure 2.7.3-3b). For any input high on the NOR gate, the output goes low, turning off QA and QB. This turns the switching transistor off. As the voltage of the load increases the error amplifier output decreases so that the sawtooth will reach the same voltage earlier in the cycle. Comparator output remains high longer (Figure 2.7.3-3b, dashed lines). Thus, the switching on-time is reduced. This action takes place at an output voltage very close to 29 volts.

Although this design does not use pins 4 and 5 of the SG 1524 it will be helpful to complete the description. If pins 4 and 5 are connected to a load current sense resistor, an increased current will increase the voltage with pin 4 high relative to 5. This pulls the comparator (pin 9, Figure 2.7.3-2) input down and action is similar to that described for an increase of output voltage. Thus, the output voltage controls the on-time of the series switch Q1 and thus, the energy delivered. Immediately after the load capacitor C8 is discharged, the voltage at E2 is down two volts (about 27 volts) providing approximately 100% on-time. Long on-time occurs during initial charging of C8. This design uses a SG 1549 current sense latch which provides increased sensitivity and current limit on a "per cycle" basis. The block diagram is shown in Figure 2.7.3-4.

a. System Output Volts / Increased System Volts / Oscillator

b. Comparator Output

c. F/F A / F/F B

d. NOR A

e. NOR B
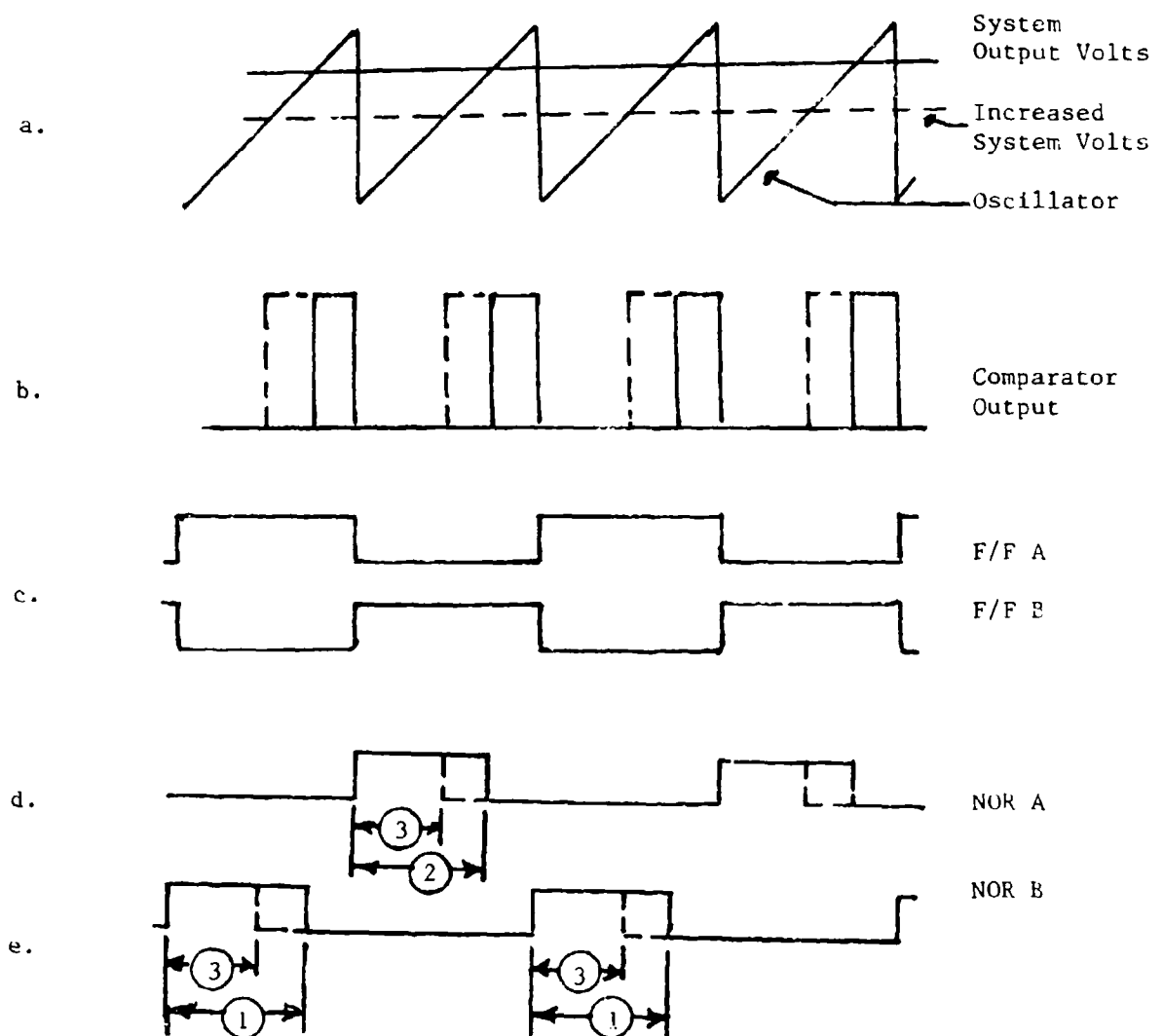
1　Time on for AQ

2　Time on for QB

3　Time on for QA and QB, increased Load Voltage

Figure 2.7.3-3

SG 1524 Action for Increasing Load Voltage

2.7.3 Detailed Circuit Description (Continued)

The current sensing resistor R16, Figure 2.7.3-1 is connected between pins 3 and 4. When this voltage reaches 100 millivolts the output (pin 6) switches to "high." This high is connected to pin 10 of the modulator (Figure 2.7.3-1). Through transistor action the comparator output is pulled down turning QA and QB off (Figure 2.7.3-2) thus turning Q1 off (Figure 2.7.3-1). A small amount of hysteresis is provided in Figure 2.7.3-4 to latch the output. Reset is provided by connecting pin 3 of the modulator to pin 7 of the latch. Via this path, oscillator pulses trip the latch comparator to output "low." In this manner each current pulse, if high enough, is capable of stopping the charge cycle.

Additional components are needed to raise the power level to that necessary to turn Q1 on and off. Assuming charging is in progress, QA and QB alternately furnish current to the base of Q5 with on-time T1 and off-time T2, where T1 + T2 = 50 microseconds. The net result is a pulsed voltage to the charging network that appears as shown in Figure 2.7.3-5.

When Q5 is conducting (T1), current through R24 (Figure 2.7.3-1) provides a voltage at the gate of Q2 turning this P-FET on. This provides base current to Q1, the switching transistor. L1 will now be charged by a current ramp. T2 starts when QA and QB turn off, turning off Q5, Q2, and Q1. CR1 completes the circuit as L1 current ramps down continuing the capacitor charge.

2.7.4 Circuit Details (Refer to Figure 2.7.3-1)

In order to reduce Q1 storage time, a charge must be pulled out of the base when turn-off starts. This begins at the start of T2 when the collector of Q5 goes high. Current now flows into the base of Q6, turning Q7 on through transformer T3. Current now flows through Q7 and CR4, into the emitter of Q1 and out of the base (reverse current). The time necessary to reduce the charge in Q1 base is of the order of one microsecond. The reduced storage time that results greatly reduces the dissipation in Q1.
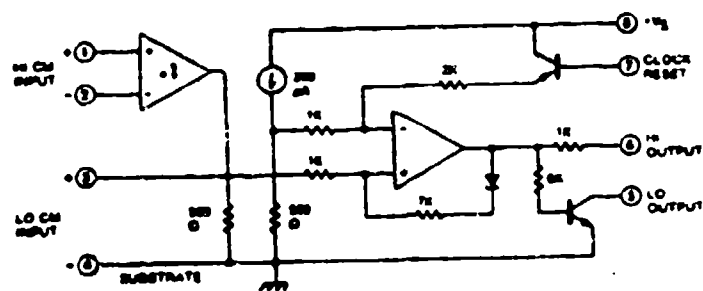
Figure 2.7.3-4

Block Diagram, SG 1549 Latch

QI-CURRENT

LI CURRENT
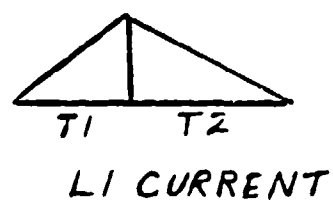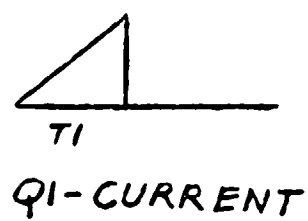
Figure 2.7.3-5

Waveform of Output and Charging Network

2.7.4   Circuit Details   (Continued)

C6 is connected to the oscillator output (pin 3). This extends the dead time. Normally, there is plenty of time to turn Q1 off. During initial charging when L1 current is far below 24 amperes, on-time is nearly 50 microseconds. Off-time will be dead time and it is during this time that Q1 charge is removed. C6 provides the necessary time. In order not to load Q1 when it is on, the circuitry of Q7 is isolated by the transformer T3 and the diode CR4. Power for this circuit is provided by U5, a DC/DC power supply. This supply has excellent input-to-output isolation. Again, CR4 will prevent capacitive current through these windings. (See the discussion at the end of this report for an alternative to U5.)

Because there will be some exciting current buildup in transformer T3, a separate supply is provided, regulated by VR4.

R10 and C4 determine the frequency of 20 KHz.

R15 and C5 are compensation for loop stability. This includes C8 and L1.

C7, CR2, and R28 constitute a turn-off snubber providing a current path such that transistor current may cease before full voltage appears across the collector-emitter. During on-time C7 is charged through R28. At turn-off C7 supplies current through CR2.

The .08 ohm in the collectors of Q1 and Q3 provide drain-to-source voltage for the FETs Q2 and Q4. This permits hard turn-on of the power transistors and reduces their dissipation.

The input ac power comes via transformers T1 and T2. These transformers are constructed so that the capacitance between primary and secondary is less than 100×10^{-12} farads. The T2 secondary windings could be included on T1. However, a fault such as a short on the secondary of T2 would not open the circuit breakers.

2.7.4   Circuit Details   (Continued)

Bridge #1 provides main power, which is approximately 600 watts with a range
of voltages of 38 to 65 vdc on the load side.

A TTL input of 4 mA into pin 2 of U6 will shut down the system.

2.7.5   Overvoltage

During a fault when the primary side voltage may go up to 360 volts, the
circuitry is designed to turn off. Normally, Q3 is closed. (The output of U4
is high.) At 260 volts there will be 65 VDC at E1 and 18.6 volts at E2. If
the line voltage rises the output of Bridge #2 rises in proportion. Before E1
gets to 100 volts, the comparator U4 is tripped by the rising voltage at E2.
This turns Q3 off. Since there will be some energy in the leakage inductance
of T1 a surge suppressor (Z1) is connected across the line. Some hysteresis
is provided for U4. All components on the load side of Q3 can withstand 100
volts.

The reliability of the load capacitors is largely dependent on the capacitor
internal temperature. The calculation of this temperature rise is not precise
since some of the variables are not well defined. The power generated in a
capacitor is I^2R where "R" is the equivalent series resistance. This
parameter is quite variable with temperature. The vendor has suggested that a
capacitor be supplied with an embedded thermocouple to check the temperature
rise in a test circuit.

2.7.6   Switching Theory

The switching power supply is a very efficient device to convert from one dc
voltage to a lower DC voltage. Referring to Figure 2.7.6-1, the efficiency is
equal to $E_{in}/(E_{in} + V_s)$.
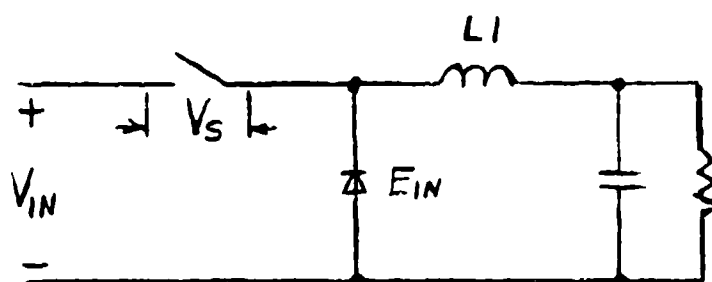
Figure 2.7.6-1

Simplified Power Switch, Charging Circuit

2.7.6   Switching Theory   (Continued)

This assumes no losses in the components including no switching losses in "S".   The switch saturation voltage V_s can be of the order of one volt. This high efficiency is sustained even though V_{in} may be highly variable. This is in contrast to the reduced efficiency for the analog series pass regulator when V_{in} varies either due to line regulation or ripple from the filter.   See Figure 2.7.6-2.
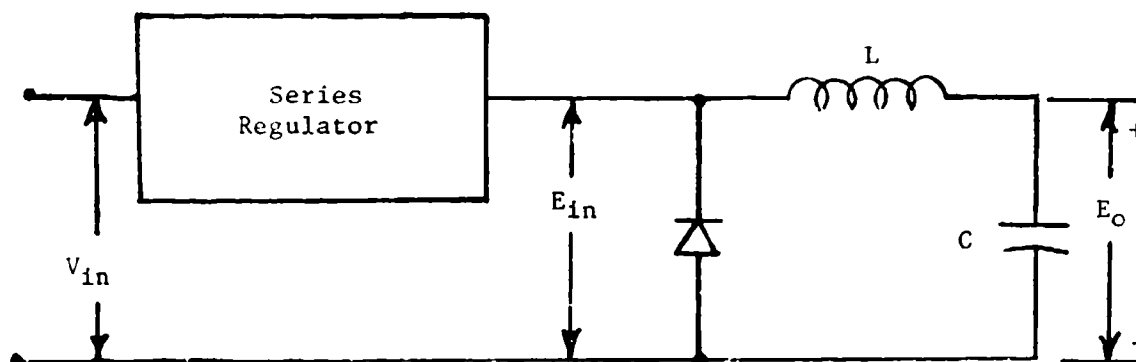
Figure 2.7.6-2

Configuration for a Series Pass Regulator

2.7.6   Switching Theory (Continued)

From the relation $E = L \, di/dt$ we get the design equations and the value of "L." The basic equation is: $ET1 = L \, \Delta \, I$.

When charging "S" is closed the voltage across "L" is $E_{in} - E_o$ (refer to Figure 2.7.6-1).

   Charge: $(E_{in} - E_o) \, T1 = L \, \Delta \, I$

   T1 - Charge Time

   ΔI - Current Increment = 4 Amperes

On discharge, "S" is open and the voltage across "L" is E_o.

   Discharge: $E_o \, T2 = L \, \Delta \, I$

   $T1 + T2 = 50 \times 10^{-6}$ Second (Period of 20 KHz)

These equations hold if the time increment is short compared to $2\pi \, \sqrt{LC}$ so that the voltage E_o is essentially constant during one charge cycle. These relations give the following results for an input of 65 volts and an output of 28 volts:

   $T1 = 50 \, E_o/E_{in} = (50 \times 28)/65 = 21.54$ Microseconds

   $T2 = 50 - 21.54 = 28.46$ Microseconds

   $L = E_o \, T2/4 = (28 \times 28.46)/4 = 199$ Microhenries

In this design a frequency of 20 KHz was chosen. This represents a reasonable compromise between efficiency and component size. Assuming the energy loss per cycle in the switch is constant, the power consumed will be $E \times F$ where "E" is the energy and "F" is the frequency. This refers to switching losses during turn-on and turn-off but not to saturation losses.

2-131

2.7.6   Switching Theory (Continued)

There is also an advantage to maintaining constant frequency and permitting T1 and T2 to vary. A Fourier analysis will show a constant set of harmonic frequencies but of varying amplitude. Allowing the frequency to vary will produce a variable set of harmonics, making filtering more difficult. With an average current of 22 amps, the charge supplied to C will be:

$$Q1 = \int \lambda dt = IT$$

The charge lost on discharge from 29 to 27 volts is:

$$Q_2 = C \Delta E = .3 (29-27) = .6 \text{ Coulomb}$$

For $Q_1 = Q_2$:

$$IT = .6$$

$$T = .6/22 = .027 \text{ Second (To Recharge)}$$

Recharge will take place in about 27 milliseconds.

If the input dc voltage is less than 65 volts then the on-time will be longer. The average current will be slightly higher than 22 amps. This may be shown by again solving the equations above for T1, T2, and "I" using the same value of "L."

2.7.7   Heat Sinking

A number of components dissipate enough power to require heat sinking. Some calculations are shown below:

1. For Q1, the power dissipation will be 62 watts. From this, knowing the device capabilities, the heat sink requirements can be calculated.
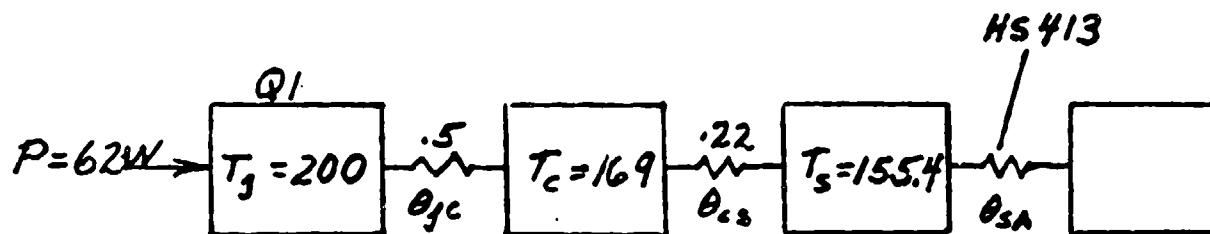
Figure 2.7.7-1

Thermal Resistance Network for Q1 Transistor

θ_{jc} = Junction to Case

θ_{cs} = Case to Sink

θ_{sa} = Sink to Ambient

T_c = T_j - θ_{jc} × 62 = 200 - .5 × 62 = 169°

T_s = T_c - θ_{cs} × 62 = 169 - .22 × 62 = 155.4°

Wakefield heat sink 413 has a rise of 84° for 62 watts.

155° - 84° = 71°

Equivalent θ_{sa} = 84/62 = 1.35

2-133

2.7.7   Heat Sinking (Continued)

2. For Q2, the power dissipation will be six watts. From this, knowing the
    device capabilities, the heat sink requirement can be determined.
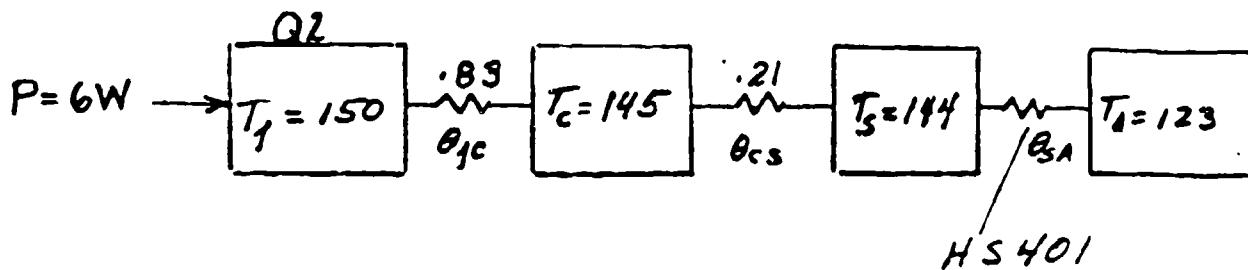
Figure 2.7.7-2

Thermal Resistance Network for Q2 Transistor

$$T_c = T_j - \theta_{jc} P = 150 - .83 \times 6 = 145$$
$$T_s = T_c - \theta_{cs} P = 145 - .21 \times 6 = 144$$

Wakefield 401 heat sink rises 21° for six watts.

$$T_A = T_S - 21 = 123°$$

This unit will operate safely up to 123° ambient.

2.7.8   The Series Switch

The following discussion about this design will point out the trade-offs in the configuration and the reason for the selection of certain components.

The series pass transistor switch Q1 and driver Q2 are shown below.
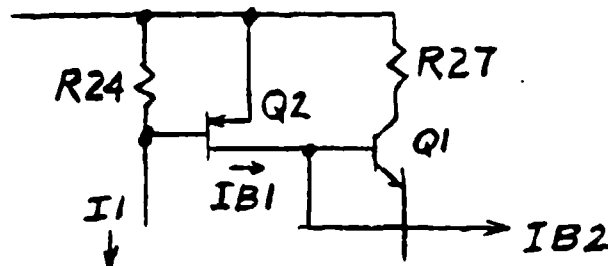
Figure 2.7.8-1

Series Pass Switch

Current "I" through R24 drops the gate voltage of Q2. Q2 conducts current to the base of Q1 turning this transistor on. For low loss, it is desirable to provide enough base current to saturate Q1. Q1 will then have less than 1.0 volt across collector to base. Since one volt is not sufficient for satisfactory operation of Q2, R27 is added. Omitting R27 would not permit Q1 to saturate resulting in more loss in the collector. Thus, R27 provides a sink for losses which would otherwise occur in Q1. This will increase the reliability of Q1.

Switching losses in Q1 will be minimized if turn-on, turn-off, and delay time are kept to a minimum. Ib1 and Ib2 should have steep wave fronts - much less than one microsecond. Ib1 is supplied by Q2, a high-speed FET. Although Q2 requires essentially no drive power it does have input capacitance. To get a fast rise of voltage at the gate of Q2, R24 must be small. The necessity for Ib2 has previously been explained.

A Darlington could have been used in the above circuit. The losses would have been comparable. However, considerable drive power would have been required had Q2 been chosen bilateral.

The specifications available on the high current, high voltage device Q1 are not as complete as the circuit designer requires for a complete determination of all the pertinent components. It is expected that testing will show that some circuit modifications will be necessary to arrive at the optimum trade-off.

2.7.9 A Circuit Variation

A possible variation on the existing series pass arrangement is shown in Figure 2.7.9-1 below.
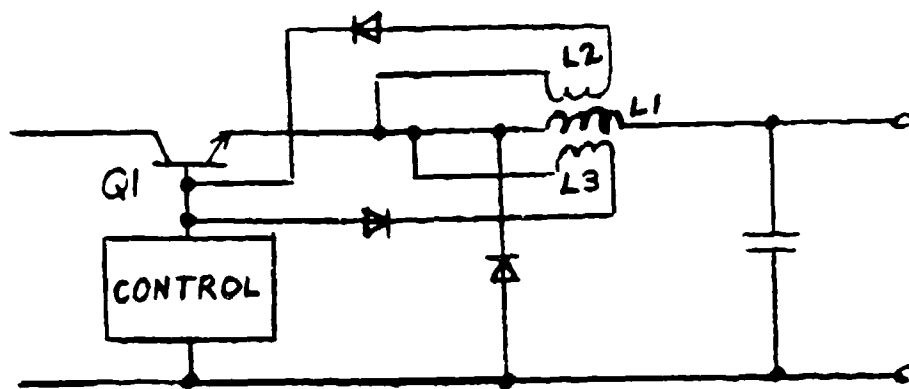
Figure 2.7.9-1

Alternate for the Power Switch

This circuit uses positive feedback. At turn-on current is supplied to the base of Q1 by the control circuit. The resulting current in L1 induces a voltage in L2 and L3. L2 provides additional drive to Q1, quickly driving it to saturation. At turn-off L3 supplies voltage to pull current out of the base. L3 could be used to provide low voltage DC to the Ib2 circuit such as used in the present design. A successful design of this alternative would eliminate the need for U5 and possibly Q7 and associated components. This simplification would result in greater reliability.

2.8   Paralleling

The theory of operation for the parallel system was verified with a computer simulation. The simulation included only the controls required for parallel operation including voltage regulation, current limiting, etc. but did not include protection circuits. The simulation did not include the 28-v-dc system because it is such a low fraction of the system rating that it was assumed that it could be safely ignored. The average total power for the 28-v-dc system is only 1630 watts as compared to 270,000 watts for the HVDC system and 120,000 watts for the 400-Hz ac system.

A two-channel simulation was used rather than a three- or four-channel simulation to save computer time and program development time. If necessary, the simulation could be modified to include more channels. The more channels that are paralleled, the easier the system is to stabilize; i.e. for a system with a very large number of participating channels, any one channel would behave as if paralleling with a much larger source. An erring channel will have the full error to correct its load sharing error, whereas the other channels will have $1/(n-1)$ of the error. In a two-channel system, each channel will have the same error, just opposite in sign. If a two-channel system is stable, then a three- or more -channel system will be more stable.

Schematic Diagram ED 395741 in Appendix A depicts the simulated system. The diagram mixes circuit connections and certain computer functions into one reference document. It contains all the variable names that are used in the simulation as they appear in the program listing. The program listing is included in Appendix B. Typical outputs from the computer simulation are included in Appendix C. The outputs consist of waveform plots and a parameter listing that records all the parameters for that particular run.

2.8 Paralleling (Continued)

The simulation is an extension of a similar one developed by Westinghouse Lima for the analysis of parallel VSCF ac systems. The simulation uses the Forward Euler Integration method. The time step is selected small enough to give visi- bility to the pertinent time constants and system responses, but long enough to keep the run time economical. The time step is named "Dt" meaning "Delta time" and is 62.5 microseconds. Many numerical analysis textbooks cover the Forward Euler method in detail and it is not repeated in this report. Westinghouse has, however, developed a technique that is an improvement over one shortcoming of the Euler method. Using the Euler method, the Dt cannot be selected shorter than half the shortest time constant in the circuit being simulated. With the Westinghouse version, if such a situation exists, the simulation will still give good accuracy and the program will not "blow up" and give totally meaningless results. In fact, this Westinghouse technique has been used in several simul ions, all of a different nature, and the results have been shown to give very good correlation with actual circuit performance.

2.8.1 Paralleling, Generator Controls

The generator terminal voltage on the simulation is located at the voltage nodes named Vhu (1,1) and Vhu (2,1) for channel one and two, respectively. The internal characteristics of the generators are simulated with the items named Vstator1, Vrotor1, and Vpmg1 for channel one and similarily for channel two. A single line simulation is done for the generator. This means that all six phases of the generator are lumped into one conductor. If the average current for one phase is desired, then the generator current in the simulation must be divided by six.

2.8.1   Paralleling, Generator Controls   (Continued)

The equations for the stator, rotor, and PMG voltages were derived from the
performance characteristics provided by the design engineer. Figure 2.8.1-1
shows the generator performance as defined by the generator designer (solid
lines) and the approximate performance (dotted lines) used in the simulation.
This figure represents the generator's main rotating field and the main
stator. The vertical axis is the terminal voltage, line-to-neutral, and the
horizontal axis is the main rotating field amperes. This curve defines K51,
SAT LIMIT, Karm1 (armature reaction factor) and Zstator1 for the generators
being simulated. These factors represent the "transient" and "sub-transient"
reactance of the generator as well as its saturation characteristics, all of
which are a function of generator speed.

Figure 2.8.1-2 is the exciter characteristics as designed (solid lines) and
the corresponding simulated performance (dotted line). Here the
characteristics are relatively independent of generator speed, so a single
linear approximation was used. This information is used to define K41 in the
exciter simulation.

The exciter stator current in the simulation is named Ifld and it is
determined by the PMG voltage, the modulation factor (Duty1gen) controlled by
the voltage regulator, and the impedance (Rfld1 and Lfld1) of the exciter
winding. Duty1gen is a number between 0 and 1 that gives 0 to 100 percent of
available PMG voltage to the exciter circuit. The PMG voltage is shown as a
Thevenin equivalent voltage, but its resistance is accounted for because Rfld1
includes both the PMG resistance and the exciter resistance.
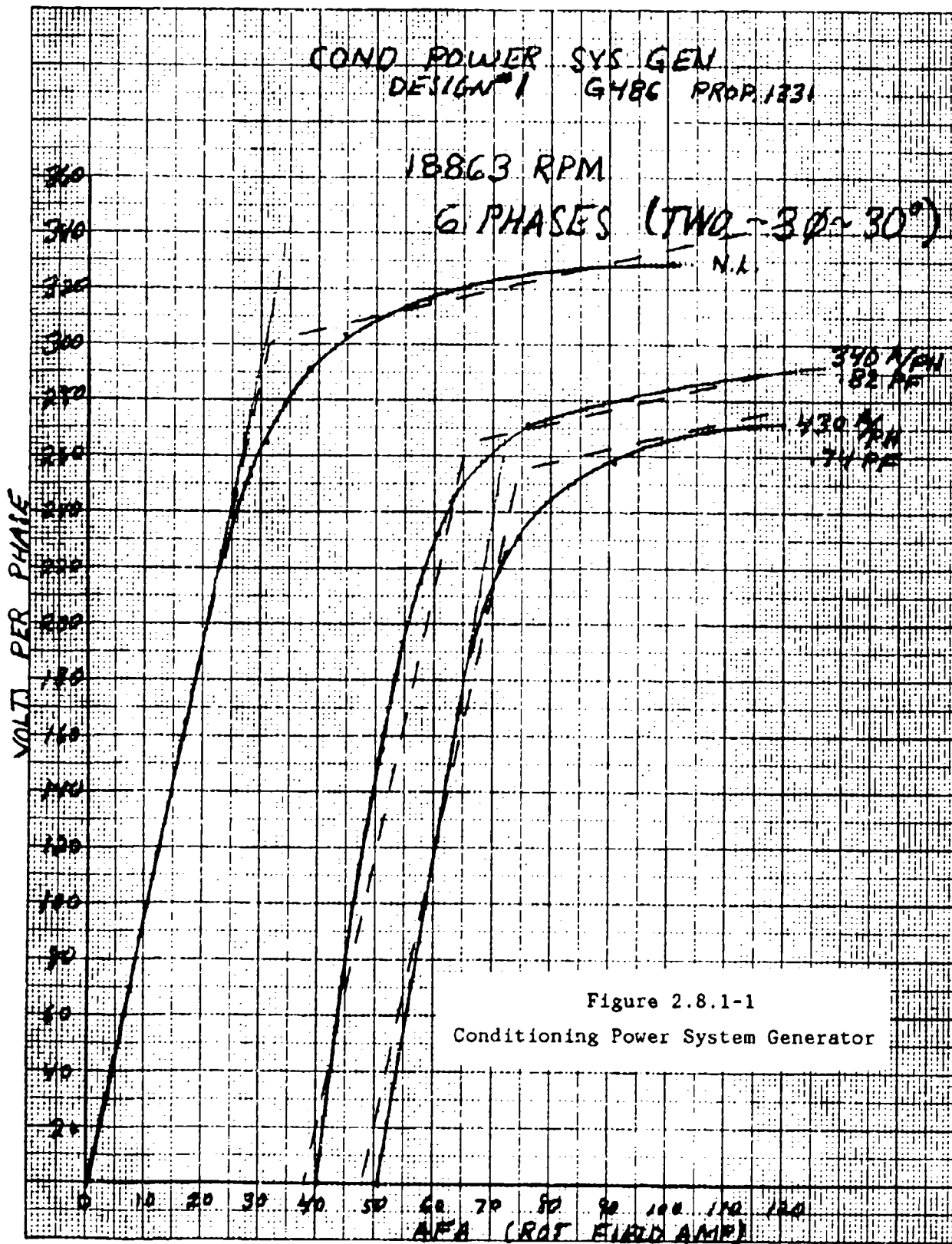
Figure 2.8.1-1
Conditioning Power System Generator
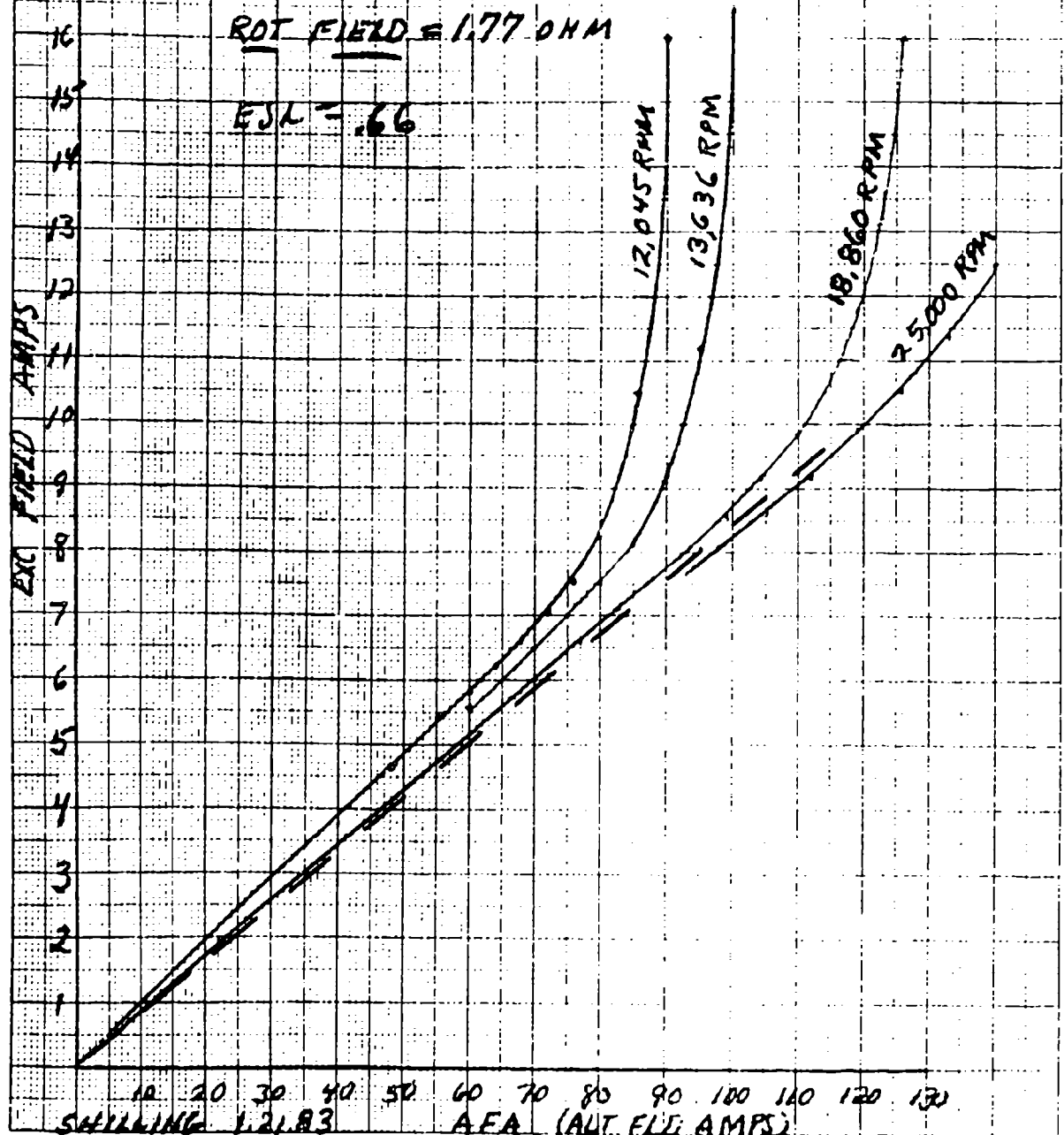
Figure 2.8.1-2

Exciter Characteristics Conditioning Power System Generator

2.8.1   Paralleling, Generator Controls (Continued)

The main part of the voltage regulator consists of the summing node with
Vreflhv as the reference input. The difference between this voltage and the
output of the HVDC system is the error (Vhvlerr) that drives the generator
regulator. The regulated voltage is scaled down to the effective line-to-
neutral voltage of the generator so that other functions can be easily added
to the loop. The gain of the voltage regulator loop is defined by K61. That
is, the reciprocal of K61 is the delta voltage required to turn the voltage
regulator from full off to full on e.g. a K61 of 0.1 would give a gain that
would force the point of regulation to be within ± 5 volts of the reference.

Additional regulator functions include the paralleling control (Vhvlub) and
the minimum generator voltage control (Vsetlgen). The minimum generator
voltage control loop is used to keep the generator "awake" during no load or
nearly no load conditions. The paralleling control loop uses the "difference
from average" load current to adjust the voltage regulator to make the channel
share load equally with other channels. Primary or ac side current sensing is
used to keep the sensing circuit low cost and reliable. Sensing current at
the 13,200 volt level has inherently costly dielectric problems associated
with it. The average current of the participating channels is on the common
conductor between units and feeding the summing node which also connects to
the Rburdl resistor. This is referred to as the average power signal bus. If
a channel is to run in the non-parallel (isolated) mode then its Vhvlub is
disabled and it is disconnected from the average power signal bus.

Other feedback functions on the generator regulator include HVDC current
limiting and the compensation feedback loop for generator/regulator
stability. The stability loop uses the generator exciter field current (Vfbl)
with an appropriate lead time constant that does a very good job of
stabilizing the actual circuit as well as the simulation. The current
limiting loop uses the difference between the input current to the HVDC system
(Ihvl) and a current limiting reference (Icllhv) to override the voltage
regulator when the HVDC current reaches 1.2 per unit. The current limiting
loop is scaled to generator line current, therefore the divide by 6 term on
Ihvl.

2.8.2 Paralleling, 13.2 kV DC System

The HVDC system is connected to the generator via a simulated feeder impedance named Zfeed1hv. The HVDC transformer/rectifier parameters are simulated as series drop impedance (Rhv1) and parallel excitation impedance (Rloss1hv). The load (Rloadhv) is connected to the two parallel channels through tie bus impedances (Rhv1tie). All of the HVDC impedances are reflected to the primary side of the transformer, thus the impedances are modified by the transformer turns ratio squared: $(Nturns1tr)^2$.

Rhv1 is modified to also provide the rectifier action of the HVDC rectifier bridge. If reverse current flows through Rhv1, then it assumes a very high resistance level typical of diode leakage resistance.

The output filtering on the actual HVDC system has a time constant smaller than the simulation time increment and therefore is not included in the simulation. Such a time constant would be important in a simulation that is concerned with waveform quality or ripple, but is not needed here where the desired response is the overall system reaction to major load changes, etc.

2.8.3 Paralleling, 115 VAC System

The paralleling of ac systems requires control of both amplitude and relative phase angle of the ac sources. Likewise, the error current between the output of the paralleled channels must be broken into real and reactive components to control the amplitude and angle. For this reason, the 115V ac portion of this sytem is simulated as a true ac system in which the output voltages are three-phase, 400-Hz, ac waveforms. With this type of simulation, the real and reactive load current demodulators can be simulated as the real circuit functions rather than indirect equations, which may have unknown errors or assumptions in them.

2.8.3　　　　　Paralleling, 115 VAC System　(Continued)

Each inverter is simulated as a three-phase dc-link inverter with three-phase feeders and a balanced three-phase load on each channel. By deriving the three phases in this manner, the point-of-regulation (POR) sensing can be easily simulated without the need for smoothing filters, etc. This is important because such filters are not included in the actual system and they would substantially alter the transient performance and stability of the ac system. The inverters are simulated as variable amplitude (Vmag1) and variable angle (Ang1) Thevenin sources; i.e., Vmag1*SIN(Ang1). The instantaneous angle is calculated from the system frequency (Fvco1), which in turn, is determined by a voltage controlled oscillator (VCO). Inputs from the real load division circuits and the frequency reference (Fapu) control the VCO for parallel operation. The instantaneous magnitude is controlled by the voltage regulator and the reactive load division circuits. The circuit simulation, therefore, is nearly identical to the actual circuit and gives correspondingly good results.

The voltage regulation reference for the ac system is Vrefinv1 and it has a value approximately equal to the peak amplitude of the 115V ac sinewave output. Except for scaling, this is the same as the actual regulator and sensing circuits. Constant K81 determines the gain of the voltage regulator. That is, a K81 of .5 will give full on to full off control on the voltage regulator with a POR change of 2 volts. Hence, the output will be regulated to within ± 1 volt of the reference.

The ac system is different from the standard dc-link VSCF system in that it does not use a generator in the voltage regulator loop. Instead, it uses the controlled rectifier ac-to-dc converter. The response time and impedances for this device are much different than a generator. Thus the simulation was very useful for the final design of the voltage regulator and paralleling loops. For example, the converter has no appreciable time constant and it was necessary to add a deliberate 20 millisecond pole in the front end of the converter controls for stability compensation reasons.

2.8.3 Paralleling, 115 VAC System (Continued)

The differential current sensing loop for parallel operation consists of the current transformer with turns ratio (Nturns1) and burden (Rburd1) and compensation capacitor (Cburd1). The output of this loop is demodulated into real (Vreallerr) and reactive (Vimaglerr) components with polarity sign as indicated on the schematic. The reactive error is added into the voltage regulator loop with a gain suitable to meet parallel load division specifications. Likewise, the real error is added into the frequency control loop with a suitable gain. With no real error present, the frequency will follow the external master frequency reference (Fapu) with little or no phase error.

Current limiting in the ac system is also modeled like the actual system. The inverter pole currents (I1a, I1b, I1c) are monitored, and if they exceed the reference level (Icl1) then the respective pole is "turned off." When the pole current falls below the reference, it is allowed to "turn back on." This takes care of the instantaneous overload that happens immediately after an overload is applied. On a longer term basis, the inverter link voltage is suppressed by a circuit that detects the difference between the pole currents and another reference slightly less than the Icl1 reference. The factor Kl11 is 0.95 so that current limiting will stabilize at 95 percent of the pole current limiting level. Circuit constant K112 determines the gain of this circuit.

Certain saturation voltages, etc., are very important to the behavior of the entire system and they are included in the simulation. Included in these variables are:

- Real load division integrator output saturation
- Reactive load division amplifier output saturation
- VCO input control voltage range (frequency range)
- Link controlled rectifier ceiling voltage

2.8.3   Paralleling, 115 VAC System   (Continued)

The link rectifier and filter are simulated in such a manner that only the
important time constants are considered. That is, with the rectifier
conducting and power flowing from the generator to the inverter, the filter
time constant is very small compared to the simulation time step. The
simulation is structured to ignore the link filter under this condition. When
the link rectifier is reverse biased the inverter may have such a light load
on it that the link filter may offer a time constant substantial to the system
response. The simulation will recognize such conditions and include the link
filter effects.

The load that the 115V AC system puts on the generator is simulated by
computing the inverter link current and applying it (Iinvlac) to the generator
through a feeder impedance (Zfeedlinv). The link overvoltage clamp used on
the actual inverter is simulated by a resistance (Rsnub) and associated
driving transistor.

2.8.4   Paralleling, Program Listing

The program listing for the 200/300 kVA conditioned power system simulation is
included in Appendix B. All the circuit parameters for the system are defined
in the first part of the program. The parameters were randomly selected,
within their respective tolerance levels, so that a realistic system would be
simulated. These component values and constants are not changed with each
computer run, rather they are the same unless the operator alters them in the
listing. Thus all runs can be correlated to each other. Because of the
randomized parameters, the system will run with errors in load balance on a
steady-state basis similar to the real system with no exactly matched
components. There are certain items that were deliberately set to their
tolerance extremes (opposite sign between channels) so that certain worst-case
performance parameters could be observed. For example, to see the worst
performance on the reactive load division, the voltage regulator on one
channel was set to rated plus one percent and the other to rated minus one
percent.

2.8.4   Paralleling, Program Listing   (Continued)

Each run of the simulation computes 0.075 seconds of simulated time and requires about 45 minutes real time to run. The final conditions from that run are stored in a diskett file that can be used as a starting point (initial conditions) for another run. All the state variables are stored for this purpose. Certain parameters are also printed out on a "Parameter Listing" sheet, which records all the component values for that run plus any comments regarding the run that the operator wishes to make. The final conditions of certain select variables are also printed so that the user can determine the condition of the system. For example, the real and reactive loads on each channel of the ac system are printed out. Studying the example runs in Appendix C will illustrate the others.

The most important output of the simulation is the plots of certain variables in the system. Eight are stored during the run and plotted when complete. Those selected are specified in the listing and can be altered if the user wishes. Those items selected are printed on the parameter listing along with the scale factors so that the user can correlate plots to variables. The plots are in eight different colors, which is good for the user but hard to reproduce.

2.8.5   Paralleling, Simulation Outputs

Example outputs of the parallel simulation are given in Appendix C. Each example has its two-page "Parameter Definition List" and one page of plots. The first run is a stabilizing run, which shows the steady state condition of the system with full rated load applied to the system. The second run shows the system response to a total load dump on the HVDC system only. The third run shows the response to application of full load back on the HVDC system. The fourth run is with a fault applied to channel 1 of the 115-v-ac system. The fifth run is the removal of that fault. All of the above runs are at full speed on the generators.

3.0   MECHANICAL DESCRIPTION

The conceptual layouts of the major assemblies of the electrical system have been completed. These are presented in this section.

The mechanical aspects of the generator were presented in earlier sections. However, due to the peculiarities of the design, a detailed mathematical analysis of the mechanical configuration was conducted to determine natural frequencies.

The generator design was modified as required to move the resonant frequencies out of the operating speed range. The analysis and the results are presented in the Generator Mechanical Description.

Conceptual layouts were made of the HVDC power supply, the converter/inverter (400 Hz ac) and the 28-volt dc supply.

The preliminary layouts are presented with the final mechanical layout to be completed in the next phase of the program.

3.1   Generator Mechanical Design

The generator mechanical design is predicated on an analysis of the mechanical configuration. This analysis follows.

3.1.1   Finite Element Model

Due to symmetry, only one half of the generator assembly is modeled with a proper boundary condition (Figure 3.1.1-1). The model is composed of 304 solid elements (20 nodes each) of the SUPERB program, which is an FE code of Structural Dynamics Research Company.

Figure 3.1.1-2 shows a cross-sectional view of the symmetric plan. A frame consists of three parts: an aluminum end plate (designated as 1) a magnesium in-between end plate (3) and a magnesium barrel (2). The barrel also includes the weight of the main stator. A doughnut-shaped magnesium box (4) for

3-1

3.1.1   Finite Element Model   (Continued)

connectors is supported by the driven end plate (3). The whole generator
assembly is V-clamped to the engine structure at the OD of the driving end
plate (1). A main rotor is supported by two bearings (K1 and K3), which are
clamped to both end plates (1 and 3, respectively). The main rotor consists
of three parts: two steel end plates (5 and 7) and in-between an aluminum
rotating shaft (6). The shaft also includes the weight of the main stacks
outward and the weight of excitor and PM stacks inward.

The rotating rectifiers are clamped to aluminum brackets (8), which are then
supported by the driven end plate (7). The driving end plate (5) is driven by
a stub shaft, which is not shown in Figure 3.1.1-2. The plate (5) also drives
an aluminum tube (9), which rotates with the bearing (K2).

K2 is clamped to a PM section (10) of an aluminum stationary shaft. The shaft
also consists of an excitor section (11) and a supporting plate (12). The
plate (12) is bolted to the end plate (3). The shaft also includes the weight
of the exciter and PM stators.

Three spring constants are $K1 = 21.38 \times 10^4$ lb/in., $K2 = 20.00 \times 10^4$, and
$K3 = 70.36 \times 10^4$.

3.1.2   Model Analysis

When the model analysis is applied to the model described above, five designs
emerge. Table 3.1.2-1 summarizes the first five frequencies of the designs.
Essentially the objective is to move the second mode above the maximum
operating speed of 15,000 rpm (or 250 Hz).

3.1.2.1   Design 1

The Design 1 model is shown in Figure 3.1.1-2. Figures 3.1.2.1-1 through
3.1.2.1-3 show the first three model shapes. The first and second modes (205
and 218 Hz) are within the operating range. The first mode is a movement in

AF 300 KVA GEN

AF CENERATOR ASSY

PLOT NO. 3

AF CENERATOR ASSY
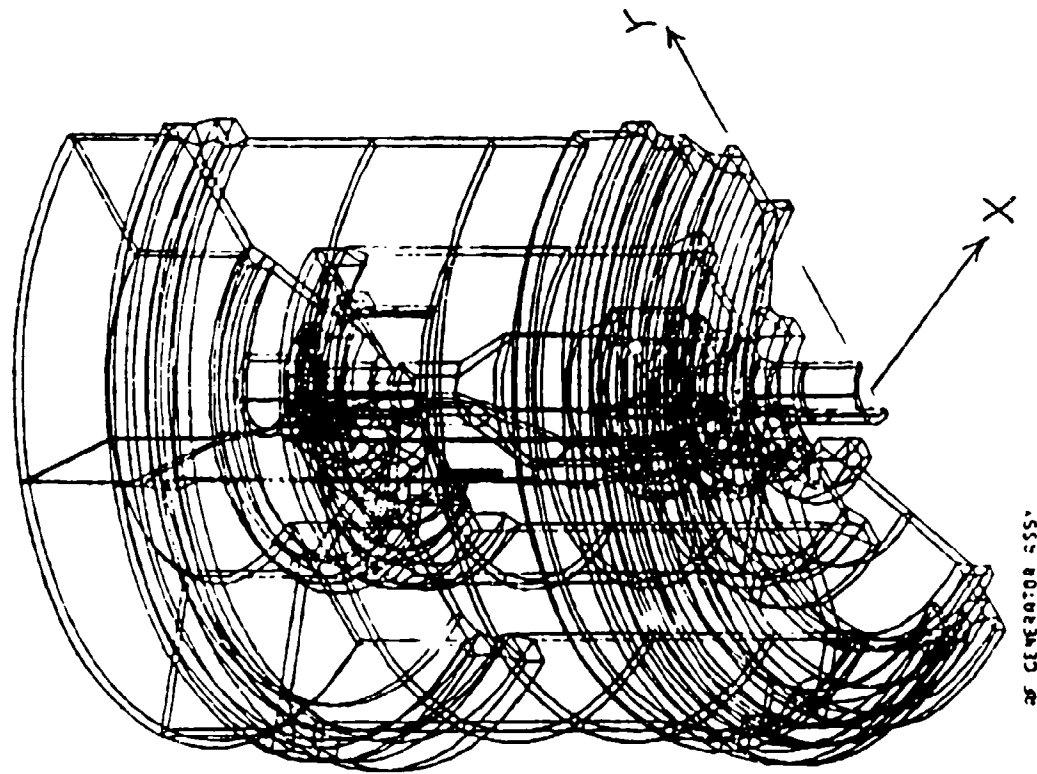
PLC NO. 1

Figure 3.1.1-1

Finite Element Model (300 kVA Generator)

Figure 3.1.1-2
Cross-Sectional View of FE Model

3-4
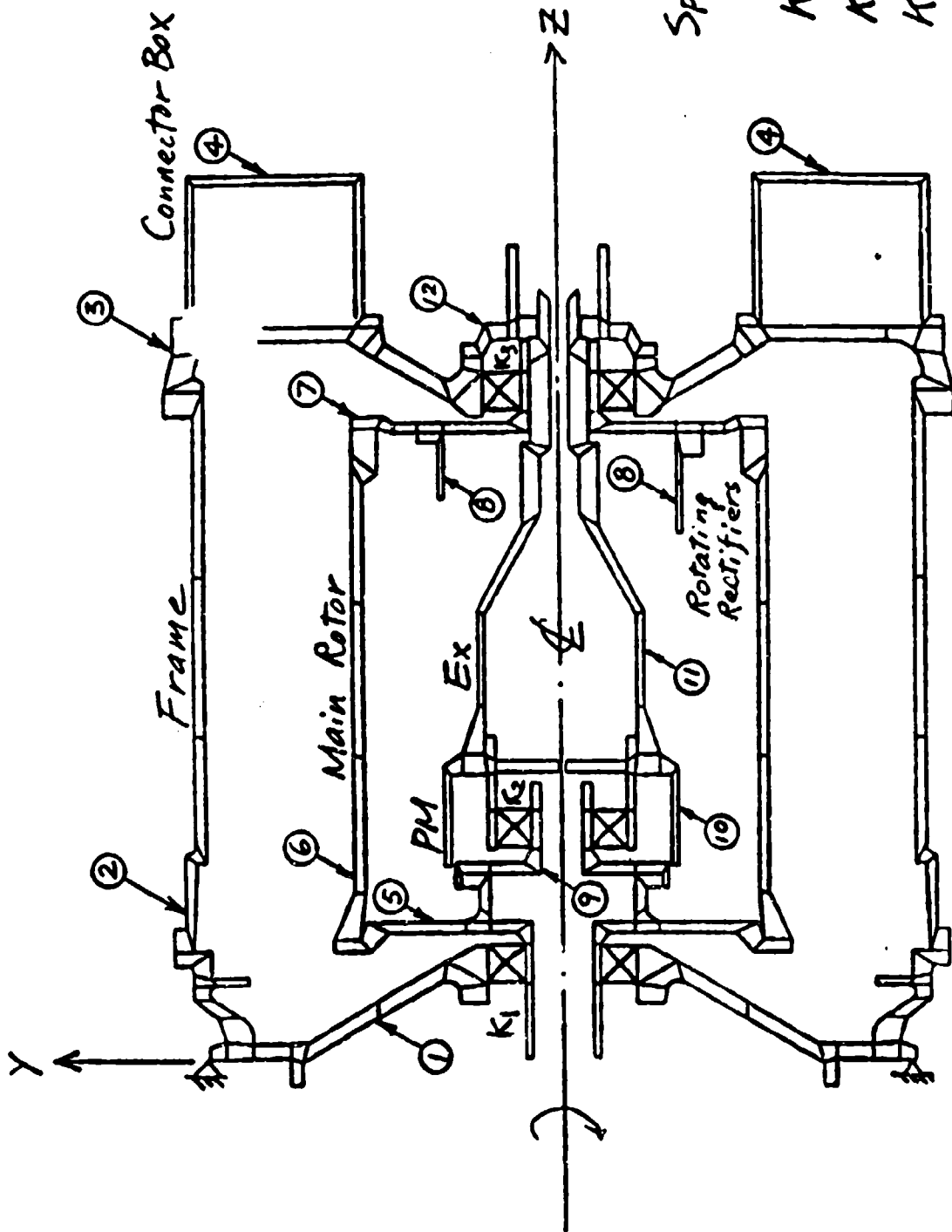
Table 3.1.2-1

Summary of Model Analysis

Modes (Hz)	Design				
	1	2	3	4	5
1	205	205	208	208	206
2	218	224	241	249	252
3	465	468	475	477	461
4	592	593	613	613	605
5	759	760	760	760	756

3.1.2.1   Design 1   (Continued)

the vertical direction (Figure 3.1.2.1-1), which is mainly sensitive to the bearing spring constants. The squeeze film damping concept is suggested to damp the vertical movement.

The second mode is a movement in the axial direction (Figure 3.1.2.1-2), which is mainly related to structural stiffness. The objective of the following design modifications is to increase this frequency above the maximum operating speed of 15,000 rpm (or 250 Hz).

3.1.2.2   Design 2

Figure 3.1.2.2-1 shows two design changes made for Design 2 to stiffen the structure in the axial direction. The thickness (A) of the steel plate (5) is increased from 0.166 to 0.200 inch and the thickness (B) of the magnesium plate (3) is increased from 0.208 to 0.250 inch.

3-5
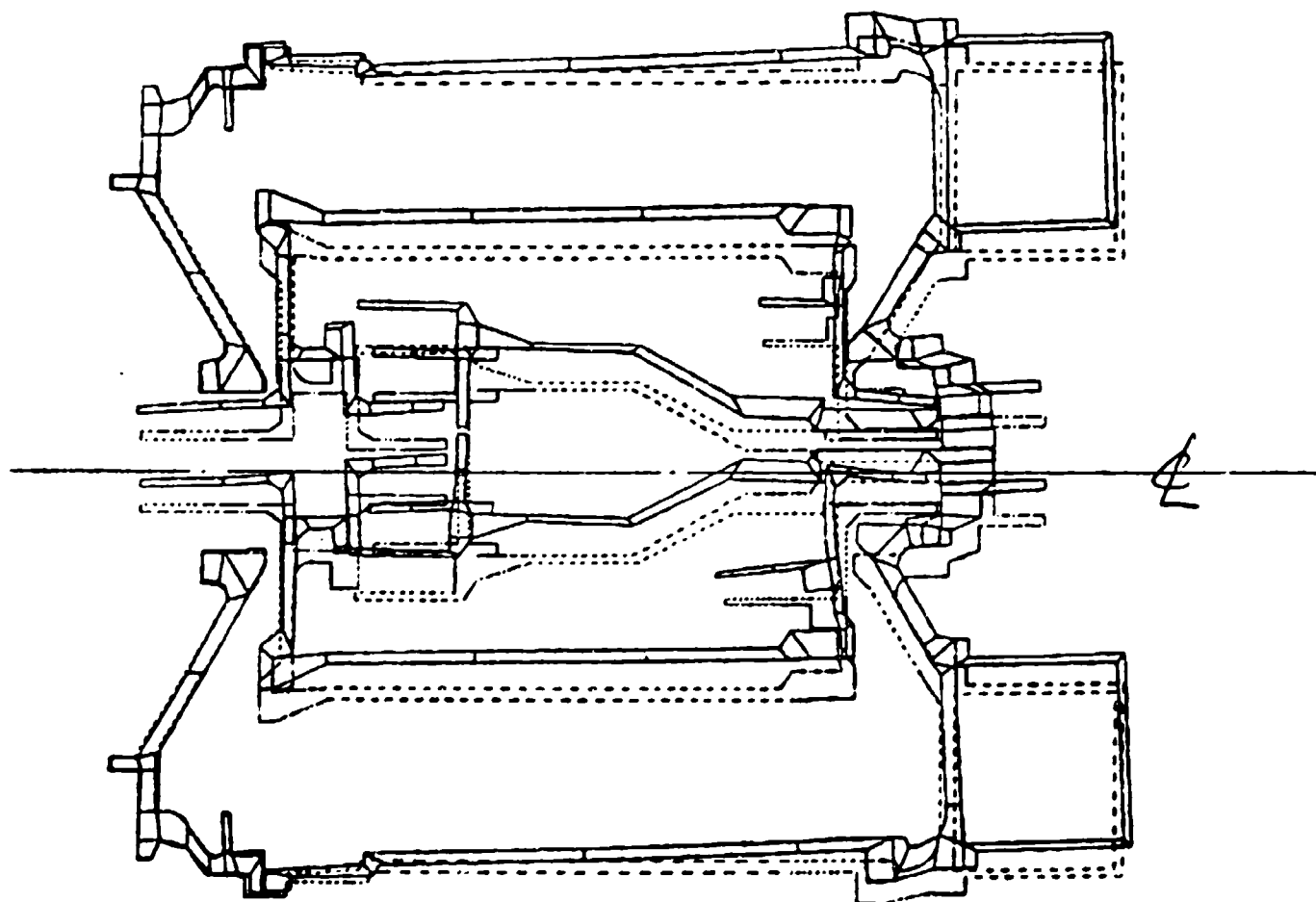
AF GENERATOR ASSY DESIGN (DYNAMIC)
SUPERB POST PLOT NO. 1
DISTORTED GEOMETRY   83/08/27   10.59.22

Figure 3.1.2.1-1

1st Mode 205 Hz - Design 1 Model

AF GENERATOR ASSY DESIGN (DYNAMIC)
SUPERB POST PLOT NO. 2
DISTORTED GEOMETRY   03/04/27   10.59.23
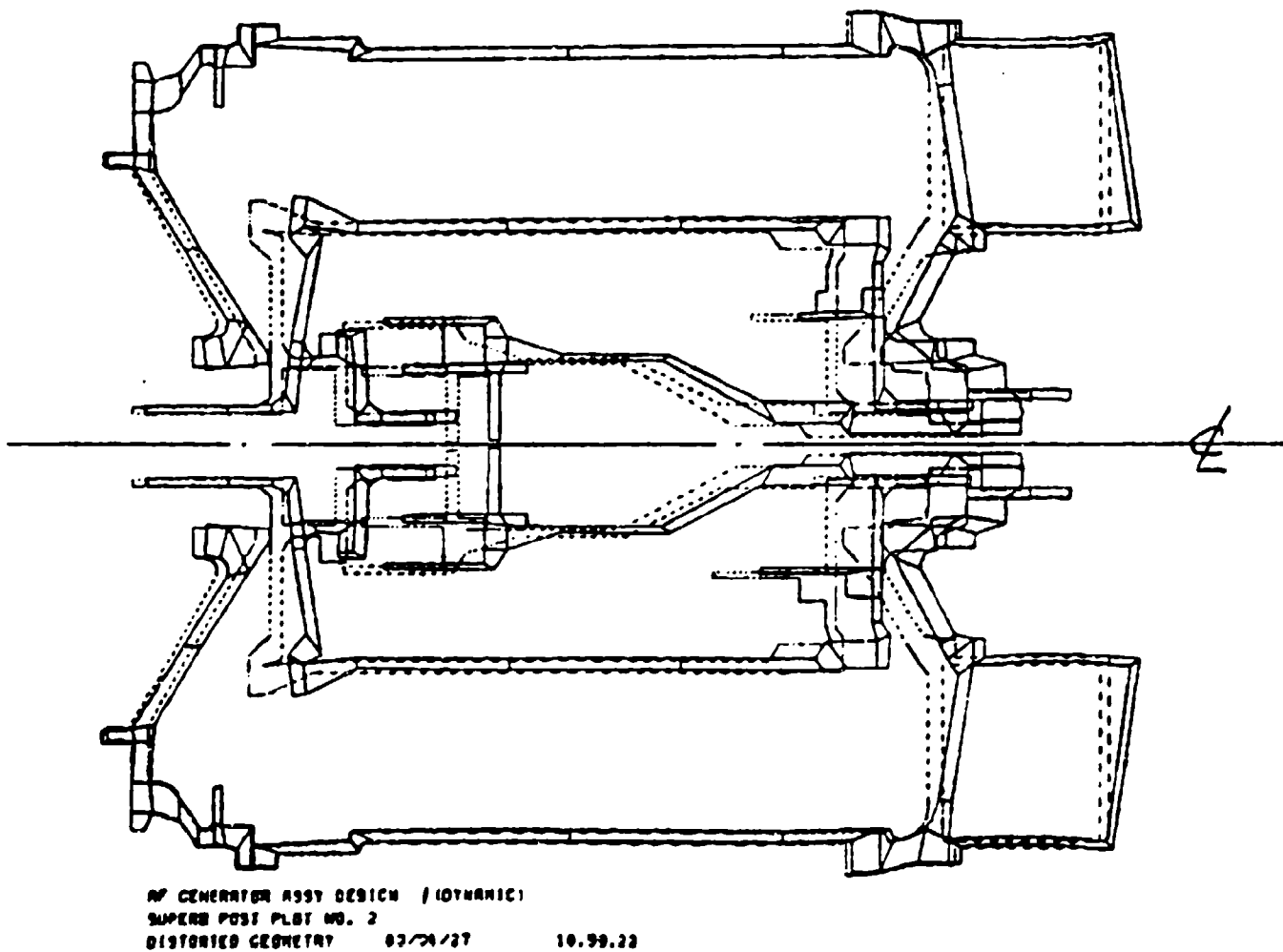
Figure 3.1.2.1-2
2nd Mode 218 Hz - Design 1 Model

AF GENERATOR ASSY DESIGN (1DYNAMIC)
SUPERB POST PLOT NO. 3
DISTORTED GEOMETRY   03/08/27   10.59.22
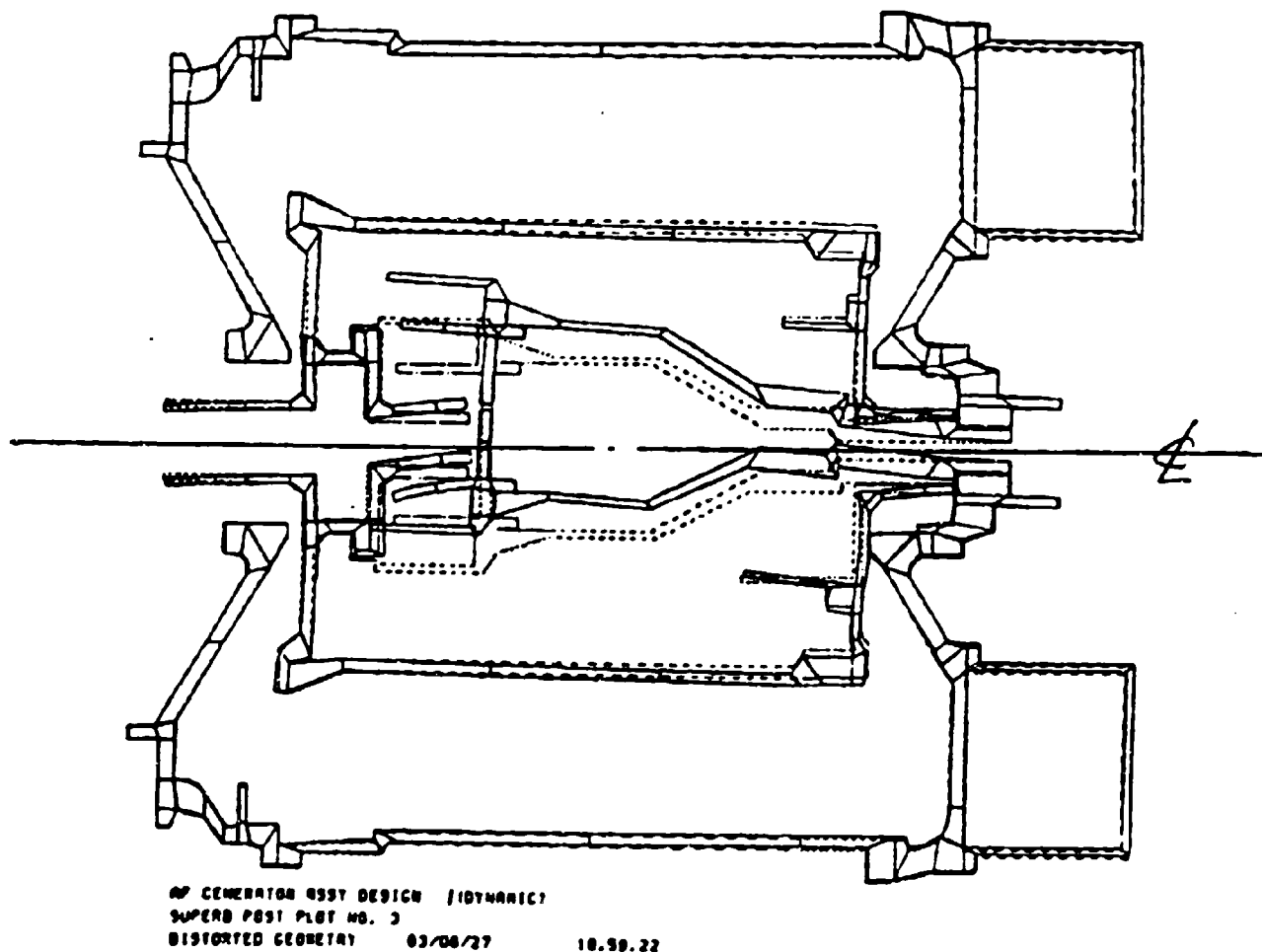
Figure 3.1.2.1-3
3rd Mode 465 Hz - Design 1 Model

3.1.2.2   Design 2   (Continued)

Figure 3.1.2.2-2 shows the first frequency is still 205 Hz. Figure 3.1.2.2-3
shows the second mode becomes 224 Hz, which is only 3% greater than that of
Design 1.

3.1.2.3   Design 3

Figure 3.1.2.3-1 shows two design changes are made for Design 3. The
thickness (A) of the steel plate (5) is further increased from 0.200 to 0.250
inch, and the driven end plate (3) is made of aluminum instead of magnesium.

Figure 3.1.2.3-2 shows the first frequency is 208 Hz. Figure 3.1.2.3-3 shows
the second mode becomes 241 Hz, which is still less than the goal of 250 Hz.

3.1.2.4   Design 4

Figure 3.1.2.4-1 shows three local changes (designated as C1, C2, and C3 in
the plates 1, 5, and 3, respectively).

Figure 3.1.2.4-2 shows the first frequency is 208 Hz. Figure 3.1.2.4-3 shows
the second mode becomes 249 Hz or 14,940 rpm, which is very close to the goal.

3.1.2.5   Design 5

Figure 3.1.2.5-1 shows two additional changes. The thickness (A and B) of the
plates (5) and (3) is increased to 0.280 inch versus 0.250 inch for the
previous design.

Total weight of the assembly is 139.65 pounds, which is composed of 101.21
pounds for the "electric weight" and 38.44 pounds for the "medium weight".
The C.G. locates in the center line 6.119 inches from the mounting face.
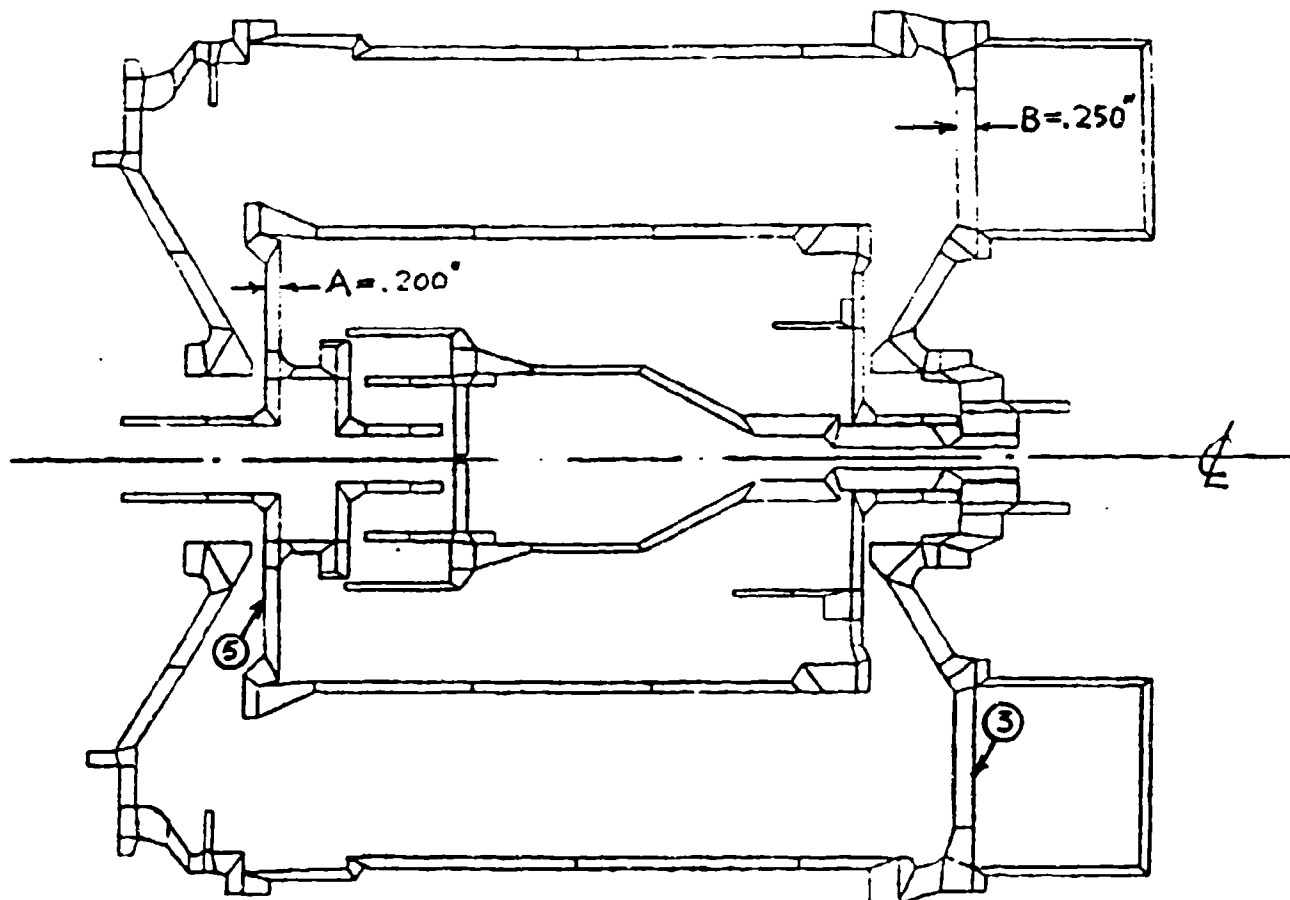
RF GENERATOR ASSY DESIGN 2 (DYNAMIC)

PLOT NO. 1

Figure 3.1.2.2-1

Design 2 Model
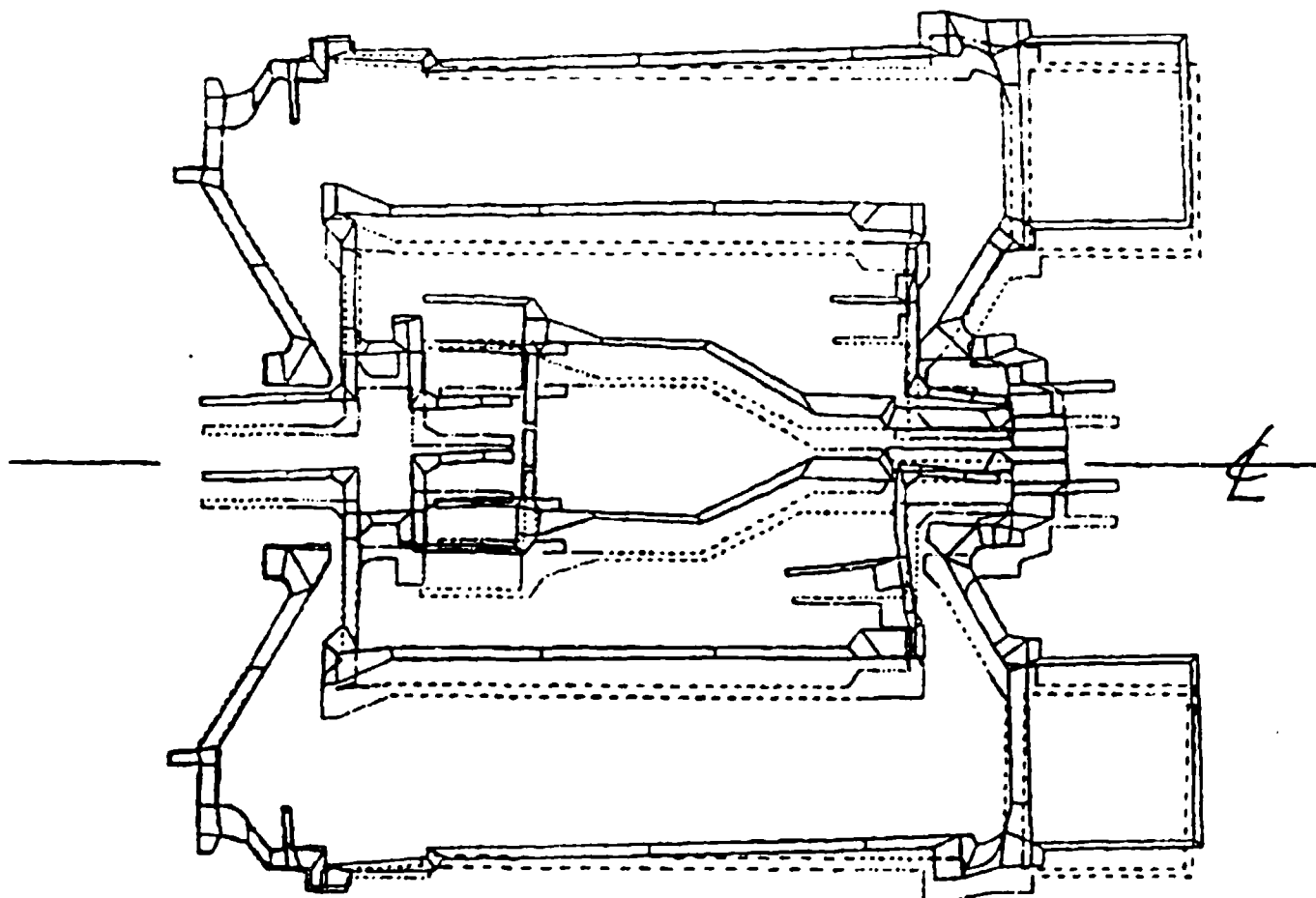
AF GENERATOR ASSY DESIGN 2 (DYNAMIC)
SUPERB POST PLOT NO. 1
DISTORTED GEOMETRY   03/07/15   18.05.17

Figure 3.1.2.2-2

1st Mode 205 Hz. - Design 2 Model

AF GENERATOR ASST DESIGN 2 (DYNAMIC)
SUPERB POST PLOT NO. 2
DISTORTED GEOMETRY   03/07/15   19.05.17
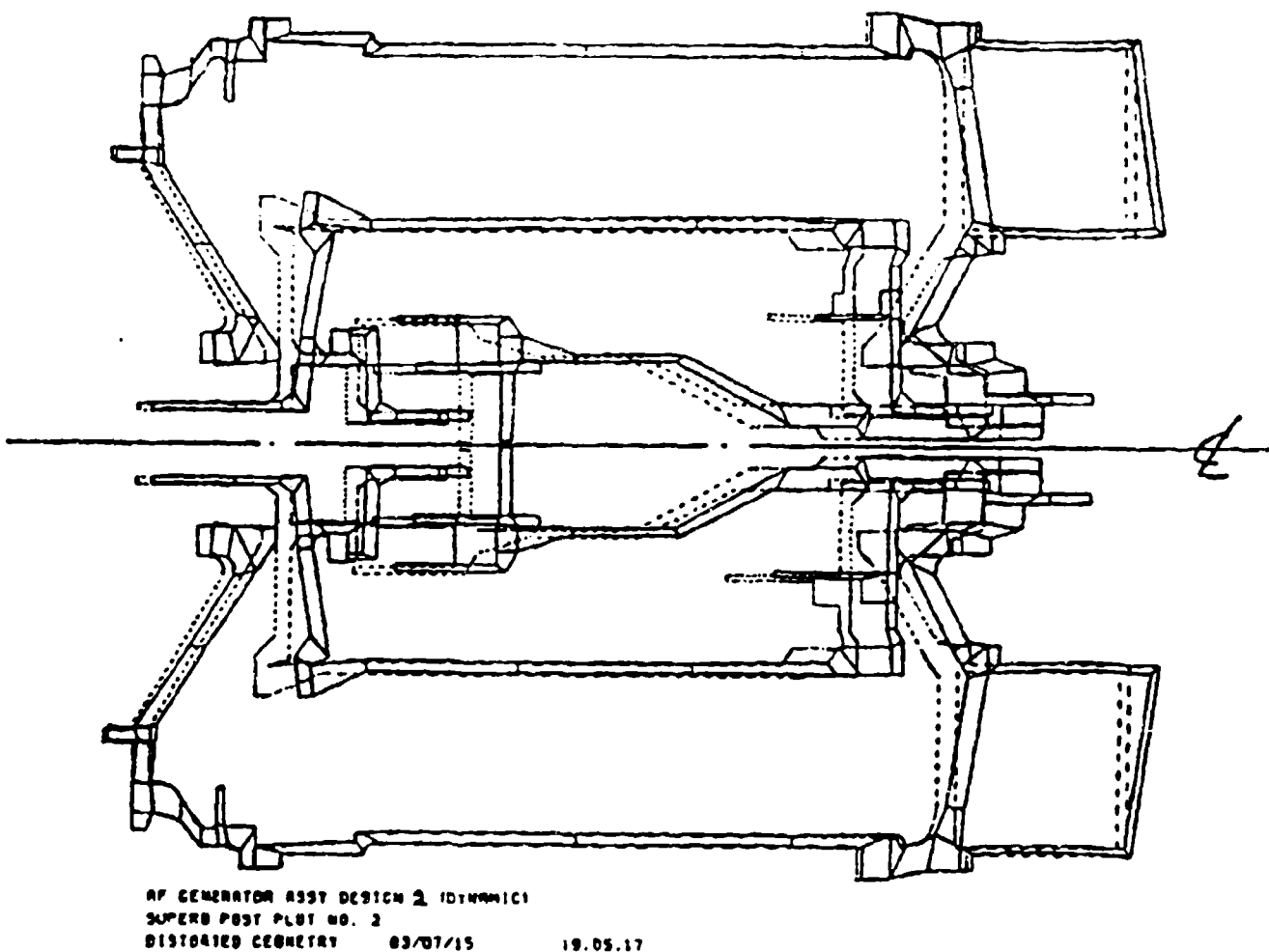
Figure 3.1.2.2-3
2nd Mode 224 Hz - Design 2 Model

AR GENERATOR ASSY DESIGN 3(DYNAMIC)
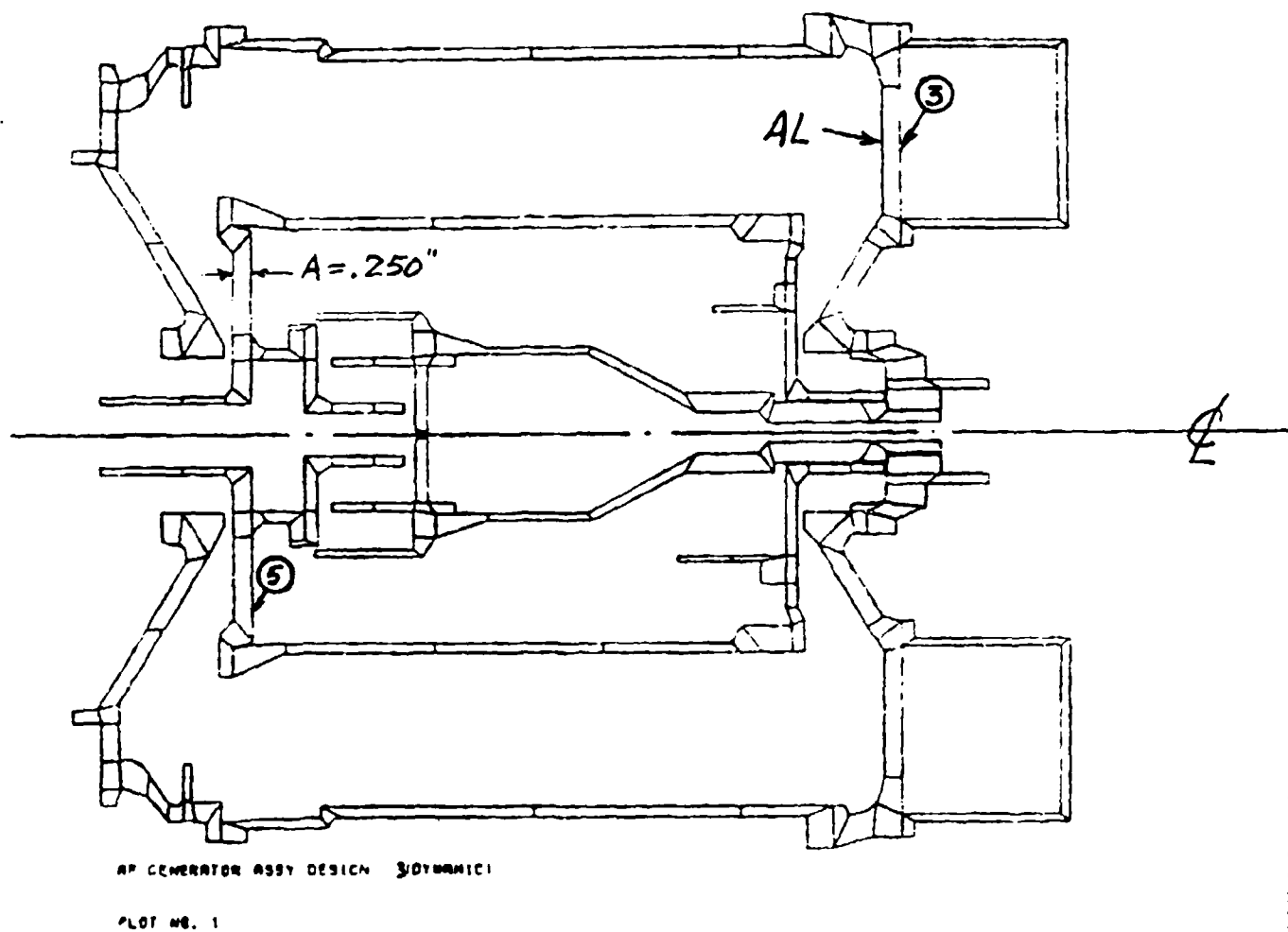
PLOT NO. 1

Figure 3.1.2.3-1
Design 3 Model

RF GENERATOR ASSY DESIGN 3 (DYNAMIC)
SUPERB POST PLOT NO. 1
DISTORTED GEOMETRY   83/07/22   20.19.13
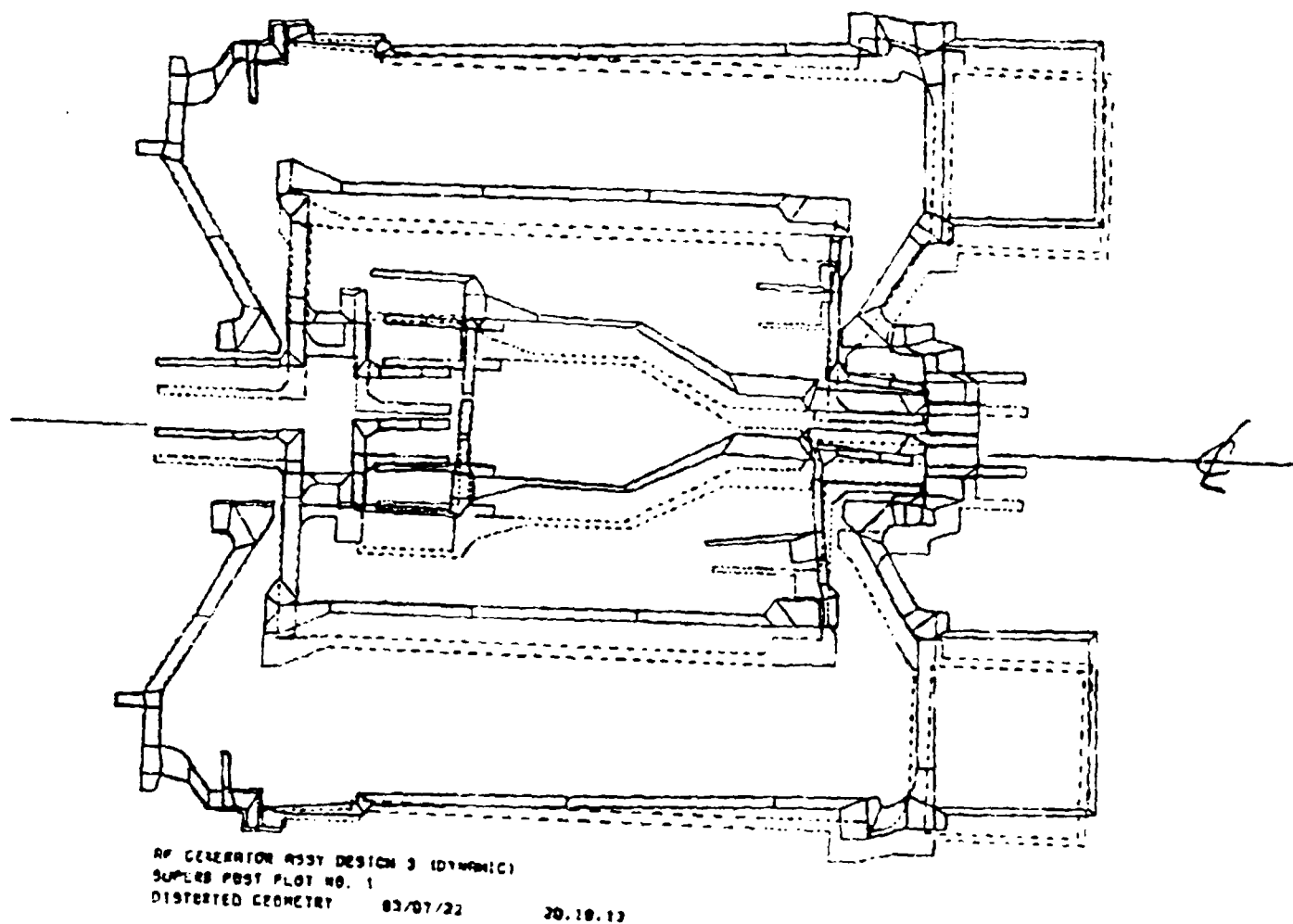
Figure 3.1.2.3-2
1st Mode 208 Hz - Design 3 Model

3-14

RF GENERATOR ASSY DESIGN 3 (DYNAMIC)
SUPERB POST PLOT NO. 2
DISTORTED GEOMETRY   83/07/22   20.10.13
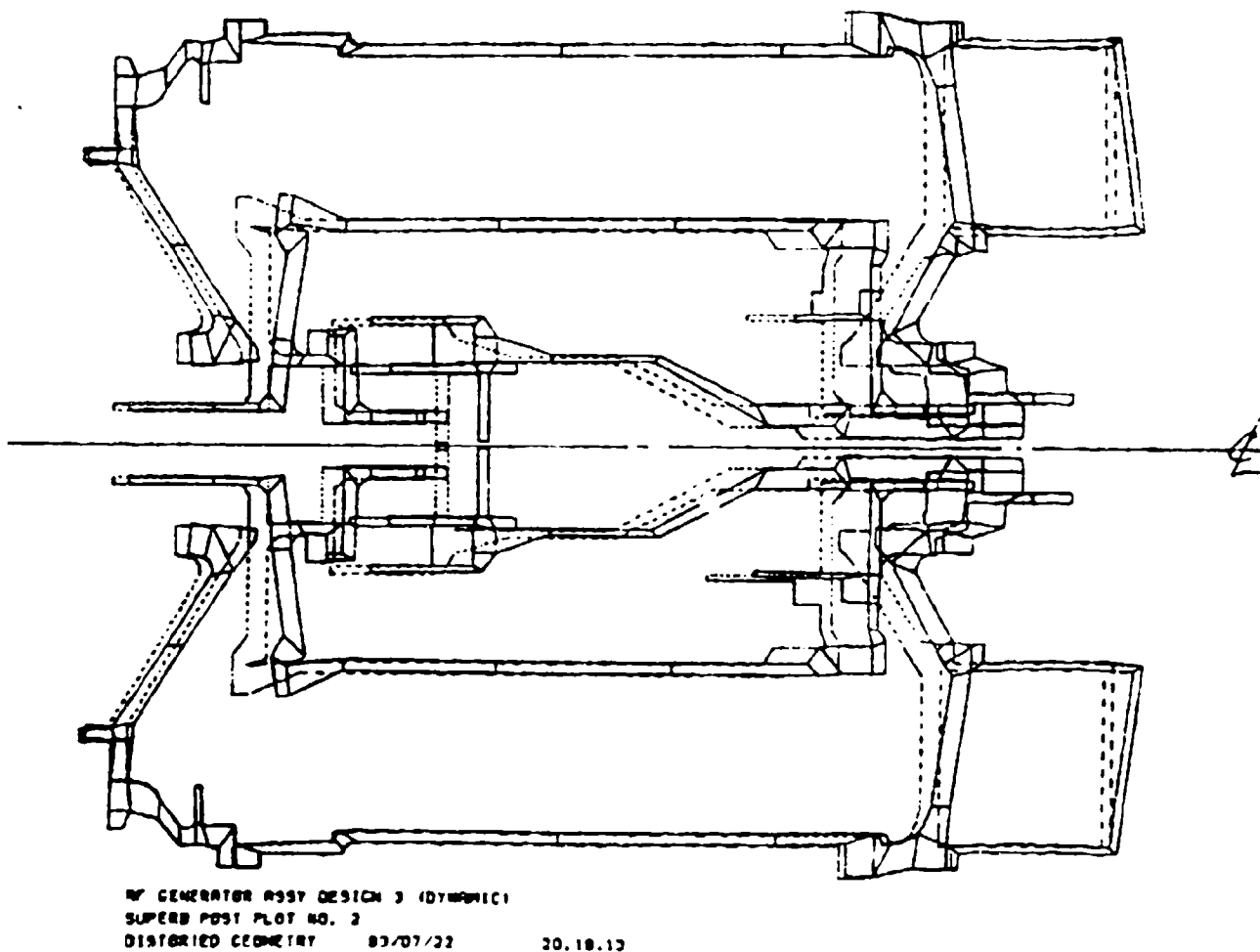
Figure 3.1.2.3-3

2nd Mode 241 Hz - Design 3 Model

CHANGE 1

C 3

A = .300

C 2

⑤

⑤
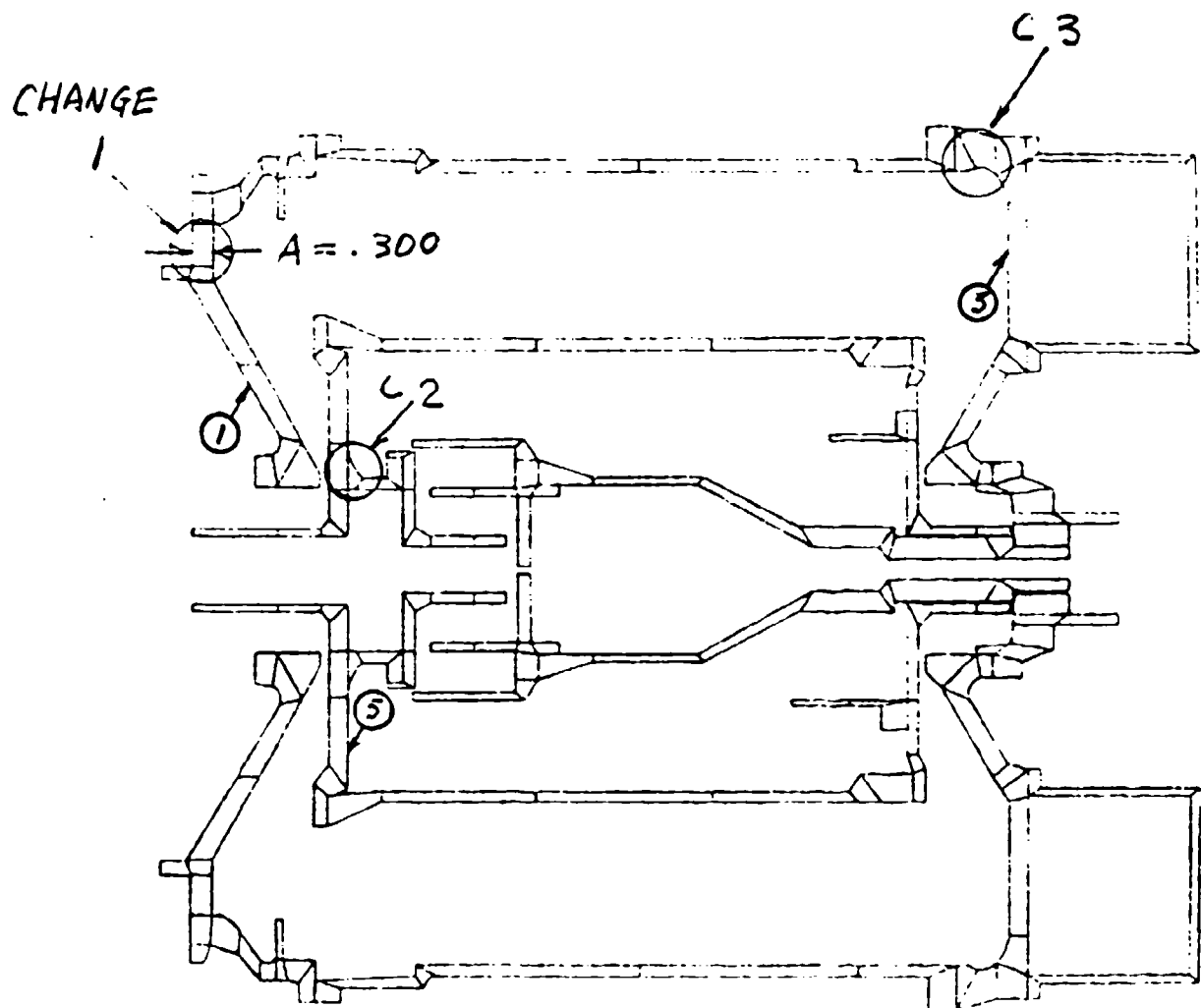
RF GENERATOR ASSY DESIGN **4** (DYNAMIC)

PLOT NO. 1

Figure 3.1.2.4-1
Design 4 Model

AF GENERATOR ASSY DESIGN 4 (DYNAMIC)
SUPERB POST PLOT NO. 1
DISTORTED GEOMETRY   83/07/29   23.43.15
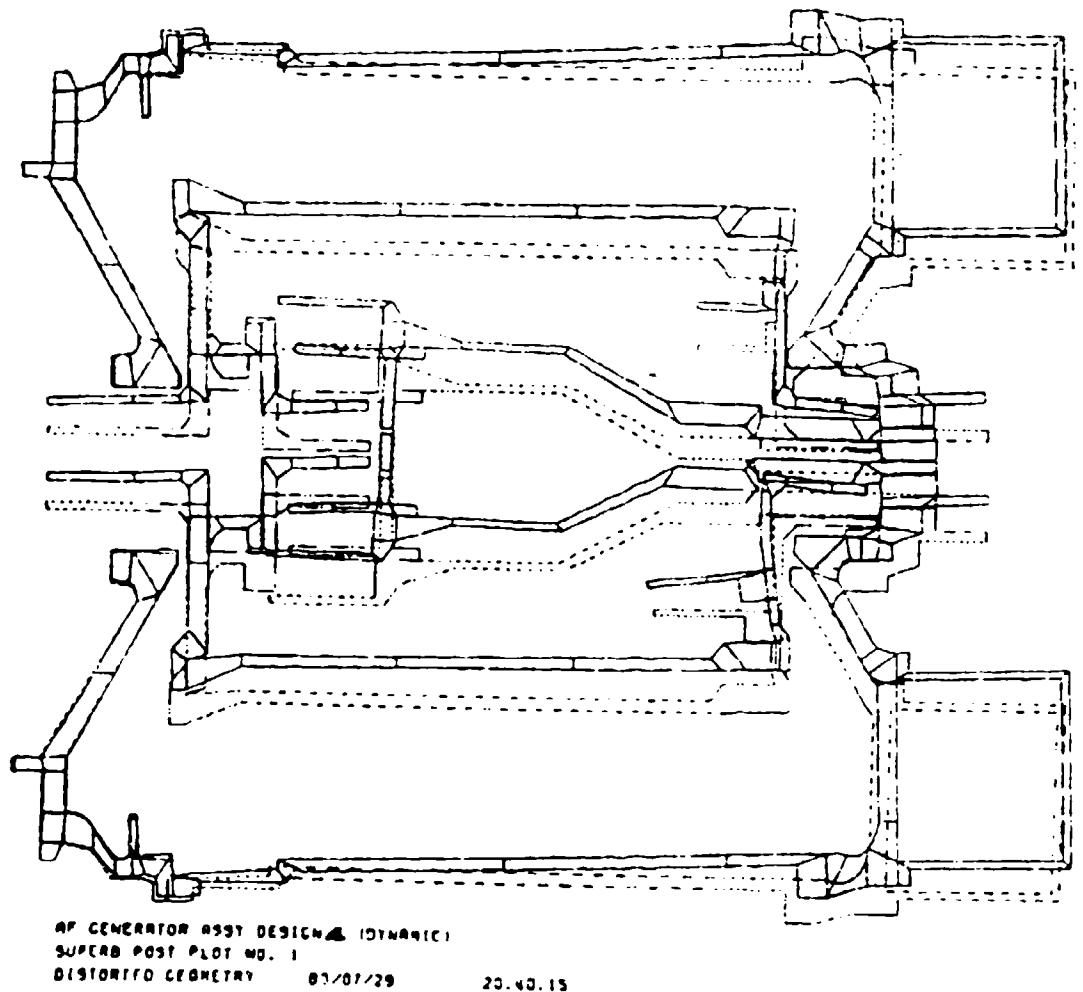
Figure 3.1.2.4-2

1st Mode 208 Hz - Design 4 Model
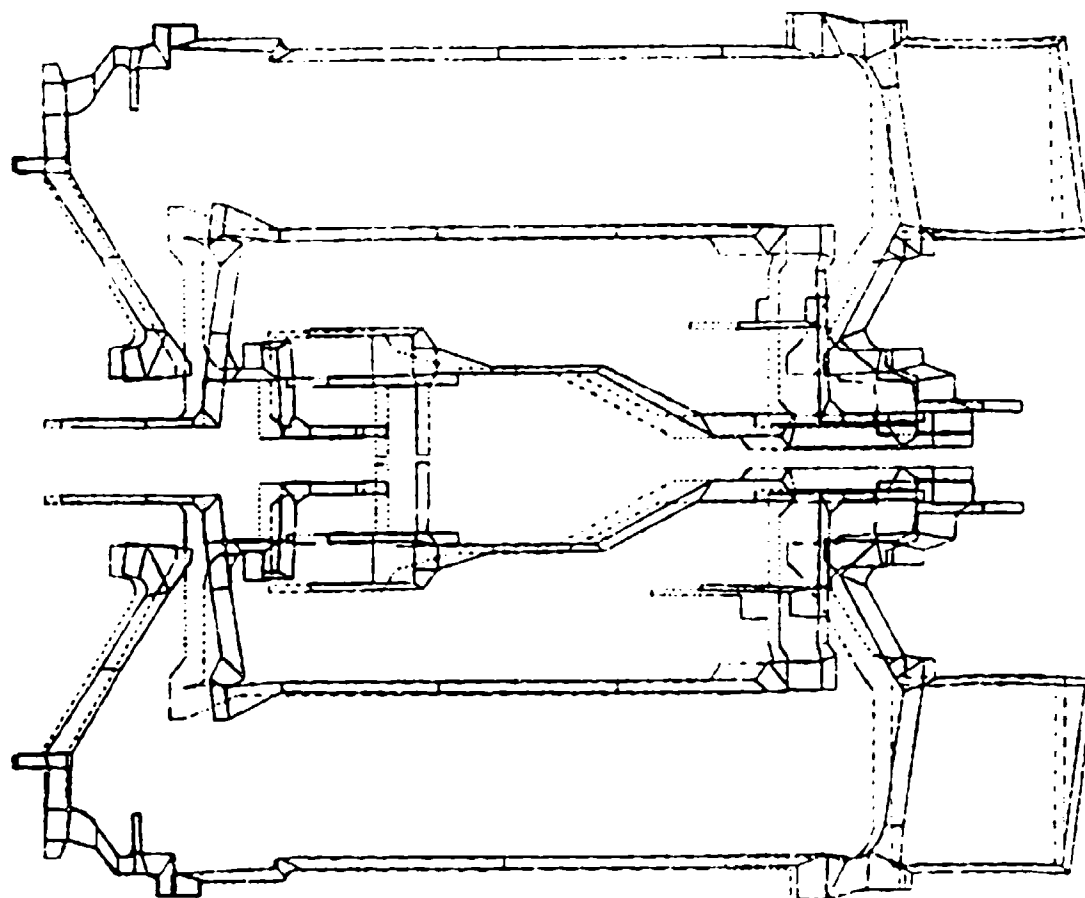
RF GENERATOR ASSY DESIGN 4 (DYNAMIC)
SUPERB POST PLOT NO. 2
DISTORTED GEOMETRY   83-07-29   20.40.15

Figure 3.1.2.4-3

2nd Mode 249 Hz - Design 4 Model

6.119"

.300

B =.280

A =.280

.250

CG

℄

⑤

③
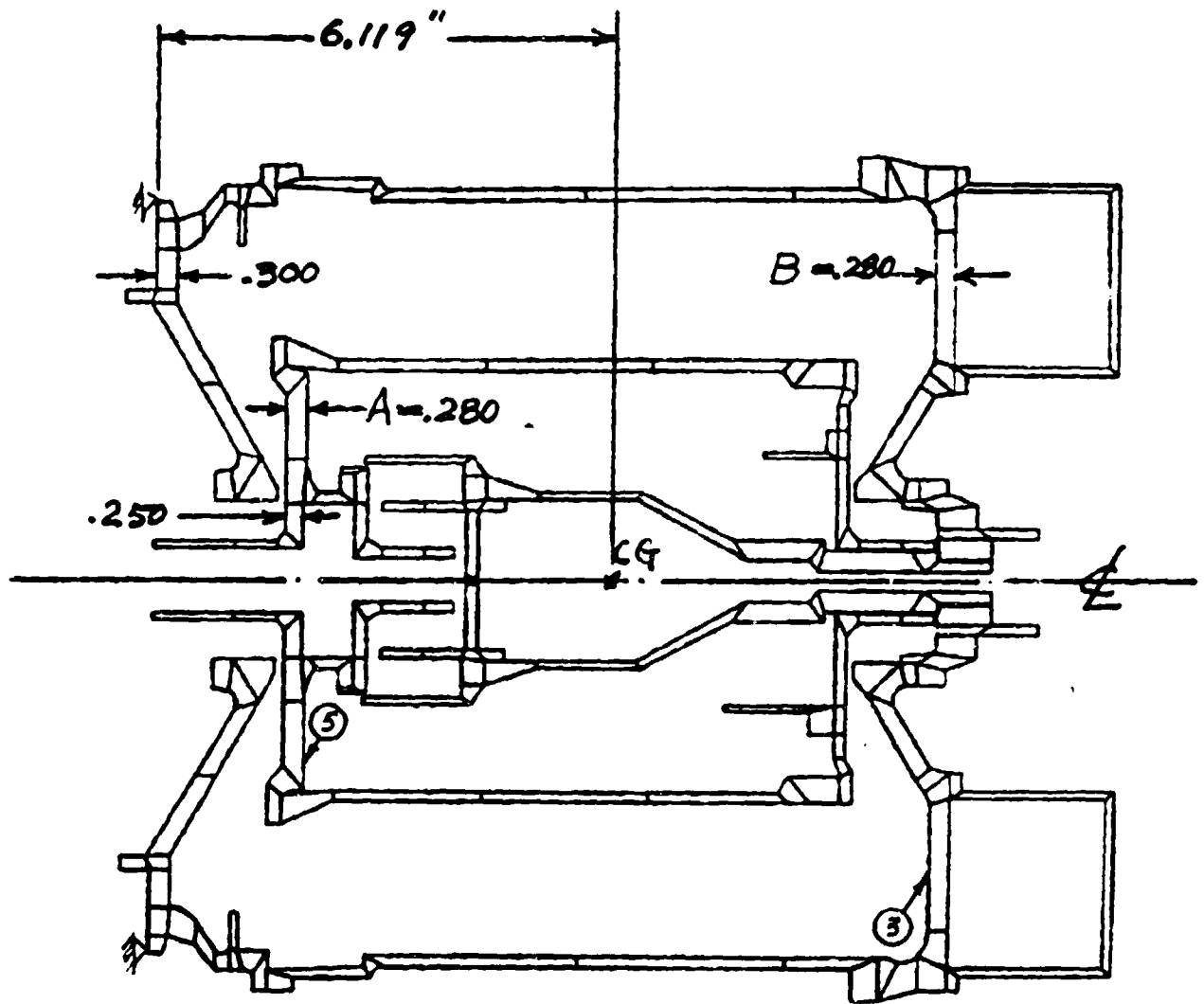
AP GENERATOR ASSY DESIGN 5 DYNAMICS

PLOT NO. 1

Figure 3.1.2.5-1
Design 5 Model

3-19

3.1.2.5   Design 5   (Continued)

Figures 3.1.2.5-2 and 3.1.2.5-3 show that the first and the second natural
frequencies are 206 Hz and 252 Hz, respectively. Finally, only the first mode
is below the maximum speed (15,000 rpm). This mode movement is to be damped
by the squeeze film concept applied to the bearings.

3.1.3   Structural Analysis

The objective of the structural analysis is to determine the load capacity in
both vertical and axial directions. The capacity is determined by the
yielding of critical material involved.

Figure 3.1.3-1 shows the vertical loading capacity is 109 g, which is based
upon the yielding strength (100 KSI) of steel (AMS 6274, RC =32-38). The
maximum stress in the material is 99.16 KSI under the condition of 109g.

Figure 3.1.3-2 shows the axial loading capacity is 124g, which is based upon
the same material yielding strength (100 KSI). The maximum stress at the
corner is 99.52 KSI under the condition of 124g.

3.1.4   Conclusion

The assembly design final is Design 5, which has only one basic frequency of
206 Hz within the operating speed range. The movement of this mode is to be
damped by the squeeze film concept applied to the bearings.

The estimated weight of the assembly is 139.65 pounds, which does not include
the weight of the three bearings and the stub shaft. The load capacities are
109g in the vertical direction and 124g in the axial direction.
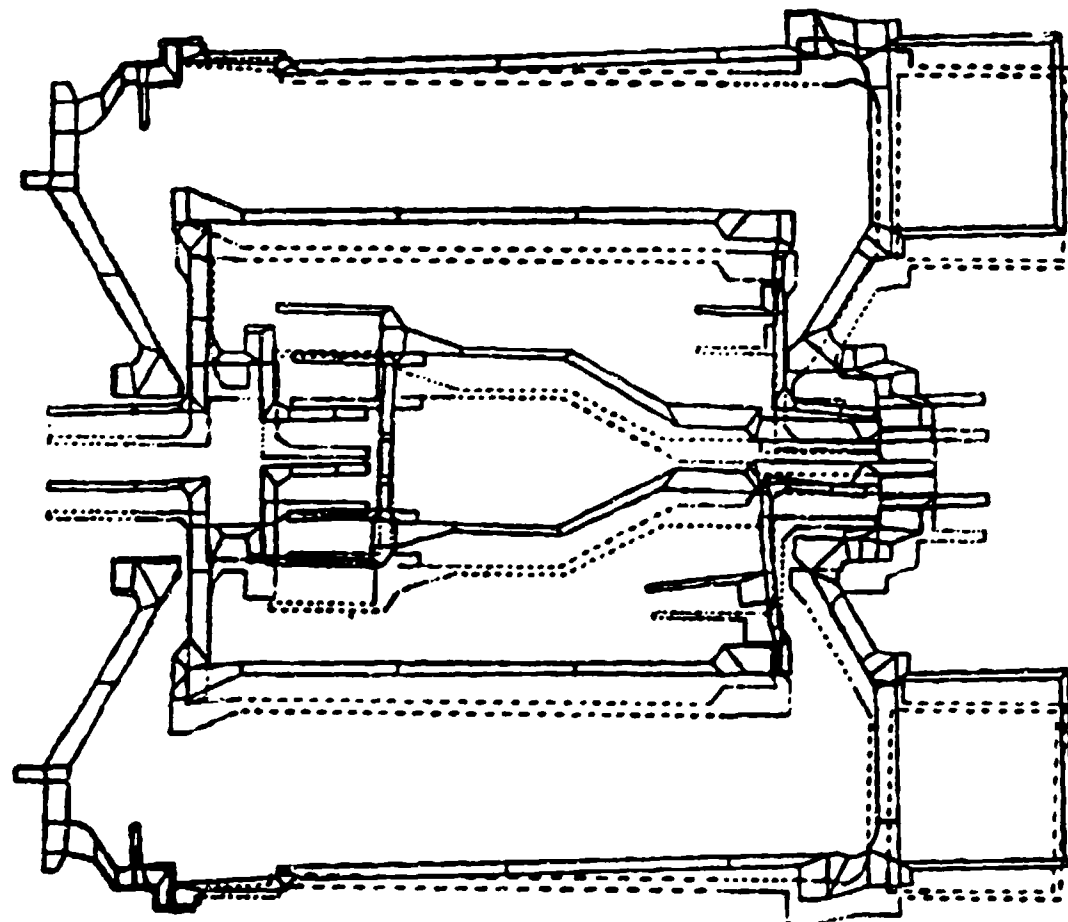
Figure 3.1.2.5-2

1st Mode 206 Hz - Design 5 Model

3-21
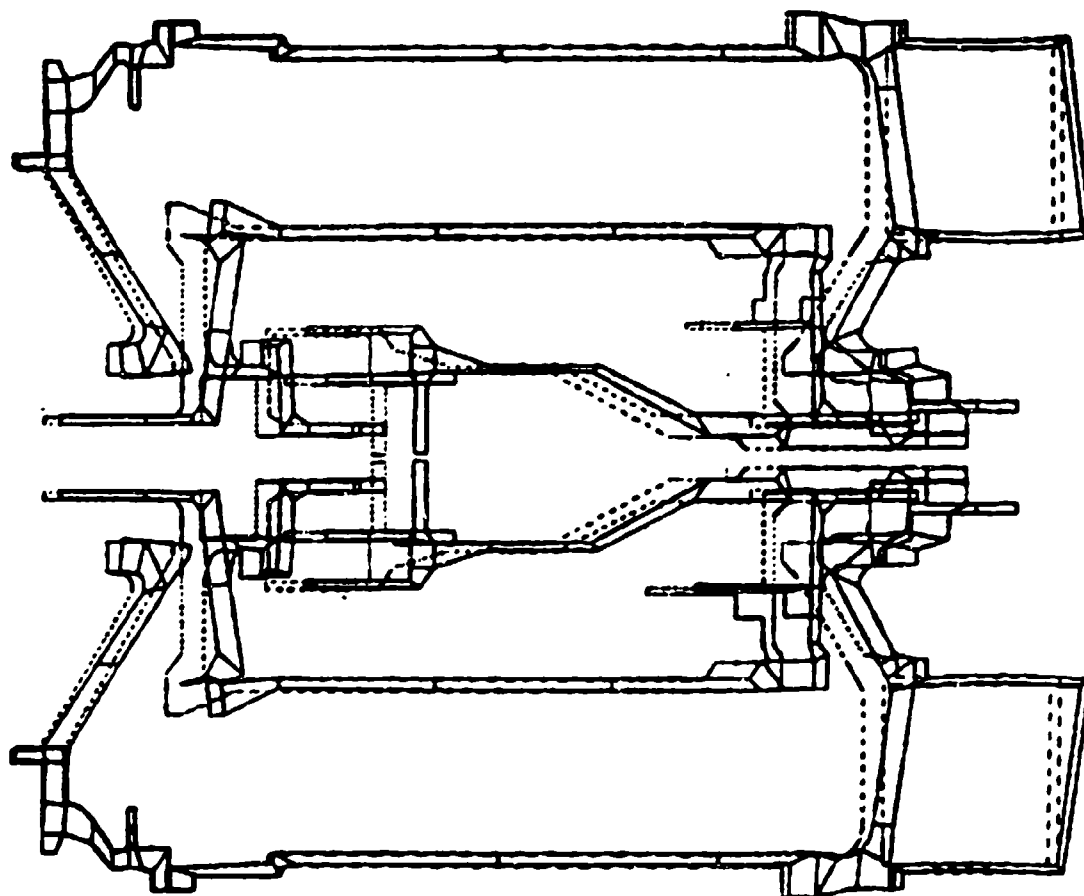
DF GENERATOR POST DESIGN 5 (DYNAMIC)
SUPERD POST PLOT NO. 3
DISTORTED GEOMETRY   93/09/27   18.09.03

Figure 3.1.2.5-3

2nd Mode 252 Hz - Design 5 Model

109 g
Vertical

99160 psi
(St.)

of generator post design 5 (static)
super post plot no. 1   loading case 1
distorted geometry   83/08/27   15.30.34
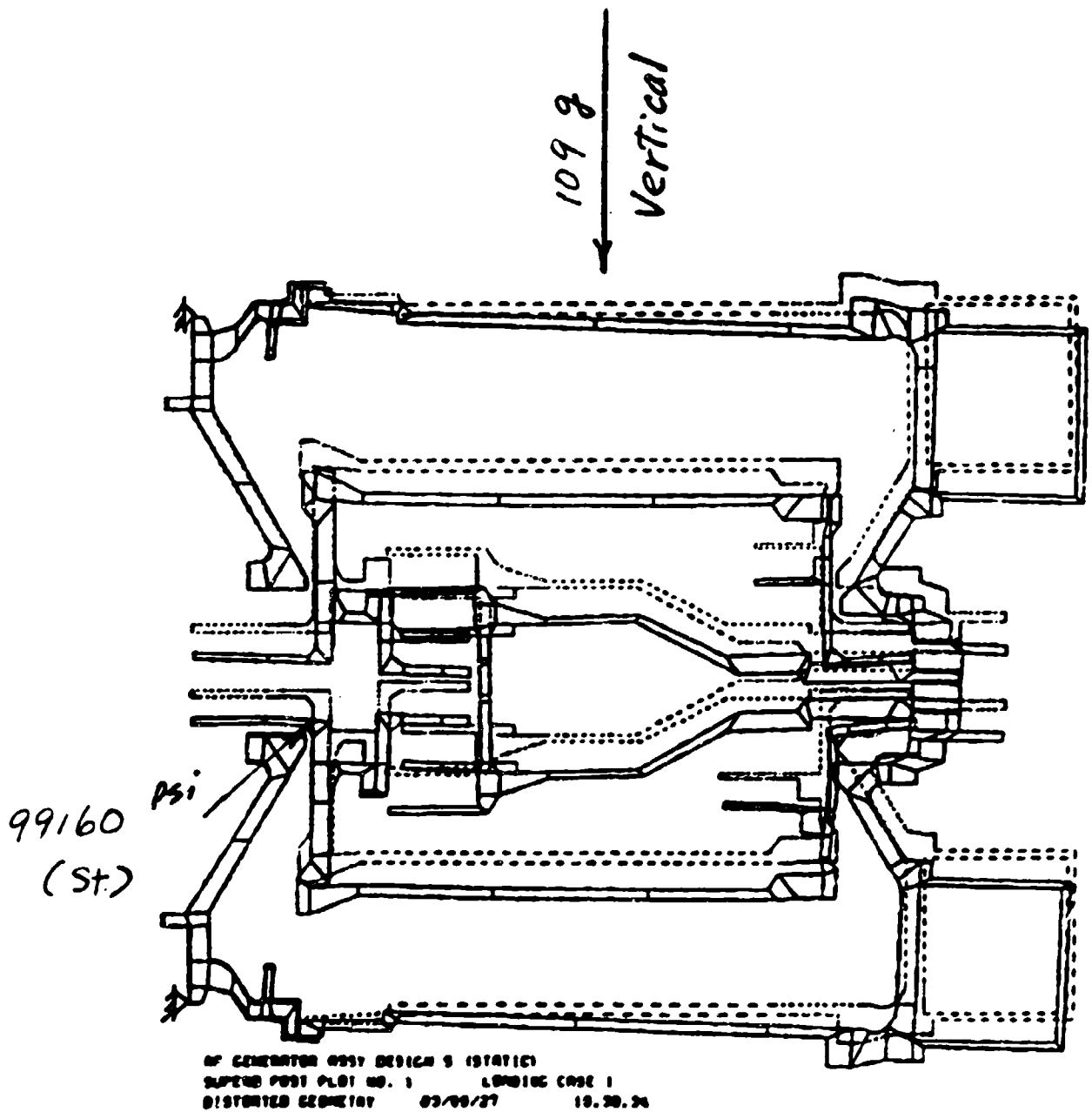
Figure 3.1.3-1
Vertical Loading Capacity - Design 5 Generator

$124\, g$

Axial

$9952\, Psi$

$(St.)$
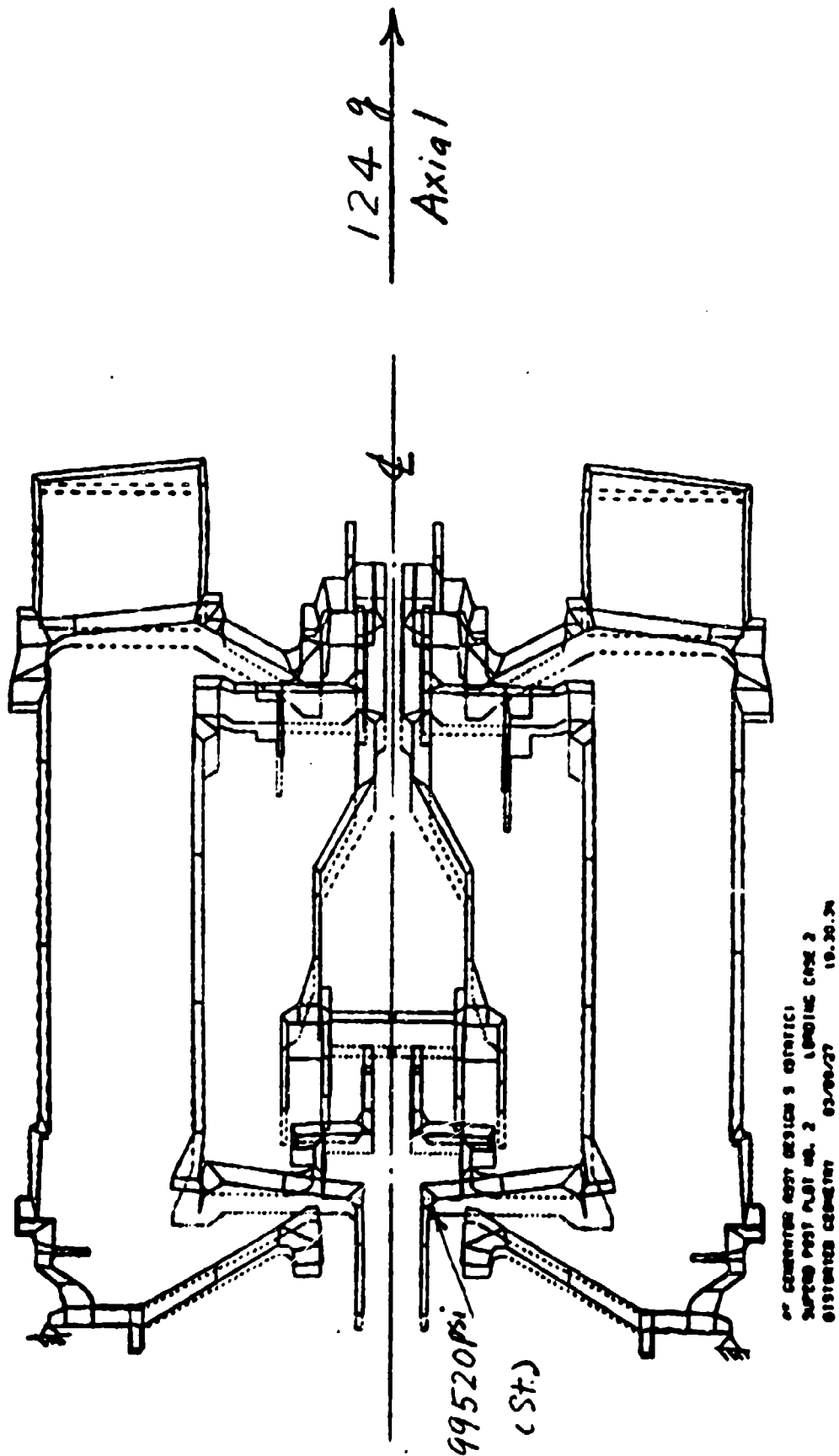
Figure 3.1.3-2

Axial Loading Capacity - Design 5 Generator

3-24

3.2 Generator Control Unit

The generator control unit outline and layout are shown in Figures 3.2-1 and 3.2-2. The unit is a fully enclosed assembly of plug-in printed circuits. The unit is designed for easy access. This is achieved by using 1/4-turn fasteners on the cover. With the removal of the top cover, any printed circuit module can be modified or removed without disturbing any other module. The sides and front panel mount to a 1/8 inch thick flat aluminum plate. The front panel is used for mounting three transformers and the system interfacing connector.

There is a total of six two-sided printed circuit modules that all plug into a mother board.

The mother board is mounted to an aluminum bracket that encloses it. The mother board contains all wiring between the functional modules and all wiring from the modules to the external connector. Connections on the mother board are made by wire wrapping to pins on the back side of the board connectors. The boards all use polarized-edge, guide-type connectors.

All components and printed circuit modules are cooled by natural convection.

3.3 400 Hz Converter/Inverter Mechanical Description

Figure 3.3-1 shows the outline of the 400 Hz inverter, and Figure 3.3-2 shows the inverter layout. The inverter unit is divided into two sections; one section that is cooled by oil, and one section that is cooled primarily by surrounding air. The sealed housing will be made from a large platform and a five-sided enclosure for the lab unit. The platform contains oil distribution ducts, and mounting points for the various subassemblies. For a production unit, the housing could be cast from aluminum using plaster mold techniques, but the lab unit prototype will be machined from half-inch thick plate stock. The spraying nozzles are located in machined plates that mount over the oil distribution ducts on the half inch mounting plate. Handles are located at
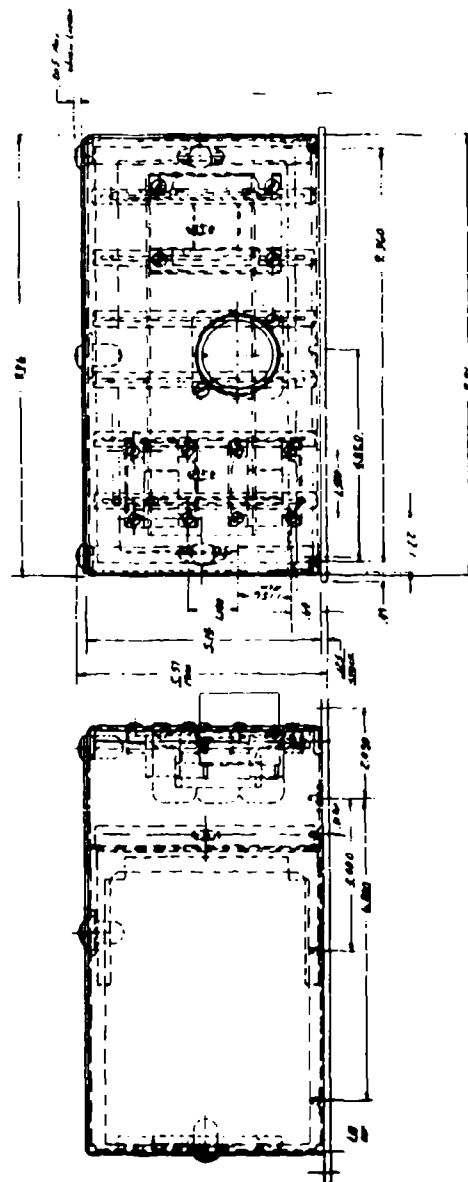
Figure 3.2-1
GCU Outline

Figure 3.2-2
GCU Layout

CONNECTORS
17 SHELL SIZE
MS 27470

GENERATOR INPUT
TERMINAL DESIGNATIONS
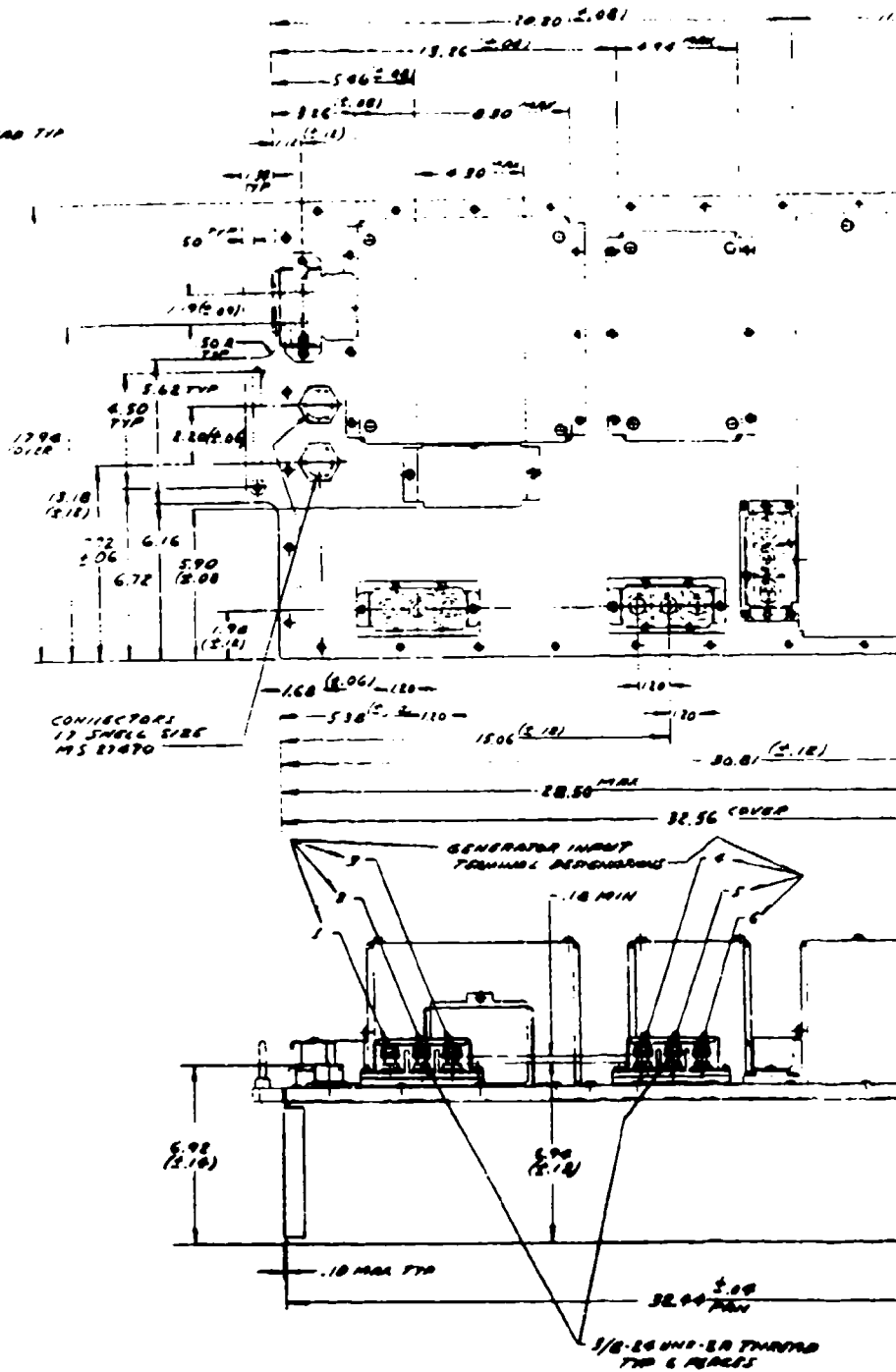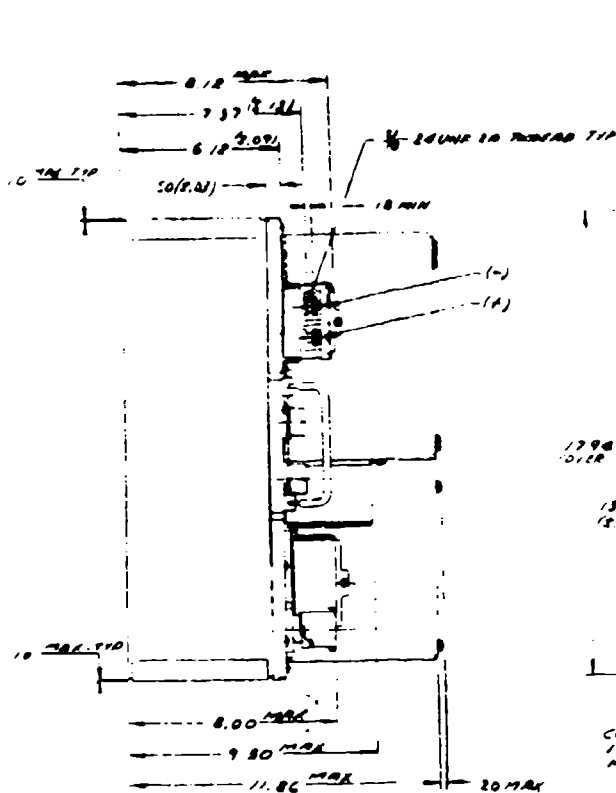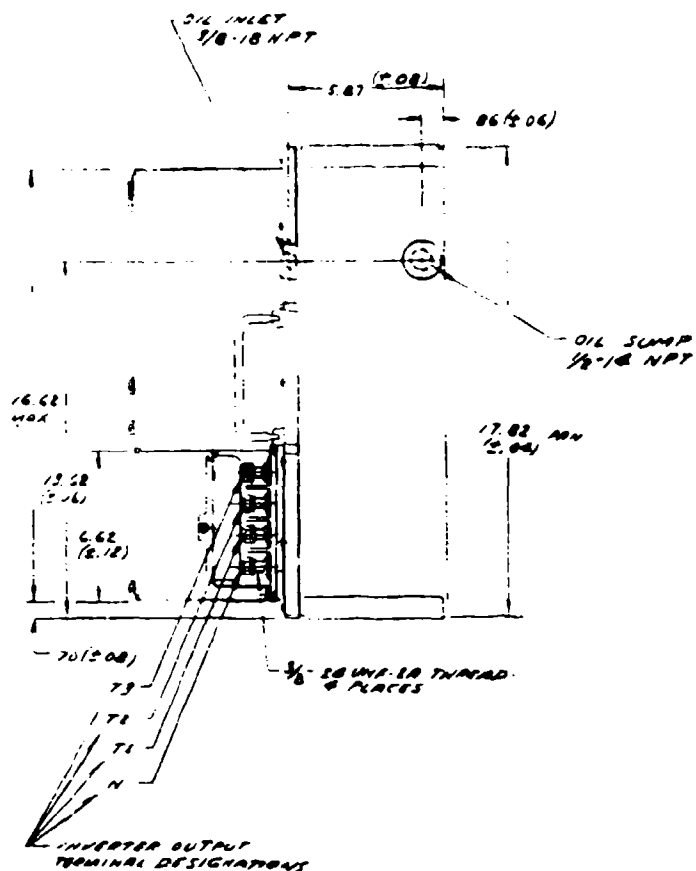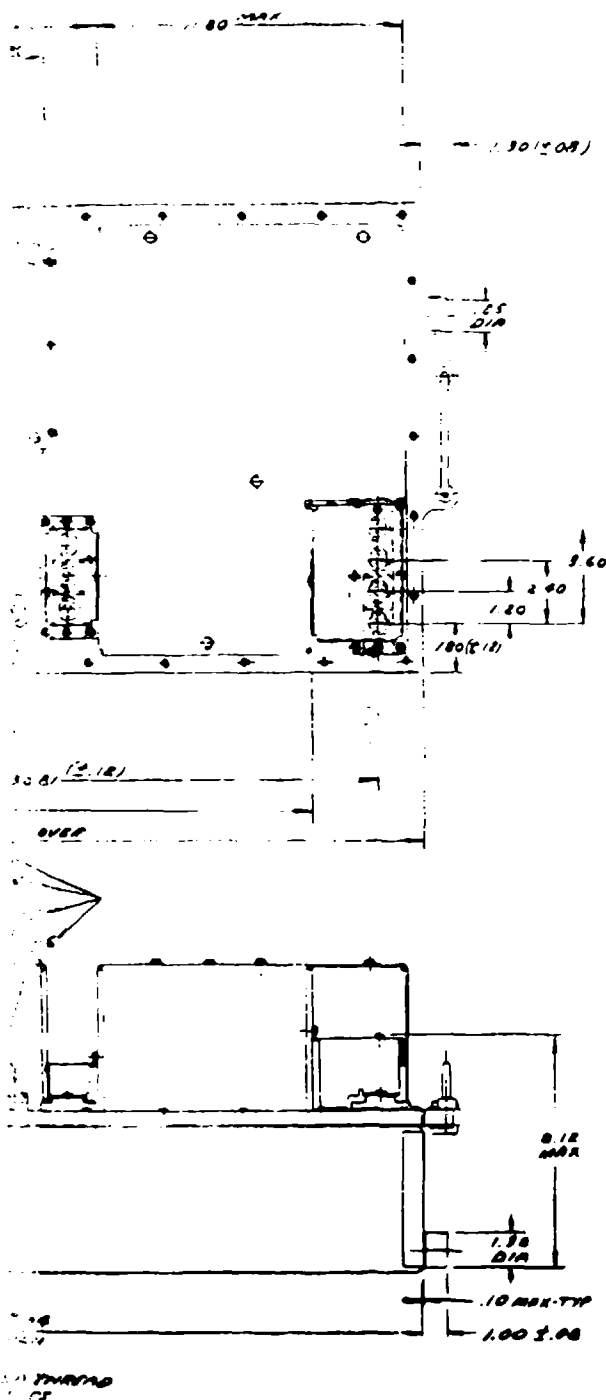
Figure 3.3-1
400 Hz Inverter Outline

400 HZ INVERTER LAYOUT

Figure 3.3-2

3-30

400 HZ INVERTER LAYOUT

ED 404333

Figure 3.3-2

SECTION A-A
TYP - 6 PLACES
SCALE 2/1

Figure 3.3-2

400 HZ INVERTER LAYOUT

ED404333

both ends of the plate to aid in maintainability, and a gasket seals the oil
pan type cover against the mounting plate.   This allows for easy access to the
various subassemblies.

Six subassemblies will be housed within the sealed enclosure.   They are a
preregulator assembly, three identical inverter pole assemblies, one neutral
forming transformer, and one output inductor assembly.   All are cooled by
direct impingement of MIL-L-7808 oil from the spray nozzles.

3.3.1   Preregulator Assembly Mechanical Description

Figure 3.3.1-1 shows the configuration of the preregulator assembly.   Twelve
size 6 fast-switching "hockey puck" SCRs are clamped between copper bus
bar/heat sink plates.   Gimbal spacers are used on the ends of the stacks to
ensure that an even load is applied to the semiconductors.   One-quarter inch
diameter draw bolts are used along with spring clamps to apply the 1000/1400
pounds force required to meet the specification requirements of the
semiconductors.

Slotted mounting brackets are attached to the ends of the stacks to allow for
tolerance in mounting to the aluminum plate.   These mounting brackets also
have tabs bent over on the side for printed circuit boards to mount.   There
are two printed circuit boards mounted in this fashion off each stack.   One is
"piggy-backed" on top of the other with standoffs.   These four printed circuit
boards contain the gate drive transformers and snubber components.   The
control functions for the preregulator assembly will be housed in a remote
unit (inverter control unit).   The vertical orientation of the printed circuit
boards is desirable due to the oil cooling provisions.

Mounted between the two symmetrical stacks of semiconductors is the magnetic
assembly.   This consists of two individual subassemblies, one the interphase
transformer, and the other the filter inductor.   This magnetic assembly has
independent mounting provisions from the stacks.

PREREGULATOR

DFTM - P. Hanu 83/66

ED 404328

INDUCTORS NOT ATTACHED TO POLE ASSY.
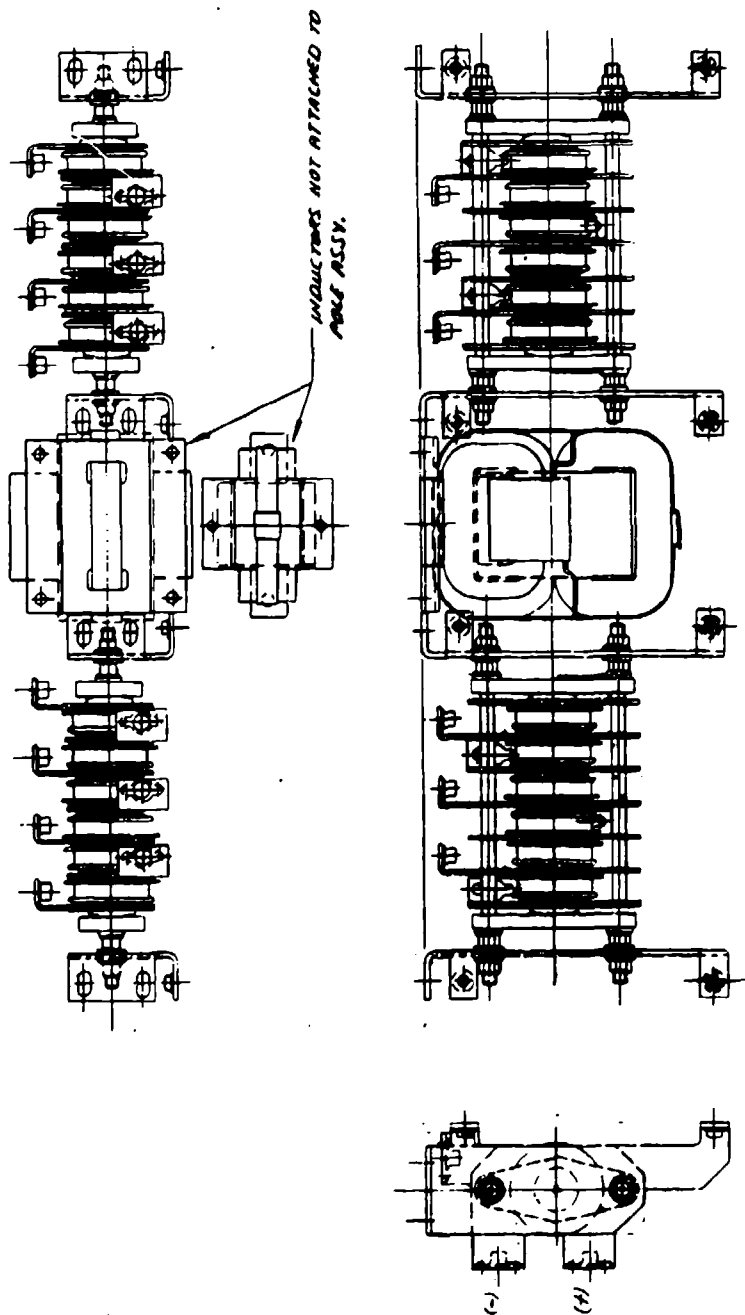
Figure 3.3.1-1

Pre-regulator Assembly Mechanical Configuration

3.3.1 Preregulator Assembly Mechanical Description (Continued)

Input to the preregulator assembly is made via six copper bus bars from the generator input feed-through terminals to the top of the preregulator at tabs on the various bus bar/heat sink plates. The incoming bus bars are fed through current transformers located beneath the feed-through terminals.

The busing away from the preregulator assembly is accomplished by staggering tabs off the side of the bus bar/heat sink plates. Also, a copper bus bar acting as a current shunt is used to detect the current balance in the windings of the interphase transformer. Any error is detected by the DC sharing loop in the control circuits and used to drive the error to zero. Saturation of the interphase transformer is thus prevented, which keeps the size and weight of it, and the SCRs, to a minimum.

There is a total of seven spraying nozzles located above the preregulator assembly. This is required due to the amount of heat the SCRs generate. The maximum oil inlet temperature is 40°C and the maximum temperature rating for the SCRs is 125°C. This allows for a maximum temperature rise of 85°C.

3.3.2 Power Pole Assemblies

Figure 3.3.2-1 shows one of three identical power pole assemblies. Six size 9 hockey puck transistors and two size 7 hockey puck commutation diodes are clamped between copper bus bar/heat sinks. There are also two controlled-current feedback transformers (with single turn primaries) clamped in the stacks. Three spring clamps along with the 1/4 inch draw bolts are used to achieve the desired clamping force. Gimbal spacers are used on the ends of the stacks to ensure uniform distribution of loading on the stacks. Aluminum spacers are added to balance the stack lengths and to increase the thermal capacitance of the assembly.

POWER POLE ASSY

ED404329

INTERPHASE XFMR

VIEW A-A

Figure 3.3.2-1
Power Pole Assembly

3.3.2 Power Pole Assemblies (Continued)

The busing from the preregulator is connected to the DC link laminated bus bar assembly. This can be seen in the inverter unit layout, Figure 3.3-2. This assembly is used to pick up the dc-link filter capacitors and the 800 Hz trap inductor. Feed-through terminals are located directly above the laminated bus bar at the appropriate locations to reduce inductance between the capacitors and the poles. A detail of these feed-through terminals is shown in section A-A of Figure 3.3-2. Terminals are also provided for the link suppressor module connections.

The base drive printed wiring board is located below the power pole and is mounted directly to bus bar/heat sink plates. This printed wiring board contains all the necessary components to drive the CCFTs. Stud-mounting type diodes are mounted along the center of the printed wiring board. The power poles bus bar/heat sink configuration allows for these diode terminals to point upward.

The power pole assemblies are mounted in a fashion similar to the preregulator assembly. Brackets at the ends of the stacks bend out at 90° to allow easy mounting to the 1/2 inch aluminum plate. The holes in these brackets that are used for mounting are slotted to pick up any tolerance in the power pole assembly length.

3.3.3 Output Inductor

The output inductor is shown in Figure 3.3.3-1. It consists of three coils, sheet-wound with copper strip, and interleaved with polyamide film for turn-to-turn insulation. These coils are mounted onto a gapped, double "E" core, laminated stack. Spacers are used to allow for cooling oil to flow through windings and cool more efficiently. It will be impregnated with high solid Amide-Imide to ensure stability and high thermal conductivity. The inductor is designed per MIL-T-27, Grade 6, for 220°C continuous operation at the relatively high current density of 6000 amps/square inch to conserve weight, and is cooled by direct impingement of cooling oil on windings. The output inductor assembly weighs approximately 25 pounds.
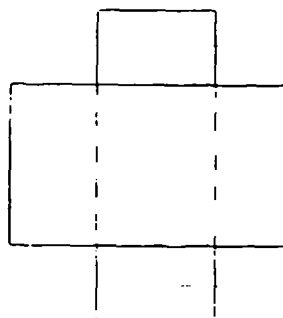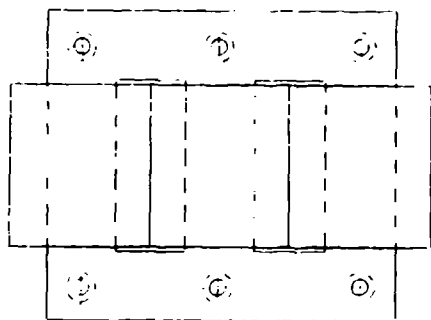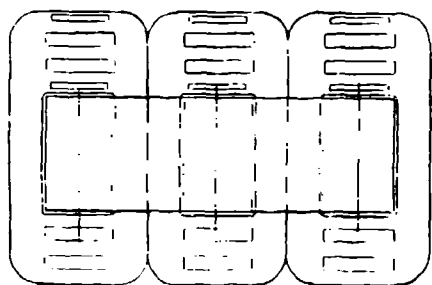
OUTPUT INDUCTOR

DFTM-R Glenn 03/4/6

ED404331

Figure 3.3.3-1
Output Inductor

3.3.3 Output Inductor (Continued)

From the output of the power poles, three bus bars lead over to the output inductor. Directly above the finish leads of the inductor, are located three feed-through terminals. These are used to pick up the ac output filter capacitors. These filter capacitors are arranged such that a single bus bar for each phase picks up a group of five capacitors and then passes through the corresponding current transformer and terminates at the output terminal board. The output terminal board also serves as a feed-through terminal down into the oil cooled area to pick up the neutral forming transformer.

3.3.4 Neutral Forming Transformer

The neutral forming transformer is shown in Figure 3.3.4-1 and has an approximate weight of 24 pounds. The method of assembly chosen is the interconnecting star or zig-zag connection. This method was selected because the performance to weight ratio is the best. The inherently stable neutral derived from this connection permits single-phase line-to-neutral loads with the six winding currents equal to one third the neutral current and equal to each other. It consists of three conventional type coils mounted onto a gapped "double E" core, laminated stack.

3.3.5 Cooling Oil

Cooling oil per MIL-L-7808 to the 400 Hz power conditioning package is cooled, filtered, and pumped by equipment separate from the package. Minimum flow rate required at 40°C inlet temperature is six gallons per minute. Estimated pressure required to provide the flow rate is less than 50 psig. The flow rate may be allowed to drop off at lower oil temperatures while maintaining a constant input pressure of 50 psig. To ensure cooling at low temperatures when very little oil will flow at 50 psig inlet pressure, there must be a reservoir of cooling oil within the sealed enclosure. The depth of the reserve oil is approximately 1.5 inches. During high temperatures when oil is flowing at rapid rates, the reserve will drop due to a large amount of oil adhering to the various plates and heat sinks within the power conditioner sealed enclosure.

PC BOARDS

CONNECTOR

NEUTRAL FORMING XFMR

ED404332
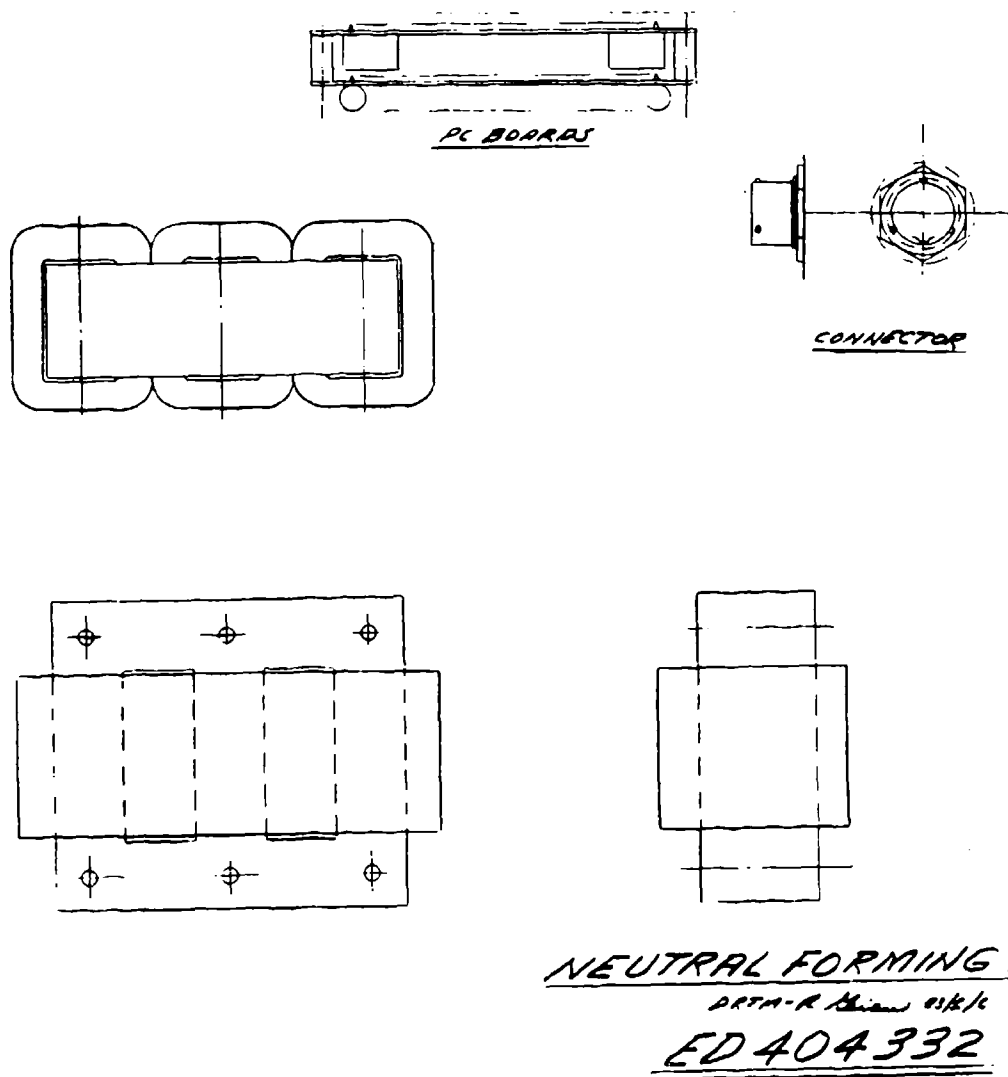
Figure 3.3.4-1
Neutral Forming Transformer

3.3.6   Inverter Control Unit

The inverter control unit, as shown in Figures 3.3.6-1 and 3.3.6-2, is a separate fully enclosed individual assembly of plug-in printed circuits. The unit contains two isolated compartments; the larger is for control of the inverter and the smaller for control of the preregulator.

The inverter control unit is remote from the inverter assembly. It is interconnected to the power conditioner by three connectors; two from the inverter control section and one from the preregulator control section.

The control module has two connectors. One interfaces with the power conditioner, another with system wiring. The power conditioner connector makes the transistor base drive logic interface, thyristor gate drive logic, and makes the circuit interface of all sensing of voltage and current. The system connector provides the interface to the remote current transformer, the contactors, and the generator PMG.

The majority of the inverter control components are packaged into plug-in printed circuit board modules. The printed circuit board modules have been sized to contain full system functions and attain a low number of interconnections between modules.

All printed circuit board modules plug into a mother board that is a printed circuit board also. It contains all wiring between the function.l modules and all wiring from these modules to the three external connectors.

The printed circuit board modules are clamped into place on the base with the aid of wedge locks. The wedge locks are attached to a heat sink plane on the printed circuit boards and conduct heat away from the boards down to the base. Board spacing on the lab unit lends itself to increased maintainability. Maintainability is also enhanced by individual L-shaped covers; one cover for the inverter control compartment, and one for the preregulator control compartment. With either cover removed, any printed circuit board module in the corresponding compartment can be removed from the back of the control module without disturbing any other module.

Figure 3.3.6-1

Inverter Control Unit Outline
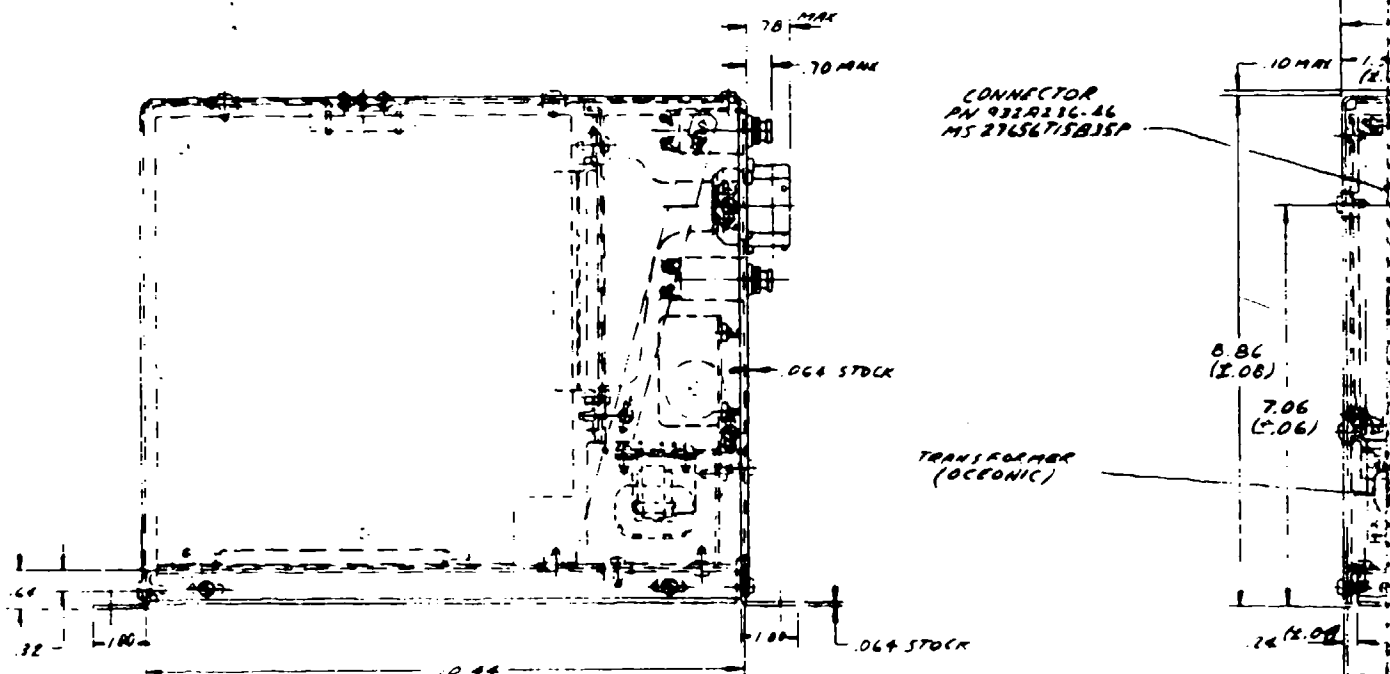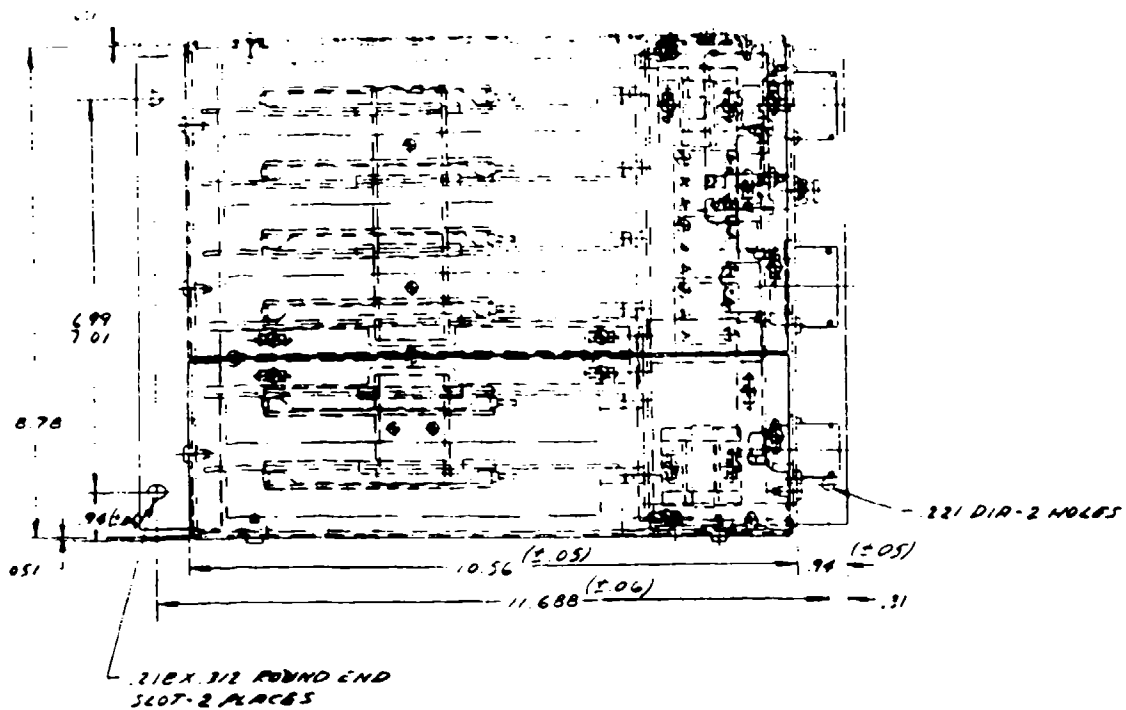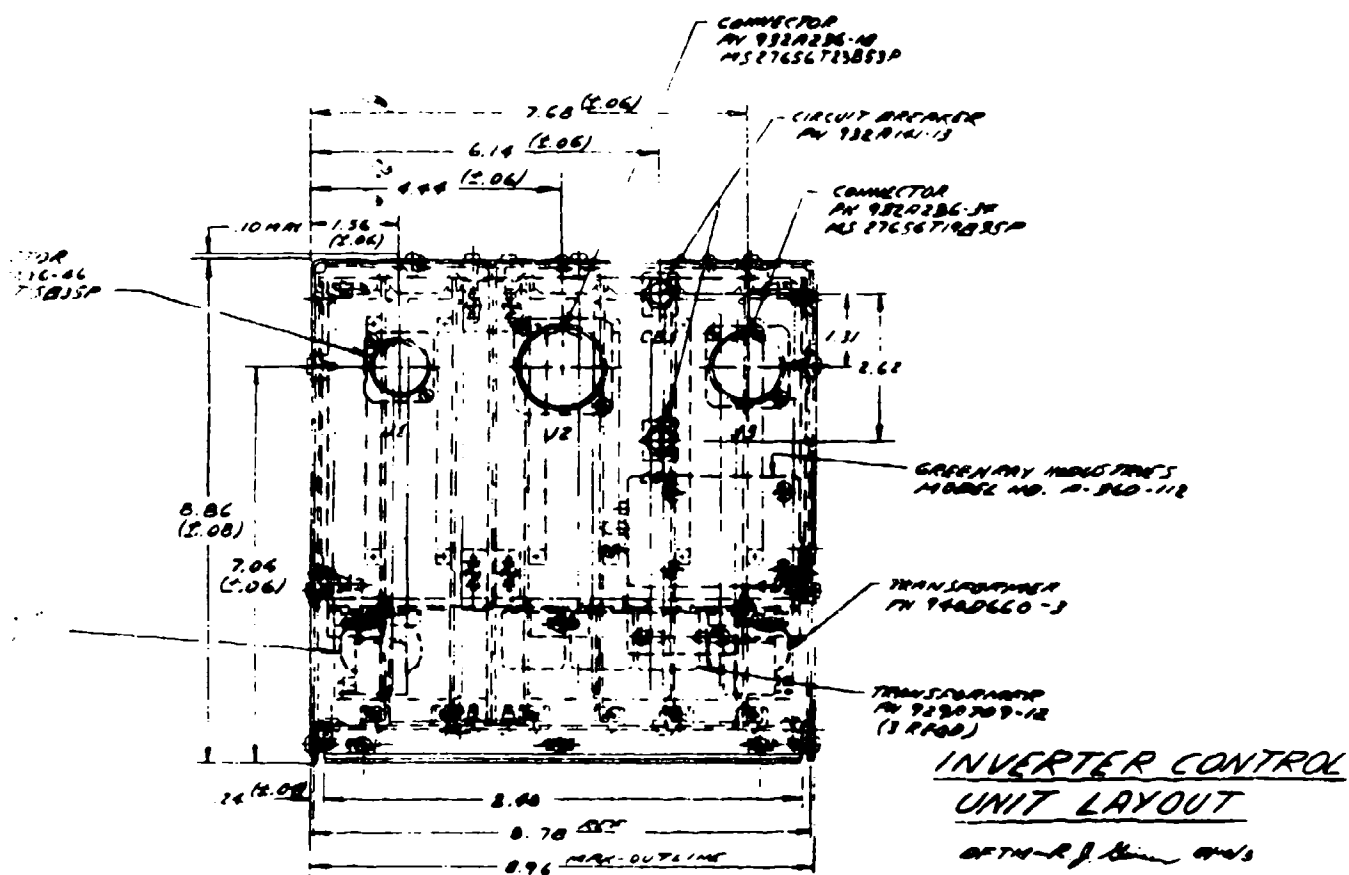
INVERTER CONTROL UNIT LAYOUT

after R.J. Stein dwg.

ED 404344

3-43

Figure 3.3.6-2

3.3.6   Inverter Control Unit   (Continued)

The boards for the control module have up to eight layers of copper. Six
layers are used for circuit, one for a ground plane, and one for the heat
sink. The heat sink layer is on the component side and is used exclusively
for conduction of heat to the wedge locks on the edge of the board. The
thickness of the copper sink varies with the amnount of heat to be carried
away. The layers of circuits are interconnected through plated holes. The
boards conform to MIL-P-55110 using metal-clad laminate per MIL-STD-454,
Requirement 5. The boards are conformal coated for environmental protection
and to enhance the thermal conduction from the components to the board heat
sink planes.

Any major heat-dissipating components are chassis mounted. This is
accomplished by the use of a mounting bracket that connects to the front panel
and base.

The connectors on each printed circuit board conform to MIL-C-55302. The
boards have polarized connectors to prevent incorrect installation. An
environmental gasket is placed in the interface between the connector plug and
the receptacle to prevent pin-to-pin leakage or dielectric failure during high
moisture.

3.3.7   Link Suppressor Module

An outline of the link suppressor module is shown in Figure 3.3.7-1. The
layout of the module is shown in Figure 3.3.7-2. The link suppressor module
is required to suppress transient overvoltages on the link. The suppressor
can be reduced in power handling capability once system "bugs" are worked out
and the regulator optimized. In a production unit, the functions of the link
suppressor could be incorporated into the inverter, but for the sake of a lab
breadboard unit, it is a separate remote unit.

Figure 3.3.7-1

Link Suppressor Module Outline

LINK SUPPRESSOR MODULE
LAYOUT

ED404343

Figure 3.3.7-2

3.3.7   Link Suppressor Module   (Continued)

The unit is connected directly to the link by two leads going to two terminal posts on the aluminum mounting plate. The link suppressor module also has an external round connector for system interface.

The unit contains two size-9 matched power transistors that are clamped together in a fashion similar to the pole assemblies. This includes draw bolts, spring clamps, gimbal spacers, and bus bar/heat sink plates. The unit also contains two 11 inch long power resistors. One is mounted directly above the other with the use of standoffs and mounting brackets. A printed circuit board is mounted vertically on the side of the unit that runs parallel to the two power resistors. There are also two small boards in the front of the unit for mounting various components.

The chassis consists of an 0.064 inch thick aluminum base, and a front panel containing the connector that mounts to the base. The top, sides, and back are all enclosed with a one piece cover. This allows for complete accessibility for any required maintenance.

3.4   Mechanical Design of HVPS

The basic shape of the power supply assembly was determined by the selection of pressurized gas as the major dielectric medium. For pressurized gas the minimum weight container would be a sphere. Since the spherical shape may not allow for the optimum use of interior space, a cylinder with toro-sheroidal heads is used.

The basic container is designed to Section VIII, Unfired Pressure Vessels, of the ASME Boiler Code. A design to this code will result in a container that is safe under all expected conditions of pressure and temperature. At the specified temperatures, aluminum will be used for the vessel. The basic vessel wall will be approximately 0.09 inch thick. Other materials could be used, but past experience has shown that the overall design will weigh less when the tank is made from aluminum.

3.4.1   Mechanical Layout

The final mechanical layout will be done during the next phase. A preliminary layout has been done. This is shown in figure 3.4.1-1. All of the power supply components are mounted to a framework. They are installed or removed from the pressure vessel as a unit. All low voltage connections are made through hermetically sealed, round MS connectors. Different size connectors are used for different functions. For similiar connectors, such as the prime power input connectors, the connectors are keyed to prevent mating with the wrong halves.

Four connectors are used for the prime power; two for each three-phase output for the generator. Two connectors are used because one connector cannot handle the current. The connectors for the different three-phase inputs are keyed differently so that the wrong input cannot be connected.

Inside the tank the leads are connected to a terminal board on the subassembly frame. The leads are disconnected at the terminal board to remove the subassembly.

All internal wiring is done at the subassembly stage before the subassembly is placed in the tank. The wiring and connections are designed to prevent corona. Soldered high voltage connections will use the "solder ball" technique where a ball of solder of specified radius is formed around the connections. Bolted high voltage connections will use ball nuts or acorn nuts to prevent sharp points, which would cause corona.

The placement of parts is determined primarily to keep high voltage wiring to a minimum. All high voltage wiring is by direct short runs. Component spacing is determined by the voltage stresses in the space between components. Enough safety factor is added to prevent corona under worst-case conditions.
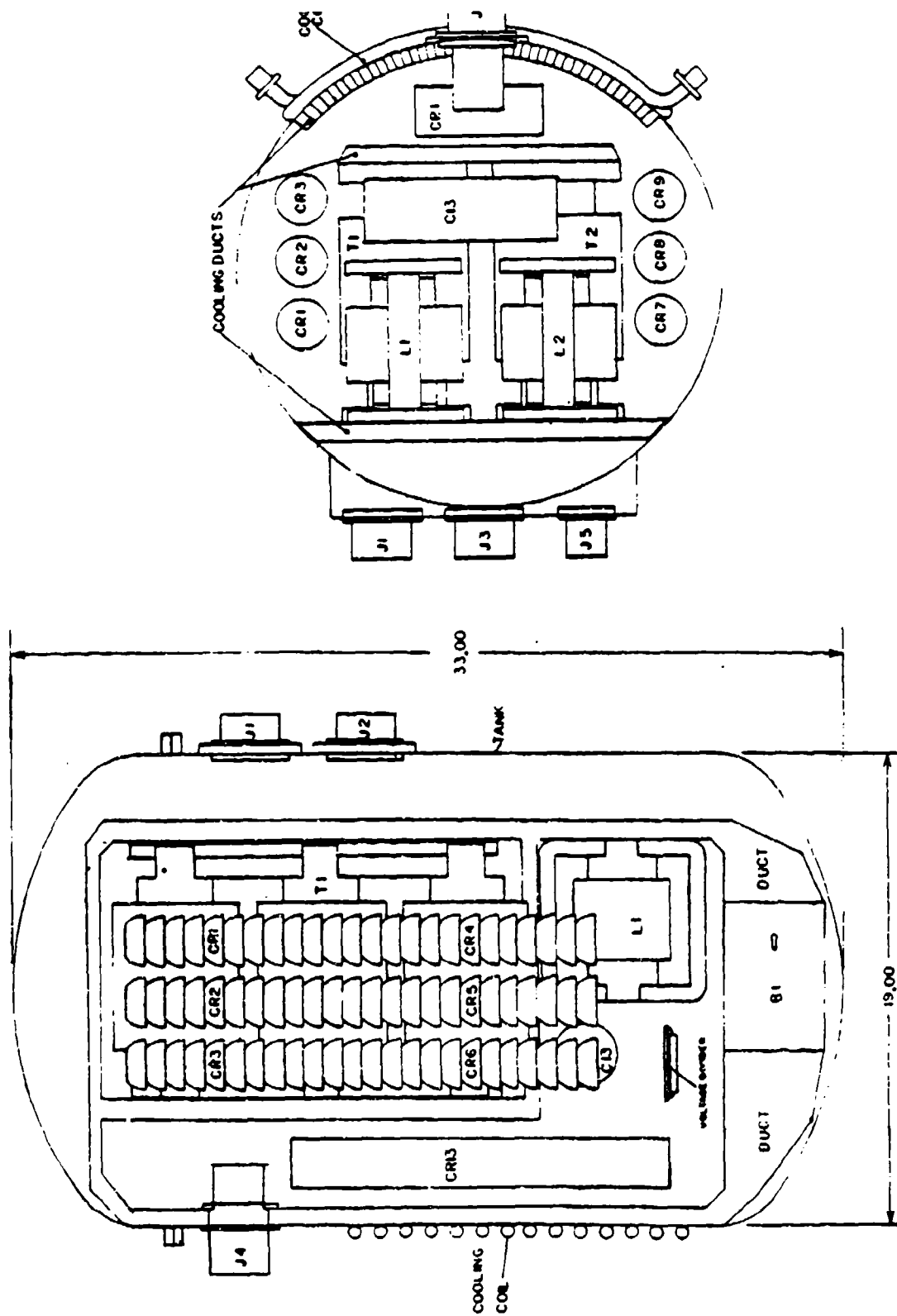
Figure 3.4.1-1

HVPS Mechanical Layout

3.4.2   Transformer Design

The transformer is mounted so that the core is in good thermal and mechanical contact with the metal structure in the subassembly. The subassembly is designed to be able to support the weight of the transformers and directly transfer that weight to the external mounting. Heat is transferred through the frame to the tank wall. The transformer is shown in Figure 2.6.1-2.

The coils are wound on high temperature epoxy glass coil forms. The primary form has an inside diameter that fits around the square leg of the core. The coil form is longer than the window opening of the core. It is notched at each end to permit it to go around the cross piece of the "E". This holds the primary coil forms centered around the core leg.

The secondary coil forms are similar to the primary coil forms except that the inside diameter is larger. The secondary coils are placed over the primary coils.

End plates are used to mount the transformer. The end plates have tapped bosses as shown in Figure 2.6.1-2. The coil forms fit over the bosses. Spacers are placed between the primary and secondary coil forms. A screw into the tapped boss holds the primary and secondary coils in place.

3.4.3   Cooling

The power supply primary cooling means is a cooling jacket external to the tank but thermally part of the tank, which is cooled by either water or oil. The area to be cooled and the required coolant flow will be determined after the final mechanical design is completed.

Heat is transferred through the tank wall into the primary cooling system. This heat is transferred to the tank wall by both conduction and forced convection. Heat from the transformer cores is conducted through the internal structure to the tank in the area of the primary cooling coil. Heat from the coils, diodes, and other parts is transferred to the tank wall by the forced

3.4.3   Cooling   (Continued)

flow of the SF6 past the parts to be cooled. The SF6 is circulated by the
blower B1 through a closed loop. After the SF6 has cooled the components, it
passes through a finned area directly inside the tank wall from the primary
cooling loop.

If the cooling system fails, a thermal switch, which opens on increasing
temperature, shuts down the power supply. An over-pressure relief valve opens
if the internal pressure exceeds a safe level.

The final mechanical details of the power supply layout and cooling will
be done during the next phase.

The electrical design of the power supply and transformer has been
completed. Parts selection is complete for the electrical circuit. The
filter inductor and balancing inductor, both of which are conventional
designs, must be completed during the next phase.

3.5   28 Volt Power Conditioner

The 28 volt power conditioner is contained in a housing measuring 22×10×7
inches (Figure 3.5-1). This includes a set of ten load capacitors, each
approximately 0.03 farads. A number of the components require heat sinks and
these are all mounted to the case. The case is perforated to dissipate heat
since no cooling fan is used. Most of the parts are on one PC board.

Figure 3.5-1

Outline, 28 Volt Power Conditioner

4.0   SUMMARY OF POWER SYSTEM

4.1   <u>System Description</u>

This section provides a summary of the selected power system to meet the
requirements of the specification titled "200 to 300 kVA, Conditioned Power
System Development". Included in this summary is the single line diagram
which depicts the component required for one channel of the four channel
system.

A tabulation is included of the component sizes and weights, as well as the
system losses and resultant efficiencies.

Changes were made in system philosophy as the study progressed. The major
changes are as follows:

1. The generator maximum rated speed was changed from 25,000 rpm to 15,000
   rpm. This change resulted from the analysis conducted relative to
   generator cooling. Reference section 1.2.2.2.3, Thermal Rationale, on
   page 1-57 of this report.

2. Separate feeders were run for each of the major conversion units (HVDC and
   the 400 Hz AC systems). Analysis showed paralleled conductors were
   required from the generator to the conversion equipment due to conductor
   skin effects. There was, therefore, no penalty in using separate feeders
   with the big advantage or reduced interaction between the HVDC and the 400
   Hz systems. The impact of skin effect at the maximum generator operating
   frequency is presented in Tables 1.2.1-3 on page 1-20 of this report.

3. The high voltage power supply uses two three phase full wave rectifier
   bridges in parallel.

4.2   System Components

The system components are depicted on the single line diagram, Figure 4.2-1.
The components consist of:

1.   AC Generator
2.   Generator Control Unit (GCU)
3.   AC Converter (115/200 volts, 400 Hz.)
4.   Inverter Control Unit (ICU)
5.   High Voltage DC Supply (HVDC)
6.   Voltage Reduction Circuit (K) (In the HVDC)
7.   Low Voltage DC Supply (LVDC)
8.   Generator Breaker A (GBA, Breaker from the Generator to the AC Converter)
9.   Generator Breaker B (GBB, Breaker to the LVDC)
10. Generator Breaker C (GBC, Breaker to the HVDC)
11. Load Breaker (LB, Breaker to the 115/200 volt, 400 Hz AC load bus)

The associated current transformers are not shown on this single line diagram.

An auxiliary contact is required on the GBC to provide transfer of the point
of regulation between the high voltage DC output and the input to GBC from the
generator. This transfer is used to provide regulation on the HVDC system
when it is operating (above 83% speed) and to provide generator voltage
control on the input to the 400 Hz converter when the HVDC system is not
connected.

This technique provides good voltage regulation on the HVDC system and allows
transfer to a lower voltage level at the lower speeds such that the generator
would not be operating at saturated conditions at the slow speed.

Preliminary designs were made on items 1 through 7 above. These are described
briefly in the following paragraphs.
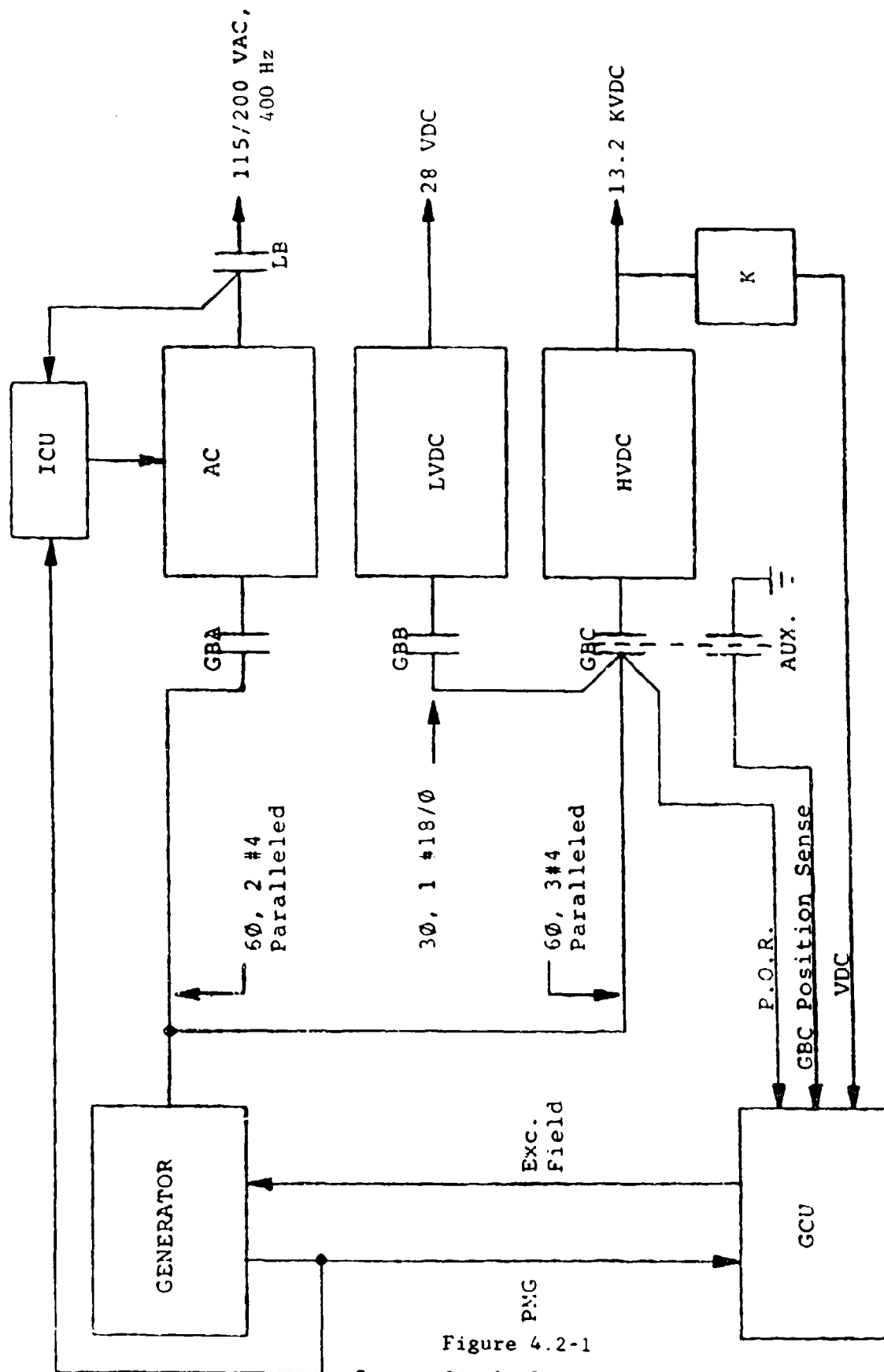
Figure 4.2-1

System Single Line Diagram

4.2.1   Generator

The generator is a special design from two aspects. One is that the generator is a non-standard six phase machine. The output has been wound to provide two sets of three phase outputs, each being separated from the other by 30 electrical degrees. This approach provides for minimum complexity and minimum filtering requirements in rectifier type circuits. All three power conversion systems present rectification type loads to the generator.

The second aspect is the mechanical design of the generator. To provide for proper cooling, the length of the main machine was reduced and the diameter increased.

To keep rotor tip speeds to acceptable levels, the maximum speed was reduced to 15,000 rpm from 25,000 rpm. With the larger rotor diameter, a unique exciter has been designed which makes use of the space available inside the rotor. The exciter and PMG are nestled inside the main machine rotor, keeping the overall generator length short and utilizing space to the maximum extent. See Figure 1.2.2.2-2 on page 1-31 for the scheme employed.

4.2.2   Generator Control Unit

The generator control unit includes the voltage regulator, the system control and the system protection.

The unit senses for generator power ready conditions and provides a power ready output to the inverter control unit (400 Hz). Power is provided to the close coils of the contactors for the HVDC power system and the low voltage (28 VDC) DC system at the power ready condition and 83% speed signal.

The unique feature of transfer of the voltage sense point is accomplished within the GCU by sensing the HVDC contactor position. From 53% speed to 83% speed, the generator output voltage is controlled to about 150 volts L-N. At 83% speed, the HVDC system contactor closes and the voltage sense is transferred to the HVDC output sense to control the HVDC output to 13.2 kilovolts. The resultant generator output voltage is approximately 245 volts L-N for this condition.

4.2.2   Generator Control Unit   (Continued)

The system protection is included in the GCU. This is depicted on the logic diagram, Figure 2.1.2-1 on page 2-3. It should be noted that for generator overvoltage and undervoltage, the sense level is switched in the same manner as the generator voltage control.

4.2.3   AC Converter

The AC converter package contains the power components required to convert generator output power to 400 Hz AC power.

The two sets of 3-phase generator outputs are each rectified through their own 3-phase full wave SCR bridges. The outputs are paralleled through a load sharing inductor and filtered to provide the DC-Link voltage to the inverter bridge. The output of the inverter is filtered to provide the high quality 400 Hz AC power.

A neutral forming transformer is connected across the output to form the neutral for the three-phase, 4-wire system.

The output voltage is fed to the ICU (inverter control unit). This voltage is compared to a reference in the ICU, the error signal is then amplified and fed to the SCR bridges to control the DC-Link voltage such that a constant 115/200 volts is maintained at the point of regulation.

The basic power circuits are shown on Figure 2.4.2.1-1 on page 2-62.

4.2.2   ICU (Inverter Control Unit)

The ICU provides the controls for the 400 hz conversion unit. This includes two basic functions. One is the programmed waveform pattern for switching the transistors in the inverter power poles to develop the 400 Hz output. The second is the 400 Hz system voltage control which is accomplished by sensing the point of regulation voltage and correcting for any errors through the SCR rectifier bridge to control the DC voltage fed to the input to the inverter.

4.2.2   ICU (Inverter Control Unit) (Continued)

The controls involved are shown in the block diagram, Figure 1.2.3-1 on page 1-65.

The 400 Hz system protection and the required control power supplies (for 400 Hz system) are also included in the ICU. Protection provided includes the following:

    Input Undervoltage
    Input Overcurrent
    Output Overvoltage
    Output Undervoltage
    Output DC Content
    Output Extraneous Frequency
    Output Abnormal Frequency

The regulation loop includes current limiting as well as link voltage suppression.

The schematic for these controls is shown on Figure 2.5.1-1 on page 2-81.

4.2.5   High Voltage DC Supply (13.2 KV)

The high voltage DC supply schematic is shown in Figure 2.6-1, page 2-104.

The input is from the six-phase generator. Each set of three-phase voltages from the generator feed transformer rectifiers which have their outputs paralleled through a load sharing inductor. This output is then filtered and fed to the 13.2 KV load.

The system output voltage is sensed and a fixed ratio is fed back to the voltage regulator to provide voltage regulation through generator excitation control. When the HVPS is not powered, voltage regulation (of the generator) is transferred to the generator side of the contactor.

4.2.6   Low Voltage DC Supply (28 VDC)

The low voltage DC supply provides a pulsed 17 KW (per channel) load with an average load of 600 watts.

The schematic for this supply is shown in Figure 2.7.3-1, page 2-115.

The input is one of the 3-phase outputs from the generator. The principle used for operation is that of storing energy in capacitors during the OFF time of the unit and then discharging the capacitors during the pulse load.

In this manner, there are no large power pulses drawn from the generator and the system is not sensitive to input power variations.

The unit develops its own DC power for operation of its control circuits.

4.3   Feeder Configuration

Analysis was conducted on feeder configurations that may be used in this system.

This included use of common feeders as well as dedicated feeders for each of the power conversion systems.

The factor that had the greatest influence on feeder configuration selection was the analysis relative to skin effect at the generator frequencies. Based on the analysis, 2 sets of #4 feeders were selected for the conversion unit for the 400 Hz system and three sets of paralleled feeders for the HVDC conversion unit.

4.4   System Losses

System losses were calculated at the highest continuous load levels at both minimum and maximum generator speeds (83% and 110%).

4-7

4.4.1 Feeder Losses

The calculated feeder losses in watts are as follows:

Feeders To	Speed 83%	110%
HVDC Unit	3480	3750
400 Hertz Unit	4100	4450
Total Watts	7580	8200

The difference in losses at the two frequencies is due to differences in skin effect at these two frequencies (2,500 Hz versus 1886 Hz)

4.4.2 Component Losses

The tabulation below shows the major losses in watts of the system components.

Component	Speed 83%	110%
Generator	42,100	44,500
HVDC	3,900	4,570
400 Hz AC	6,000	6,000
28 VDC	Nil	Nil
Total Watts	52,000	55,070

Calculated efficiency at 83% speed is equal to 88% and at 110% speed is equal to 87.5%.

These calculations are based on preliminary designs. As system component details are finalized, any changes in the loss numbers (and efficiency) can be updated.

4.5　　　　　Component Sizes and Weights

The sizes and weights of the components have been calculated as a part of the preliminary design.

The calculated sizes and weights are presented in Table 4.5-1.

The calculated weight for the feeders selected in this preliminary design is 580 pounds.

The total weight on a per channel basis then is equal to 1487 pounds.

Table 4.5-1
Tabulation of the Required Line Replaceable Units,
with Estimated Unit Weights for Production per Channel

LRU	Estimated Weight	Dimensions In Inches	Outline On Page
Generator	160	13.26D x 16.50 L	1-58
Generator Control Unit	12	9.96 x 10.92 x 5.57	3-26
AC Power Conversion Unit	163	35.2 x 17.94 x 12.06	3-29/ 3-30
Inverter Control Unit	22	10.44 x 8.96 x 8.78	3-43
High Voltage DC Power Unit	400	19.0D x 33.0L	3-50
Low Voltage DC Power Unit	38	7 x 10 x 22	3-53
Load Breaker (400 Hz)	10	7.2 x 5.7 x 6.0	---
Bus Tie Breaker (400 Hz)	10	7.2 x 5.7 x 5.0	---
Generator Breaker (to AC unit) 2 per Channel	2 x 4	8.81 x 6.81 x 8.13	---
Generator Breaker (to HVDC unit) 2 per Channel	2 x 14	8.81 x 6.81 x 8.13	---
Generator Breaker (to LVDC unit)*	6	6.0 x 6.0 x 6.5	---
Current Transformer *21 per Channel	21 x 1.0	3.0 x 3.0 x 2.0	---
Total System Weight	907	---	---

* Weights and dimensions for these components are estimated.

D - Diameter
L - Length

5.0 FUTURE WORK

This section defines the effort for the next phase of the program. Each of the major components of the system are discussed.

5.1 Generator

The generator electrical design has been completed. Detailed layout drawings of the generator are the first step in the next phase of this program. This will be followed by the manufacture of parts, assembly, and test of a complete generator.

After completion of generator verification tests, the generator would be operated in combination with the GCU.

5.2 GCU

At the completion of this contract phase, the GCU design is approximately 50% complete. The electrical design is complete, with schematic and parts list. Future work will include drafting and layout of printed wiring boards, manufacture of parts, assembly, and testing of the completed unit. Test qualifications must be prepared for the individual boards and for the complete GCU.

System tests will determine the suitability of the design assumptions and prove the system concepts.

5.3 Converter/Inverter and ICU

The mechanical design of this unit needs to be completed. From the detailed drawings, the parts will be manufactured, and the unit assembled and tested.

The unit will be operated in combination with the generator-GCU combination.

5.4   High Voltage Power Supply

The electrical design for the high voltage power supply is essentially
complete. Some electrical design, some circuit analysis, and the final
mechanical design remain to be completed.

The specific tasks that remain are:

1. Design of the filter inductor and balancing inductor
2. Final layout of the power supply parts
3. Pressure vessel design
4. Thermal calculations
5. Final review of high voltage clearances
6. Computer analysis to determine the impact of the ungrounded generator
    neutral on power supply operation

The final mechanical design was not part of the phase one tasks. The electric
field calculations cannot be completed until the final mecnanical
configuration is known.

The possible impact of the ungrounded neutral was not recognized until the
completion of the electrical design. These tasks will be done during the
first part of phase II.

5.5   28 Volt Power Conditioner

The possibilities of very high conversion efficiencies has made the switching
circuit an attractive choice for dc converters. At the same time using a high
frequency results in a small package.

Further improvements will depend on four major components: the switch, the
diode, the magnetic device, and the capacitor.

5.5   28 Volt Power Conditioner   (Continued)

Field effect transistors (FETs) are already being used at low power levels.
The FET has high input impedance and fast response making it ideal for high
frequency operation. Higher operating frequencies will make possible the use
of smaller magnetic and filtering components.

The "on" resistance is still too high for large currents. Reduction of this
resistance could make the FET competitive with the bilaterals used in the
preliminary design.

Improvements in the circuitry can also contribute to efficiency by reducing
component count. One approach would be to use positive feedback as discussed
in Section 2.7. Another approach is to use the Cuk technique.* This
technique reduces component count and reduces ripple to zero, thus reducing
losses.

5.6   Paralleling

The analysis conducted determined what control philosophy is required for
proper paralleling of the power supply units.

Paralleling tests, however, will not be conducted in the next phase, a: only
one system will be built.

*Power Conversion International, July/August 1983, pg 28, Slobodan Cuk and
William Polivka. "Analysis of Integrated Magnetics to Eliminate C·rrent
Ripple in Switching Converters"

APPENDIX A

Schematic Diagram for Computer Simulation
of
Parallel Conditioned Power System
(ED995741)
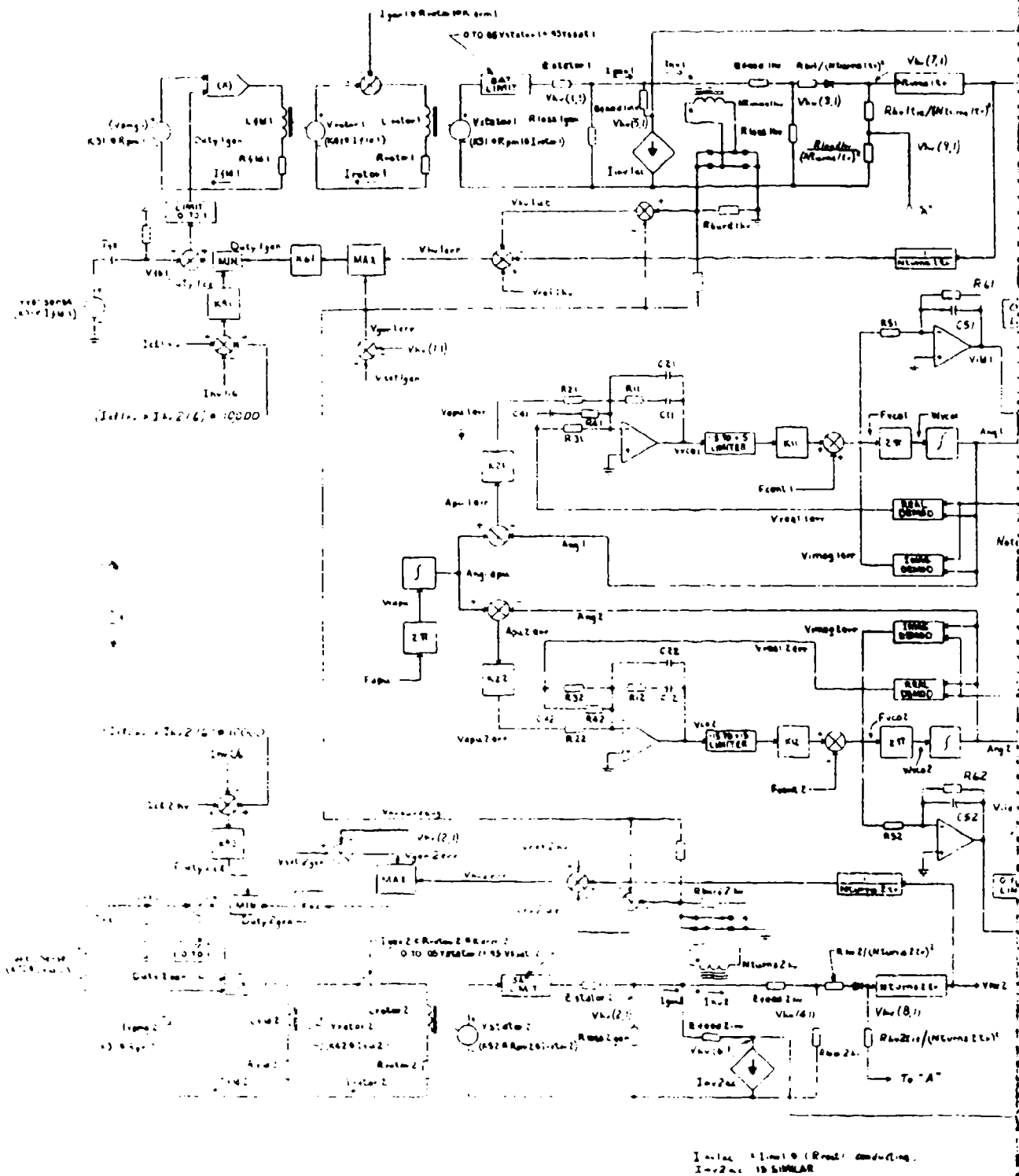
Schematic WPAFB Computer Simulation
ED395741

SCHEMATIC WPAFB
COMPUTER SIMULATION

A-3
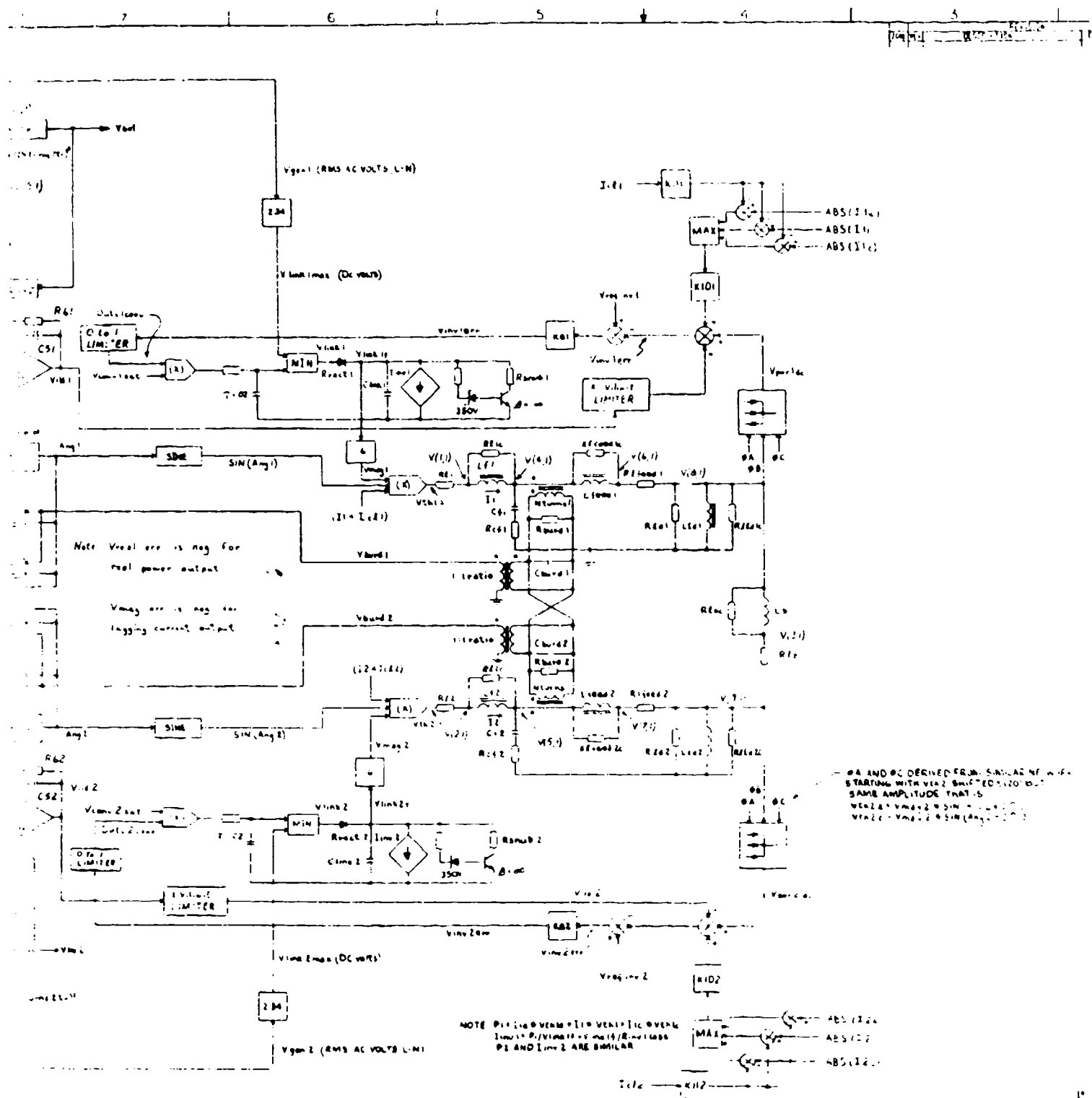
APPENDIX B

Program Listing for Computer Simulation
of
Parallel Conditioned Power System

```
5       Pgm$="WP-PAR"
10      ! This is a modification of 'WPASIM' which has random selected component
15      ! and parameter values within the assigned tolerance levels. See 'WPASIM'
20      ! for original exact values. Tolerance values for each item are shown n
25      ! to each item in this program.
30      !
35      PRINTER IS 16
40      PRINT PAGE
45      OVERLAP
50      !
55      ! REFERENCE: Schematic ED 395741, Reports # WESDL81.13 and # WESDL81.14
60      !
65      ! This program is for the Wright Patterson A/F contract for the
70      ! simulation of large "hybrid" parallel VSCF & VSDC systems.
75      ! It is an extention of the program 'PARSIM' developed for simulating
80      ! parallel VSCF systems covered in the above referenced reports.
85      ! PARSIM effort was funded in whole Westinghouse IR&D projects 41698,
90      ! 42698 and 43698.
95      !
100     ! This simulation includes 2 channels of VSCF 400Hz AC with
105     ! link controlled rectifiers, POR sensing and regulators with real
110     ! and reactive load division. As with real systems only one phase
115     ! is sensed and controlled for real and reactive load division.
120     ! The simulation also includes a simulation of the generator
125     ! with the regulators for the high voltage (13.2 kvdc)
130     ! system. Load division between the HVDC channels is controlled
135     ! through inputs to the generator voltage regulator loops.
140     ! Current limiting on both the HVDC and 400 hz systems is simulated.
145     !
150     ! WRITTEN BY D.E.BAKER 2/83,               REVISION: 0, 3/7/83
155     !                                                    1, 9/6/83
160     !
165     !
170     !
175     !
180     !
185     MASS STORAGE IS ":F8,1"
190     OPTION BASE 1
195     SHORT Plot(8,302)
200 DIM Run$[70],R(9,9),G(9,9),V(9,1),I(9,1),Vhv(9,1),Ihv(9,1),Rhv(9,9),Ghv(9,9)
205 DIM Va(9,1),Ia(9,1),Vc(9,1),Ic(9,1)
210     DIM P1$[30],P2$[30],P3$[30],P4$[30],P5$[30],P6$[30],P7$[30],P8$[30]
215     BEEP
220     INPUT "DO YOU WANT TO KEEP FINAL CONDITIONS ON DISK?",Keep$
225     BEEP
230     LINPUT "ENTER RUN TITLE.",Title$
235     IF (Keep$<>"Y") AND (Keep$<>"y") THEN 250
240     CREATE Title$,5
245     ASSIGN #1 TO Title$
250     BEEP
255     LINPUT "ENTER SHORT SYNOPSIS OF THIS RUN",Run$
260     BEEP
265     LINPUT "ENTER TODAY'S DATE.",Date$
270     BEEP
275     INPUT "ARE STD I/C WANTED (25000 rpm and full load)? Y/N",Ic$
280     GOSUB Newic
285     !
290     ! CIRCUIT PARAMETERS:
295     !
300     Rpm1=24890                      !Generator RPM
305     Rpm2=25100                      !Generator RPM
310     Rpm1hvon=18700                  !Threshold for turn on of HVDC system.
315     Rpm2hvon=18800                  !Threshold for turn on of HVDC system.
320     !
325     IF (Rpm1>Rpm1hvon) AND (Rpm2>Rpm2hvon) THEN Hvon=1
330     !
```

```
335    Dt=6.25E-5                        !Computing time increment,5%
340    K11=-7.795                        !Hz per volt,5%
345    K12=-7.916                        !Hz per volt,5%
350    K21=1.975                         !Volts per radian,5%
355    K22=2.079                         !Volts per radian,5%
360    K31=3.918E-3                      !Volts per rpm (from generator curves),5%
365    K32=3.854E-3                      !Volts per rpm (from generator curves),5%
370    K41=23.02                         !Volts per rpm per amp (from generator curves),5%
375    K42=20.93                         !Volts per rpm per amp (from generator curves),5%
380    K51=4.987E-4                      !Volts per rpm per amp (from generator curves),5%
385    K52=5.220E-4                      !Volts per rpm per amp (from generator curves),5%
390    K61=3.340E-1                      !Volts per volt,5%
395    K62=3.438E-1                      !Volts per volt,5%
400    K71=9.8390                        !Volts per amp,5%
405    K72=9.7950                        !Volts per amp,5%
410    K81=.5180                         !Volts per volt,5%
415    K82=.4950                         !Volts per volt,5%
420    K91=2.455E-2                      !Volts per amp,5%
425    K92=2.651E-2                      !Volts per amp,5%
430    K101=2.01                         !volts per amp,2%
435    K102=2                            !volts per amp,2%
440    K111=.89                          !amps per amp,2%
445    K112=.91                          !amps per amp,2%
450    Karm=.1                      !Armature reaction factor per phase at 18863 RPM,5%
455    Karm1=.01660                 !Armature reaction factor on total gen KVA basis,5%
460    Karm2=.01672                 !Armature reaction factor on total gen KVA basis,5%
465    !
470    C11=3.646E-6!10%
475    C12=3.681E-6!10%
480    C21=5.422E-7!10%
485    C22=5.252E-7!10%
490    C41=6.8E-8
495    C42=7.1E-8
500    C51=9.799E-6!10%
505    C52=1.065E-5!10%
510    Cf1=5.664E-4!10%
515    Cf2=5.733E-4!10%
520    Clink1=6.183E-4!10%
525    Clink2=6.217E-4!10%
530    Cburd1=1.25E-6
535    Cburd2=1.18E-6
540    Cburd=Cburd1+Cburd2
545    !
550    Lf1=1.560E-5! 5%
555    Lf2=1.46E-5 ! 5%
560    Lb=1.573E-6!15%
565    Lfeed1=1.473E-6!15%
570    Lfeed2=1.470E-6!15%
575    Lld1=1       !0%
580    Lld2=1       !0%
585    Lfld1=1.138E-1                    !.025sec*4.05ohms,15%
590    Lfld2=1.037E-1                    !.025sec*4.05ohms,15%
595    Lrotor1=4.771E-2                  !.03sec*1.77ohms,15%
600    Lrotor2=5.962E-2                  !.03sec*1.77ohms,15%
605    !
610    R11=7.425E3!2%
615    R12=7538!2%
620    R21=2950!2%
625    R22=3025!2%
630    R31=44050              !2%
635    R32=43920              !2%
640    R41=1020               !2
645    R42=993                !2%
650    R51=9826!2%
655    R52=9806!2%
660    R61=20294*SQR(2)      !2%
```

```
665   R62=20058*SQR(2)      !2%
670   R11=9.693E-3!10%
675   R12=8.550E-3!10%
680   R1b=2.778E-4          !10%
685   R1feed1=2.979E-4      !10%
690   R1feed2=2.777E-4      !10%
695   R1d1=1/3              !<<<<<<<<<<<<VSCF load resistance on channel 1,0%
700   R1d2=1/3              !<<<<<<<<<<<<VSCF load resistance on channel 2,0%
705   Rloadhv=324           !<<<<<<<<<<<<HVDC load resistance, ohms,0%
710   Rcf1=Dt/Cf1
715   Rcf2=Dt/Cf2
720   R11c=Lf1/Dt
725   R12c=Lf2/Dt
730   R1bc=Lb/Dt
735   R1feed1c=Lfeed1/Dt
740   R1feed2c=Lfeed2/Dt
745   R11d1c=Lld1/Dt
750   R11d2c=Lld2/Dt
755   Rsnub1=.6922                    !VSCF DC Link ov clamp resistor, ohms,10%
760   Rsnub2=.6559                    !VSCF DC Link ov clamp resistor, ohms,10%
765   Rpmg1=.92                       !PMG winding resistance, ohms,10%
770   Rpmg2=1.073                     !PMG winding resistance, ohms,10%
775   Rfld1=3.820           !10%      !Exciter stator resistance, ohms (from gen. data)
780   Rfld2=4.339           !10%      !Exciter stator resistance, ohms (from gen. data)
785   Rrotor1=1.814                   !Rotating field circuit resistance, ohms,10%
790   Rrotor2=1.826                   !Rotating field circuit resistance, ohms,10%
795   Rloss1gen=29.40                 !Gen. losses are on a total KVA basis, ohms,10%
800   Rloss2gen=26.85                 !Gen. losses are on a total KVA basis, ohms,10%
805   Rloss1hv=40.79                  !HVDC TRU losses on total KVA basis, ohms,10%
810   Rloss2hv=36.51                  !HVDC TRU losses on total KVA basis, ohms,10%
815   Rhv1tie=1.05                    !HVDC tie bus resistance, ohms,10%
820   Rhv2tie=.93                     !HVDC tie bus resistance, ohms,10%
825   !
830   Rburd1=199            !1%       !Inverter load division c/t burden, ohms, each ch
835   Rburd2=201            !1%       !Inverter load division c/t burden, ohms, each ch
840   Rburd=1/(1/Rburd1+1/Rburd2)
845   !
850   Rburd1hv=1208                   !HVDC load division c/t burden, ohms, each ch.,1%
855   Rburd2hv=1198                   !HVDC load division c/t burden, ohms, each ch.,1%
860   !
865   Nturns1=3616                    !Inverter load division c/t turns ratio,1%
870   Nturns2=3590                    !Inverter load division c/t turns ratio,1%
875   !
880   Nturns1hv=2970                  !HVDC load division c/t turns ratio,1%
885   Nturns2hv=3024                  !HVDC load division c/t turns ratio,1%
890   !
895   Nturns1tr=12                    !effective HVDC transformer turns ratio, secondary
900   Nturns2tr=12                    !to primary, based on 2 rectifier stacks in series
905                                   ! one per three phase group.
910   !
915   Nturns1tr=Nturns1tr*6*SQR(6)/PI    !Turns ratio modified per TRU topology
920   Nturns2tr=Nturns2tr*6*SQR(6)/PI    !Turns ratio modified per TRU topology
925   !
930   Rhv1s=32.30                     !Series resistance thru HVDC TRU,5%
935   Rhv2s=30.5                      !Series resistance thru HVDC TRU,5%
940   !
945   Zgen1=.1097           !Per phase impedance (Xd) at 18863 RPM, in ohms,5%
950                         ! (based on Shilling's generator regulation curves)
955   Zgen2=.1055           !Per phase impedance (Xd) at 18863 RPM, in ohms,5%
960                         ! (based on Shilling's generator regulation curves)
965   !
970   Zgen1t=Zgen1/6                  !Stator impedance on total gen kva basis
975   Zgen2t=Zgen2/6                  !Stator impedance on total gen kva basis
980   Zstator1=Zgen1t*Rpm1/18863
985   Zstator2=Zgen2t*Rpm2/18863
990   !                          B-4
```

```
995  Lfeed1inv=4.28E-6                !inverter feeder inductance on per phase basis
1000 Lfeed2inv=4.101E-6               !inverter feeder inductance on per phase basis
1005 !
1010 Zfeed1inv=Lfeed1inv*2*PI*Rpm1/10  !impedance per phase
1015 Zfeed2inv=Lfeed2inv*2*PI*Rpm2/10  !impedance per phase
1020 !
1025 Zfeed1inv=Zfeed1inv/6                    !impedance on total kva basis
1030 Zfeed2inv=Zfeed2inv/6                    !impedance on total kva basis
1035 !
1040 Lfeed1hv=2.68E-6                         !HVDC feeder inductance on per phase basis
1045 Lfeed2hv=2.86E-6                         !HVDC feeder inductance on per phase basis
1050 !
1055 Zfeed1hv=Lfeed1hv*2*PI*Rpm1/10  !impedance per phase
1060 Zfeed2hv=Lfeed2hv*2*PI*Rpm2/10  !impedance per phase
1065 !
1070 Zfeed1hv=Zfeed1hv*PI/6                   !impedance per phase due to TRU topology
1075 Zfeed2hv=Zfeed2hv*PI/6                   !impedance per phase due to TRU topology
1080 !
1085 Zfeed1hv=Zfeed1hv/6                      !impedance on total kva basis
1090 Zfeed2hv=Zfeed2hv/6                      !impedance on total kva basis
1095 !
1100 IF Hvon=1 THEN 1120
1105 Zfeed1hv=Zfeed1hv*1E5                    ! Opens HVDC breaker below 83% rpm.
1110 Zfeed2hv=Zfeed2hv*1E5                    ! Opens HVDC breaker below 83% rpm.
1115 !
1120 Fcent1=401.5!2%
1125 Fcent2=397.9!2%
1130 Fapu=400!0%
1135 !
1140 Vlim=5                         !Max control range on VCO input voltage, volts
1145 Vilimit=15                     !Voltage limit (saturation) on imag. load op-amp
1150 !
1155 Vref1gen=143                       !Generator ref voltage when HVDC is off.2%
1160 Vref2gen=140                       !Generator ref voltage when HVDC is off.2%
1165 !
1170 Vmin1gen=217                   ! Generator min. idling voltage when no HVDC load.2%
1175 Vmin2gen=213                   ! Generator min. idling voltage when no HVDC load.2%
1180 !
1185 Vset1gen=Vref1gen*(Hvon=0)+Vmin1gen*(Hvon=1)
1190 Vset2gen=Vref2gen*(Hvon=0)+Vmin2gen*(Hvon=1)
1195 !
1200 Vset1hv=12990/Nturns1tr    !HVDC reference reflected to primary (ac) side,2%
1205 Vset2hv=13420/Nturns2tr    !HVDC reference reflected to primary (ac) side,2%
1210 !
1215 Vref1hv=Vset1hv*Hvon
1220 Vref2hv=Vset2hv*Hvon
1225 !
1230 Vrefinv1=114.1*SQR(2)          !Inverter reference (peak value needed),2%
1235 Vrefinv2=116*SQR(2)            !Inverter reference (peak value needed),2%
1240 !
1245 Vconv1sat=324                  !Max dc link volts available via Duty1avg.2%
1250 Vconv2sat=320                  !Max dc link volts available via Duty2avg.2%
1255 !
1260 Icl1=1257                      !Inverter current limit threshold, amps peak per
1265 Icl2=1146                      !inverter pole,5%
1270 !
1275 Icl1hv=260.5                   !HVDC input current limit threshold, rms amps
1280 Icl2hv=248.1                   !per generator phase,5%
1285 !
1290 !
1295 !
1300 GOSUB Load_mtx
1305 Ppass=3
1310 !
1315 !
1320 Go: PRINTER IS 16
```

B-5

```
1325 PRINT "BUSY"
1330 GOSUB Plist_1
1335 PRINTER IS 16
1340 !
1345 ! TIME SEQUENCE LOOP STARTS HERE:    ****************************+***********
1350 !
1355 FOR Nt=1 TO 1200
1360 !
1365 Time=Dt*Nt
1370 !
1375 ! THE FOLLOWING CALCULATIONS ARE FOR PLOTTING PURPOSES ONLY:
1380 !
1385 Ang_err=Ang1-Ang2
1390 Ang_err=Ang_err+2*PI*((Ang_err<-PI)-(Ang_err>PI))
1395 !
1400 Ppass=Ppass+1
1405 IF Ppass<>4 THEN 1515
1410 Np=Nt/4+1
1415 Plot(1,Np)=V(6,1)/1000
1420 P1$="V(6,1)/1000"
1425 Plot(2,Np)=Ich1/5000
1430 P2$="Ich1/5000"
1435 Plot(3,Np)=Vlink1f/500
1440 P3$="Vlink1f/500"
1445 Plot(4,Np)=Ang_err*10
1450 P4$="Ang_err*10 (.1 radian f/s)"
1455 Plot(5,Np)=(Vstator1-Vstator2)/100
1460 P5$="(Vstator1-Vstator2)/100"
1465 Plot(6,Np)=(Ihv1dc-Ihv2dc)/20
1470 P6$="(Ihv1dc-Ihv2dc)/20"
1475 Plot(7,Np)=Vhv1/25000
1480 P7$="Vhv1/25000"
1485 Plot(8,Np)=Ifld1/10
1490 P8$="Ifld1/10"
1495 Ppass=0
1500 !
1505 ! GENERATOR AND REGULATOR EQUATIONS FOLLOW:
1510 !
1515 Vgen1err=Vset1gen-Vhv(1,1)
1520 Vgen2err=Vset2gen-Vhv(2,1)
1525 Vhv1err=Vref1hv-Vhv1/Nturns1tr-Vhv1ub
1530 Vhv2err=Vref2hv-Vhv2/Nturns2tr-Vhv2ub
1535 Vgen1errm=MAX(Vhv1err,Vgen1err)
1540 Vgen2errm=MAX(Vhv2err,Vgen2err)
1545 IF Hvon=0 THEN 1565
1550 Duty1gen=Vgen1errm*K61
1555 Duty2gen=Vgen2errm*K62
1560 GOTO 1575
1565 Duty1gen=Vgen1err
1570 Duty2gen=Vgen2err
1575 Duty1cl=(Icl1hv-Ihv1ac+(Icl1hv>Ihv1ac)*10000)*K91
1580 Duty2cl=(Icl2hv-Ihv2ac+(Icl2hv>Ihv2ac)*10000)*K92
1585 Duty1gen=MIN(Duty1gen,Duty1cl)
1590 Duty2gen=MIN(Duty2gen,Duty2cl)
1595 Duty1gen=Duty1gen-Vfb1
1600 Duty2gen=Duty2gen-Vfb2
1605 Duty1gen=MIN(1,Duty1gen)
1610 Duty2gen=MIN(1,Duty2gen)
1615 Duty1gen=MAX(0,Duty1gen)
1620 Duty2gen=MAX(0,Duty2gen)
1625 !
1630 !
1635 Ifld1dot=(K31*Rpm1*Duty1gen-Ifld1*(Rfld1+Rpmg1))/Lfld1
1640 Ifld2dot=(K32*Rpm2*Duty2gen-Ifld2*(Rfld2+Rpmg2))/Lfld2
1645 Irotor1dot=(Vrotor1-Irotor1*Rrotor1)/Lrotor1
1650 Irotor2dot=(Vrotor2-Irotor2*Rrotor2)/Lrotor2
```

B-6

```
1655 !
1660 Ifld1=Ifld1+Ifld1dot*Dt
1665 Ifld2=Ifld2+Ifld2dot*Dt
1670 Irotor1=Irotor1+Irotor1dot*Dt
1675 Irotor2=Irotor2+Irotor2dot*Dt
1680 !
1685 Vfb1sense=Ifld1*K71
1690 Vfb2sense=Ifld2*K72
1695 Vcfb1dot=Vfb1/(Lrotor1/Rrotor1)
1700 Vcfb2dot=Vfb2/(Lrotor2/Rrotor2)
1705 Vcfb1=Vcfb1+Vcfb1dot*Dt
1710 Vcfb2=Vcfb2+Vcfb2dot*Dt
1715 Vfb1=Vfb1sense-Vcfb1
1720 Vfb2=Vfb2sense-Vcfb2
1725 !
1730 Vrotor1=K41*Ifld1-Karm1*Igen1*Rrotor1
1735 Vrotor2=K42*Ifld2-Karm2*Igen2*Rrotor2
1740 Vrotor1=MAX(Vrotor1,0)
1745 Vrotor2=MAX(Vrotor2,0)
1750 !
1755 Vstator1=K51*Irotor1*Rpm1
1760 Vstator2=K52*Irotor2*Rpm2
1765 Vstator1=MAX(Vstator1,0)
1770 Vstator2=MAX(Vstator2,0)
1775 Vssat1=300*Rpm1/18863
1780 Vssat2=300*Rpm2/18863
1785 Vstator1=MIN(Vstator1,.05*Vstator1+.95*Vssat1)
1790 Vstator2=MIN(Vstator2,.05*Vstator2+.95*Vssat2)
1795 !
1800 ! THE POR VOLTAGE EQUATIONS FOLLOW:
1805 !
1810 Vpor1dc=(ABS(Va(8,1))+ABS(V(8,1))+ABS(Vc(8,1)))/2
1815 Vpor2dc=(ABS(Va(9,1))+ABS(V(9,1))+ABS(Vc(9,1)))/2
1820 !
1825 ! THE INVERTER V/R EQUATIONS FOLLOW:
1830 !
1835   Q1=(ABS(I1)<Icl1)              !"Q" variables are for pole current limiting
1840   Q1a=(ABS(I1a)<Icl1)
1845   Q1c=(ABS(I1c)<Icl1)
1850   Q2=(ABS(I2)<Icl2)
1855   Q2a=(ABS(I2a)<Icl2)
1860   Q2c=(ABS(I2c)<Icl2)
1865   !
1870   Verr1cl=K101*(MAX(ABS(I1),ABS(I1a),ABS(I1c))-K111*Icl1)
1875   Verr2cl=K102*(MAX(ABS(I2),ABS(I2a),ABS(I2c))-K112*Icl2)
1880   Verr1cl=MAX(Verr1cl,0)
1885   Verr2cl=MAX(Verr2cl,0)
1890 !
1895 Vinv1err=Vrefinv1-Vpor1dc-Vild1-Verr1cl
1900 Vinv2err=Vrefinv2-Vpor2dc-Vild2-Verr2cl
1905 !
1910 Duty1conv=K81*Vinv1err
1915 Duty2conv=K82*Vinv2err
1920 !
1925 Duty1conv=MAX(0,Duty1conv)
1930 Duty2conv=MAX(0,Duty2conv)
1935 Duty1conv=MIN(1,Duty1conv)
1940 Duty2conv=MIN(1,Duty2conv)
1945 !
1950 Duty1dot=(Duty1conv-Duty1avg)/.02
1955 Duty2dot=(Duty2conv-Duty2avg)/.02
1960 Duty1avg=Duty1avg+Duty1dot*Dt
1965 Duty2avg=Duty2avg+Duty2dot*Dt
1970 !
1975 ! CH1, CH2 AND APU ANGLE EQUATIONS FOLLOW:
1980 !                                              B-7
```

```
1985 Fvco1=Fcent1+K11*Vvco1
1990 Fvco2=Fcent2+K12*Vvco2
1995 Wvco1=2*PI*Fvco1
2000 Wvco2=2*PI*Fvco2
2005 Ang1=Ang1+Dt*Wvco1
2010 Ang2=Ang2+Dt*Wvco2
2015 Ang_apu=Ang_apu+Fapu*2*PI*Dt
2020 !
2025 ! SINCE PERIODIC WAVEFORMS REPEAT OVER MULTIPLES OF 2PI WE WILL
2030 ! LIMIT Ang1 AND Ang2 TO A RANGE OF 0 TO 2PI:
2035 !
2040 Ang1=Ang1+2*PI*((Ang1<0)-(Ang1>2*PI))
2045 Ang2=Ang2+2*PI*((Ang2<0)-(Ang2>2*PI))
2050 !
2055 ! BEFORE RESETTING Ang_apu WE SET UP A FLAG TO TELL THAT THIS ANGLE
2060 ! IS GOING TO BE RESET. THIS IS LATER USED IN THE APU-TO-CHANNEL
2065 ! PHASE ERROR DETECTOR FOR A 1 CYCLE (.0025 SEC) HOLD TO MORE ACCURATELY
2070 ! SIMULATE THE NON LINEAR NATURE OF THIS PARTICULAR PHASE DETECTOR.
2075 !
2080 Flag1=(Ang_apu<0)-(Ang_apu>2*PI)
2085 Ang_apu=Ang_apu+2*PI*Flag1
2090 !
2095 ! THE INVERTER THEVENIN VOLTAGES AS A FUNCTION OF TIME:
2100 !
2105 Vmag1=Vlink1f*.6
2110 Vmag2=Vlink2f*.6
2115 IF Vmag1<0 THEN Vmag1=0
2120 IF Vmag2<0 THEN Vmag2=0
2125 !
2130 Vth1=Vmag1*SIN(Ang1)*Q1
2135 Vth1a=Vmag1*SIN(Ang1+2*PI/3)*Q1a
2140 Vth1c=Vmag1*SIN(Ang1-2*PI/3)*Q1c
2145 Vth1_s=Vmag1*SIN(Ang1+PI/2) !THIS ONE IS FOR REACTIVE POWER METER
2150 Vth2=Vmag2*SIN(Ang2)*Q2
2155 Vth2a=Vmag2*SIN(Ang2+2*PI/3)*Q2a
2160 Vth2c=Vmag2*SIN(Ang2-2*PI/3)*Q2c
2165 Vth2_s=Vmag2*SIN(Ang2+PI/2) ! THIS ONE IS FOR REACTIVE POWER METER
2170 !
2175 ! MATRIX EQUATIONS FOR THE OUTPUT FILTER AND PARALLEL LOAD BUS NETWORK:
2180 !
2185 ! FIRST LOAD THE I MATRIX:
2190 !
2195 I(1,1)=Vth1/R11-I1
2200 Ia(1,1)=Vth1a/R11-I1a
2205 Ic(1,1)=Vth1c/R11-I1c
2210 I(2,1)=Vth2/R12-I2
2215 Ia(2,1)=Vth2a/R12-I2a
2220 Ic(2,1)=Vth2c/R12-I2c
2225 I(3,1)=I3
2230 Ia(3,1)=I3a
2235 Ic(3,1)=I3c
2240 I(4,1)=I1+I5-I8
2245 Ia(4,1)=I1a+I5a-I8a
2250 Ic(4,1)=I1c+I5c-I8c
2255 I(5,1)=I2+I7-I9
2260 Ia(5,1)=I2a+I7a-I9a
2265 Ic(5,1)=I2c+I7c-I9c
2270 I(6,1)=I8
2275 Ia(6,1)=I8a
2280 Ic(6,1)=I8c
2285 I(7,1)=I9
2290 Ia(7,1)=I9a
2295 Ic(7,1)=I9c
2300 I(8,1)=-I4-I3
2305 Ia(8,1)=-I4a-I3a
2310 Ic(8,1)=-I4c-I3c
```

B-8

```
2315 I(9,1)=-I6
2320 Ia(9,1)=-I6a
2325 Ic(9,1)=-I6c
2330 !
2335 ! NODE VOLTAGES:
2340 !
2345 MAT V=R*I
2350 MAT Va=R*Ia
2355 MAT Vc=R*Ic
2360 !
2365 ! CURRENT SOURCE DOTS (di/dt's):
2370 !
2375 I1dot=(V(1,1)-V(4,1))/Lf1
2380 I1adot=(Va(1,1)-Va(4,1))/Lf1
2385 I1cdot=(Vc(1,1)-Vc(4,1))/Lf1
2390 I2dot=(V(2,1)-V(5,1))/Lf2
2395 I2adot=(Va(2,1)-Va(5,1))/Lf2
2400 I2cdot=(Vc(2,1)-Vc(5,1))/Lf2
2405 I3dot=(V(8,1)-V(3,1))/Lb
2410 I3adot=(Va(8,1)-Va(3,1))/Lb
2415 I3cdot=(Vc(8,1)-Vc(3,1))/Lb
2420 I4dot=V(8,1)/L1d1
2425 I4adot=Va(8,1)/L1d1
2430 I4cdot=Vc(8,1)/L1d1
2435 I6dot=V(9,1)/L1d2
2440 I6adot=Va(9,1)/L1d2
2445 I6cdot=Vc(9,1)/L1d2
2450 Vcf1dot=(V(4,1)/Rcf1-I5)/Cf1
2455 Vacf1dot=(Va(4,1)/Rcf1-I5a)/Cf1
2460 Vccf1dot=(Vc(4,1)/Rcf1-I5c)/Cf1
2465 Vcf2dot=(V(5,1)/Rcf2-I7)/Cf2
2470 Vacf2dot=(Va(5,1)/Rcf2-I7a)/Cf2
2475 Vccf2dot=(Vc(5,1)/Rcf2-I7c)/Cf2
2480 I5dot=Vcf1dot/Rcf1
2485 I5adot=Vacf1dot/Rcf1
2490 I5cdot=Vccf1dot/Rcf1
2495 I7dot=Vcf2dot/Rcf2
2500 I7adot=Vacf2dot/Rcf2
2505 I7cdot=Vccf2dot/Rcf2
2510 I8dot=(V(4,1)-V(6,1))/Lfeed1
2515 I8adot=(Va(4,1)-Va(6,1))/Lfeed1
2520 I8cdot=(Vc(4,1)-Vc(6,1))/Lfeed1
2525 I9dot=(V(5,1)-V(7,1))/Lfeed2
2530 I9adot=(Va(5,1)-Va(7,1))/Lfeed2
2535 I9cdot=(Vc(5,1)-Vc(7,1))/Lfeed2
2540 !
2545 ! CURRENT SOURCES:
2550 !
2555 I1=I1+I1dot*Dt
2560 I1a=I1a+I1adot*Dt
2565 I1c=I1c+I1cdot*Dt
2570 I2=I2+I2dot*Dt
2575 I2a=I2a+I2adot*Dt
2580 I2c=I2c+I2cdot*Dt
2585 I3=I3+I3dot*Dt
2590 I3a=I3a+I3adot*Dt
2595 I3c=I3c+I3cdot*Dt
2600 I4=I4+I4dot*Dt
2605 I4a=I4a+I4adot*Dt
2610 I4c=I4c+I4cdot*Dt
2615 I5=I5+I5dot*Dt
2620 I5a=I5a+I5adot*Dt
2625 I5c=I5c+I5cdot*Dt
2630 I6=I6+I6dot*Dt
2635 I6a=I6a+I6adot*Dt
2640 I6c=I6c+I6cdot*Dt
```

```
2645 I7=I7+I7dot*Dt
2650 I7a=I7a+I7adot*Dt
2655 I7c=I7c+I7cdot*Dt
2660 I8=I8+I8dot*Dt
2665 I8a=I8a+I8adot*Dt
2670 I8c=I8c+I8cdot*Dt
2675 I9=I9+I9dot*Dt
2680 I9a=I9a+I9adot*Dt
2685 I9c=I9c+I9cdot*Dt
2690 !
2695 !    THE INVERTER LINK CURRENT EQUATIONS FOLLOW:
2700 !
2705 Rinv1loss=(Vlink1f>350)*Rsnub1+(Vlink1f<=350)*50
2710 Rinv2loss=(Vlink2f>350)*Rsnub2+(Vlink2f<=350)*50
2715 P1=I1a*Vth1a+I1*Vth1+I1c*Vth1c
2720 P2=I2a*Vth2a+I2*Vth2+I2c*Vth2c
2725 !
2730 IF Vlink1f=0 THEN Vlink1f=1E-6
2735 IF Vlink2f=0 THEN Vlink2f=1E-6
2740 !
2745 Iinv1=P1/Vlink1f+Vlink1f/Rinv1loss
2750 Iinv2=P2/Vlink2f+Vlink2f/Rinv2loss
2755 !
2760 ! EQUATIONS FOR THE LINK RECTIFIER AND FILTER FOLLOW:
2765 !
2770 Vlink1max=Vgen1*2.34
2775 Vlink2max=Vgen2*2.34
2780 !
2785 Vlink1=MIN(Duty1avg*Vconv1sat,Vlink1max)
2790 Vclink1dot=-Iinv1/Clink1
2795 IF (Vlink1f>Vlink1) AND (-Vclink1dot*Dt<Vlink1f-Vlink1) THEN 2820
2800 Rrect1=.005
2805 Vlink1f=Vlink1-Rrect1*Iinv1
2810 Vclink1=Vlink1f
2815 GOTO 2840
2820 Rrect1=10000
2825 Vclink1=Vclink1+Vclink1dot*Dt
2830 Vlink1f=Vclink1
2835 !
2840 Vlink2=MIN(Duty2avg*Vconv2sat,Vlink2max)
2845 Vclink2dot=-Iinv2/Clink2
2850 IF (Vlink2f>Vlink2) AND (-Vclink2dot*Dt<Vlink2f-Vlink2) THEN 2875
2855 Rrect2=.005
2860 Vlink2f=Vlink2-Rrect2*Iinv2
2865 Vclink2=Vlink2f
2870 GOTO 2905
2875 Rrect2=10000
2880 Vclink2=Vclink2+Vclink2dot*Dt
2885 Vlink2f=Vclink2
2890 !
2895 ! MATRIX ANALYSIS FOR GENERATOR BUS AND HVDC PARALLEL BUS FOLLOWS:
2900 !
2905 Rhv1=Rhv1s*(1+(Vhv(7,1)>Vhv(3,1))*10000)
2910 Rhv2=Rhv2s*(1+(Vhv(8,1)>Vhv(4,1))*10000)
2915 IF (Rhv1<>Rhv1check) OR (Rhv2<>Rhv2check) THEN GOSUB Load_mtx2
2920 !
2925 Iinv1ac=Iinv1*(Rrect1=.005)
2930 Iinv2ac=Iinv2*(Rrect2=.005)
2935 !
2940 Ihv(1,1)=Vstator1/Zstator1
2945 Ihv(2,1)=Vstator2/Zstator2
2950 Ihv(3,1)=Ihv(4,1)=0
2955 Ihv(5,1)=-Iinv1ac
2960 Ihv(6,1)=-Iinv2ac
2965 Ihv(7,1)=Ihv(8,1)=Ihv(9,1)=0
2970 !
```

B-10

```
2975 MAT Vhv=Rhv*Ihv
2980 Vgen1=Vhv(5,1)
2985 Vgen2=Vhv(6,1)
2990 Vhv1=Nturns1tr*Vhv(7,1)
2995 Vhv2=Nturns2tr*Vhv(8,1)
3000 Ihv1=(Vhv(1,1)-Vhv(3,1))/Zfeed1hv
3005 Ihv2=(Vhv(2,1)-Vhv(4,1))/Zfeed2hv
3010 !
3015 Igen1=Ihv1-Ihv(5,1)
3020 Igen2=Ihv2-Ihv(6,1)
3025 !
3030 Ihv1ac=Ihv1/6
3035 Ihv2ac=Ihv2/6
3040 Ihv1dc=Ihv1/Nturns1tr
3045 Ihv2dc=Ihv2/Nturns2tr
3050 !
3055 Vhv1burd=Ihv1ac*Rburd1hv/Nturns1hv
3060 Vhv2burd=Ihv2ac*Rburd2hv/Nturns2hv
3065 Vhvburdavg=(Vhv1burd+Vhv2burd)/2
3070 Vhv1ub=Vhv1burd-Vhvburdavg
3075 Vhv2ub=Vhv2burd-Vhvburdavg
3080 !
3085 ! SOLVE FOR THE INVERTER CURRENTS AND C/T BURDEN VOLTAGE:
3090 !
3095 Ich1=(V(6,1)-V(8,1))/R1feed1
3100 Ich2=(V(7,1)-V(9,1))/R1feed2
3105 Vcburddot=(Ich1/Nturns1-Ich2/Nturns2-Vcburd/Rburd)/Cburd
3110 Vcburd=Vcburd+Vcburddot*Dt
3115 Vburd1=Vcburd
3120 Vburd2=-Vcburd
3125 !
3130 ! DEMODULATED REAL LOAD DIV ERROR SIGNAL FOR INVERTER CH1&2 :
3135 !
3140 ! NOTE: IF THESE DEMODULATORS SEEM THE WRONG SIGN IT IS TO COMPENSATE
3145 ! FOR THE SIGN CHANGE THROUGH THE PLL INTEGRATORS.
3150 !
3155 Vreal1err=Vburd1*(2*(Ang1>PI)-1)
3160 Vreal2err=Vburd2*(2*(Ang2>PI)-1)
3165 !
3170 ! DEMODULATED IMAGINARY LOAD DIV ERROR SIGNAL FOR INVERTER CH1&2:
3175 !
3180 Vimag1err=Vburd1*(2*(Ang1<PI/2)+2*(Ang1>3*PI/2)-1)
3185 Vimag2err=Vburd2*(2*(Ang2<PI/2)+2*(Ang2>3*PI/2)-1)
3190 !
3195 ! PHASE ERRORS BETWEEN THE APU AND INVERTER CH1&2:
3200 !
3205 Apu1err=Ang_apu-Ang1
3210 Apu2err=Ang_apu-Ang2
3215 !
3220 ! THE INVERTER PHASE DETECTORS CANNOT REOLVE BEYOND ±PI, SO RESET ANGLES:
3225 !
3230 Apu1err=Apu1err+2*PI*((Apu1err<-PI)-(Apu1err>PI))
3235 Apu2err=Apu2err+2*PI*((Apu2err<-PI)-(Apu2err>PI))
3240 !
3245 ! WE WANT TO UPDATE THESE ERRORS ONLY ONCE EACH CYCLE (.0025SEC) SO
3250 ! WE USE THE Flag1 VARIABLE.
3255 !
3260 IF Flag1=0 THEN 3295
3265 Vapu1err=K21*Apu1err
3270 Vapu2err=K22*Apu2err
3275 !
3280 ! THE REACTIVE LOAD DIV ERROR SIGNALS ARE ADDED INTO THE VOLTAGE REGULATOR
3285 ! LOOP AS A "TRIM" TO NORMAL REGULATOR.
3290 !
3295    Vc51dot=(Vimag1err/R51-Vc51/R61)/C51
3300    Vc52dot=(Vimag2err/R52-Vc52/R62)/C52
```

B-11

```
3305    Vc51=Vc51+Vc51dot*Dt
3310    Vc52=Vc52+Vc52dot*Dt
3315 !
3320    Vc51=MIN(Vc51,Vilimit)
3325    Vc51=MAX(Vc51,-Vilimit)
3330    Vc52=MIN(Vc52,Vilimit)
3335    Vc52=MAX(Vc52,-Vilimit)
3340 !
3345    Vild1=-Vc51
3350    Vild2=-Vc52
3355 !
3360 Ic41=(Vreallerr-Vc41)/R41
3365 Vc41dot=Ic41/C41
3370 Vc41=Vc41+Vc41dot*Dt
3375 ! EQUATIONS FOR OUTPUTS OF THE PLL INTEGRATORS FOLLOW:
3380 ! CHANNEL 1:
3385 !
3390 Vc11dot=(Vc21-Vc11)/R11/C11
3395 Vc21dot=(Vapu1err/R21+Vreallerr/R31+Ic41-(Vc21-Vc11)/R11)/C21
3400 Vc11=Vc11+Vc11dot*Dt
3405 !
3410 ! THE VOLTAGE ON C1 IS LIMITED TO Vlim VOLTS:
3415 !
3420 Vc11=MIN(Vc11,15)
3425 Vc11=MAX(Vc11,-15)
3430 Vc21=Vc21+Vc21dot*Dt
3435 !
3440 ! THE VOLTAGE ON C2 IS ALSO LIMITED TO Vlim VOLTS:
3445 !
3450 Vc21=MIN(Vc21,15)
3455 Vc21=MAX(Vc21,-15)
3460 Vvco1=-Vc21/2
3465 !
3470 Vvco1=MIN(Vvco1,Vlim)
3475 Vvco1=MAX(Vvco1,-Vlim)
3480 !
3485 ! CHANNEL 2:
3490 !
3495 Vc12dot=(Vc22-Vc12)/R12/C12
3500 Vc22dot=(Vapu2err/R22+Vreal2err/R32+Ic42-(Vc22-Vc12)/R12)/C22
3505 Vc12=Vc12+Vc12dot*Dt
3510 !
3515 ! THE VOLTAGE ON C1 IS LIMITED TO Vlim VOLTS:
3520 !
3525 Vc12=MIN(Vc12,15)
3530 Vc12=MAX(Vc12,-15)
3535 Vc22=Vc22+Vc22dot*Dt
3540 !
3545 ! THE VOLTAGE ON C2 IS ALSO LIMITED TO Vlim VOLTS:
3550 !
3555 Vc22=MIN(Vc22,15)
3560 Vc22=MAX(Vc22,-15)
3565 Vvco2=-Vc22/2
3570 !
3575 Vvco2=MIN(Vvco2,Vlim)
3580 Vvco2=MAX(Vvco2,-Vlim)
3585 !
3590 ! REAL AND REACTIVE POWER CALCULATIONS:
3595 !
3600 Preal1=Ich1*V(4,1)
3605 Preal2=Ich2*V(5,1)
3610 Pimag1=Ich1*Vth1_s
3615 Pimag2=Ich2*Vth2_s
3620 Pout1hv=(Vhv(3,1)-Vhv(7,1))*Nturns1tr^2/Rhv1*Vhv(7,1)
3625 Pout2hv=(Vhv(4,1)-Vhv(8,1))*Nturns2tr^2/Rhv2*Vhv(8,1)
3630 !                            B-12
```

```
3635 ! TIME CONSTANT FOR THE WATTMETERS= .01 Sec:!
3640 !
3645 Watts1dot=(Preal1-Watts1)/.01
3650 Watts2dot=(Preal2-Watts2)/.01
3655 Iwatts1dot=(P1mag1-Iwatts1)/.01
3660 Iwatts2dot=(P1mag2-Iwatts2)/.01
3665 Watts1hvdot=(Pout1hv-Watts1hv)/.01
3670 Watts2hvdot=(Pout2hv-Watts2hv)/.01
3675 !
3680 Watts1=Watts1+Watts1dot*Dt
3685 Watts2=Watts2+Watts2dot*Dt
3690 Iwatts1=Iwatts1+Iwatts1dot*Dt
3695 Iwatts2=Iwatts2+Iwatts2dot*Dt
3700 Watts1hv=Watts1hv+Watts1hvdot*Dt
3705 Watts2hv=Watts2hv+Watts2hvdot*Dt
3710 !
3715 DISP "THIS RUN IS";INT(100*Nt/1200);"% COMPLETE"
3720 !
3725 NEXT Nt            !TIME SEQUENCE LOOP ENDS HERE**************************
3730 !
3735 !
3740 !
3745 !
3750 ! STORE FINAL CONDITIONS ON DISK FOR INITIAL CONDITIONS ON NEXT RUN:
3755 !
3760 IF (Keep$<>"Y") AND (Keep$<>"y") THEN 3825
3765 Save_data:!
3770 READ #1,1
3775 PRINT #1;Ang1,Ang2,Ang_apu,I1,I2,I3,I4,I5,I6,I7,I8,I9,Vmag1,Vmag2
3780 PRINT #1;Vc11,Vc12,Vc21,Vc22,Vc51,Vc52,Flag1,Watts1,Watts2,Iwatts1,Iwatts2
3785 PRINT #1;Duty1avg,Duty2avg,Rrect1,Rrect2,Vth1,Vth1a,Vth1c,Vth2,Vth2a,Vth2c
3790 PRINT #1;Vlink1f,Vlink2f,Vclink1,Vclink2,Ihv(*),Vhv1,Vhv2,Vhv1ub,Vhv2ub
3795 PRINT #1;Ifld1,Ifld2,Irotor1,Irotor2,Vhv(*),Ich1,Ich2,Ihv1ac,Ihv2ac
3800 PRINT #1;Vstator1,Vstator2,Rinv1loss,Rinv2loss,Apu1err,Apu2err,Vlink1max,Vl
ink2max
3805 PRINT #1;Vrotor1,Vrotor2,Vild1,Vild2,Vvco1,Vvco2,Ang_err,V(*),Va(*),Vc(*)
3810 PRINT #1;I1a,I2a,I3a,I4a,I5a,I6a,I7a,I8a,I9a,I1c,I2c,I3c,I4c,I5c,I6c,I7c,I8
c,I9c
3815 PRINT #1;Rhv1,Rhv2,Vhv1,Vhv2,Ihv1dc,Ihv2dc,Vcfb1,Vcfb2,Vpor1dc,Vpor2dc
3820 PRINT #1;Watts1hv,Watts2hv,Vfb1,Vfb2,Igen1,Igen2,Vgen1,Vgen2,Vc41,Vc42,Vcbu
rd
3825 GOSUB Plist_2
3830 DISP
3835 !
3840 ! THE PLOTTING ROUTINE FOLLOWS:
3845 !
3850 Plots:!
3855   PLOTTER IS "9872A"
3860   LIMIT 15,245,10,180
3865   SCALE -.075/100,.075,-1,1
3870   AXES .005,.1,0,0
3875   AXES 1,.1,.075,0
3880   PEN 1
3885   MOVE .065,-.9
3890   LABEL Title$
3895   MOVE .005,-.9
3900   IF Continuation=1 THEN 3915
3905   LABEL "(I/C=";Icfile$;")"
3910   GOTO 3920
3915   LABEL "(I/C=";Title2$;")"
3920   FOR I=1 TO 8
3925   PEN I
3930   FOR N=-2 TO 300
3935   IF N<=0 THEN 3950
3940   PLOT 4*Dt*(N-1),Plot(I,N)
3945   GOTO 3955
```

B-13

```
3950    PLOT 4*Dt*N,Plot(I,1)
3955    NEXT N
3960    PENUP
3965    NEXT I
3970    PENUP
3975    PEN 0
3980    Continuation=1
3985    Title2$=Title$
3990    PRINTER IS 16
3995    PRINT PAGE
4000 End: PRINT "FOR CONTINUATION PRESS CONTINUE"
4005    PAUSE
4010    LINPUT "RUN TITLE ?",Title$
4015 INPUT "DO YOU WANT TO KEEP FINAL CONDITIONS ON DISK?",Keep$
4020 IF (Keep$<>"Y") AND (Keep$<>"y") THEN 4035
4025    CREATE Title$,5
4030    ASSIGN #1 TO Title$
4035    GOTO Go
4040    END
4045    !
4050    ! END OF PROGRAM      **********************************************
4055    !
4060    ! PARAMETER LISTING SUBROUTINE FOLLOWS:
4065    !
4070 Plist_1: !
4075 Final_cond=0
4080 PRINTER IS 7,1
4085 PRINT "Parameter Definition List for Hybrid VCF/VSDC System Simulation, PR
OGRAM:";Pgm$
4090 PRINT
4095 PRINT "* Run Title: ";Title$,"Date: ";Date$
4100 PRINT "  Synopsis: ";Run$
4105 IF Continuation=1 THEN 4120
4110 PRINT "        This is a continuation of run: ";Icffile$
4115 GOTO 4125
4120 PRINT "        This is a continuation of run: ";Title2$
4125 PRINT "        Time frame for this run is: ";Tim<;"TO";Time+.075;"Secs."
4130 PRINT "        System rating, per channel, in KVA: VSCF=120, VSDC=270, Total=3
90"
4135 PRINT
4140 PRINT "* CIRCUIT PARAMETERS OHMS, FARADS AND HENRYS (CH1,CH2):"
4143 FLOAT 3
4150 PRINT
4155 PRINT "C11,C12                   ";C11;C12
4160 PRINT "C21,C22                   ";C21;C22
4165 PRINT "C51,C52                   ";C51;C52
4170 PRINT "Cf1,Cf2                   ";Cf1;Cf2
4175 PRINT "Clink1,Clink2             ";Clink1;Clink2
4180 PRINT
4185 PRINT "Lf1,Lf2                   ";Lf1;Lf2
4190 PRINT "Lb,Rlb                    ";Lb;Rlb
4195 PRINT "Lld1,Lld2                 ";Lld1;Lld2
4200 PRINT "Lfeed1,Lfeed2             ";Lfeed1;Lfeed2
4205 PRINT "Lfld1,Lfld2               ";Lfld1;Lfld2
4210 PRINT "Lrotor1,Lrotor2           ";Lrotor1;Lrotor2
4215 PRINT "Zgen1,Zgen2               ";Zgen1;Zgen2;"(ohms/phase at 18863 rpm)"
4220 PRINT "Zfeed1inv,Zfeed2inv       ";Zfeed1inv*6;Zfeed2inv*6;"(ohms/phase at 18
863 rpm)"
4225 PRINT "Zfeed1hv,Zfeed2hv         ";Zfeed1hv*6;Zfeed2hv*6;"(ohms/phase at 1886
3 rpm)"
4230 PRINT "Rld1,Rld2,Rloadhv         ";Rld1;Rld2;Rloadhv;" <<<<<<<<<System loads"
4235 PRINT "R11,R12                   ";R11;R12
4240 PRINT "R21,R22                   ";R21;R22
4245 PRINT "R31,R32                   ";R31;R32
4250 PRINT "R51,R52                   ";R51;R52
4255 PRINT "R61,R62                   ";R61;R62
```

```
4260 PRINT "Rcf1,Rcf2                    ";Rcf1;Rcf2
4265 PRINT "Rlfeed1,Rlfeed2              ";Rlfeed1;Rlfeed2
4270 PRINT "Rl1,Rl2                      ";Rl1;Rl2
4275 PRINT "Rfld1,Rfld2                  ";Rfld1;Rfld2
4280 PRINT "Rrotor1,Rrotor2              ";Rrotor1;Rrotor2
4285 PRINT "Rloss1gen,Rloss2gen          ";Rloss1gen;Rloss2gen
4290 PRINT "Rloss1hv,Rloss2hv            ";Rloss1hv;Rloss2hv
4295 PRINT "Rhv1,Rhv2                    ";Rhv1s;Rhv2s
4300 PRINT "Rhv1tie,Rhv2tie              ";Rhv1tie;Rhv2tie
4305 PRINT "Rburd1,Rburd2                ";Rburd1;Rburd2
4310 PRINT "Rburd1hv,Rburd2hv            ";Rburd1hv;Rburd2hv
4315 PRINT "Nturns1,Nturns2              ";Nturns1;Nturns2
4320 PRINT "Nturns1hv,Nturns2hv          ";Nturns1hv;Nturns2hv
4325 PRINT "Fcent1,Fcent2                ";Fcent1;Fcent2
4330 PRINT "VCO voltage input limit";"±";Vlim;"±";Vlim
4335 PRINT "Vfld op amp sat. limit ";"±";Vilimit;"±";Vilimit
4340 PRINT "Inverter current limit   ";Icl1;Icl2;"(pole amps peak)"
4345 PRINT "HVDC current limit       ";Icl1hv;Icl2hv;"(generator phase amps, rms)
"
4350 PRINT "K11,K12                      ";K11;K12;"(hz/volt)"
4355 PRINT "K21,K22                      ";K21;K22;"(volts/radian)"
4360 PRINT "K31,K32                      ";K31;K32;"(volts/rpm)"
4365 PRINT "K41,K42                      ";K41;K42;"(volts/amp)"
4370 PRINT "K51,K52                      ";K51;K52;"(volts/amp/rpm)"
4375 PRINT "K61,K62                      ";K61;K62;"(volts/volt)"
4380 PRINT "K71,K72                      ";K71;K72;"(volts/amp)"
4385 PRINT "K81,K82                      ";K81;K82;"(volts/volt)"
4390 PRINT "K91,K92                      ";K91;K92;"(/amp)"
4395 PRINT "K101,K102                    ";K101;K102;"(amps/amp)"
4400 PRINT "K111,K112                    ";K111;K112;"(volts/amp)"
4405 PRINT "Vrefinv1,Vrefinv2            ";Vrefinv1/SQR(2);Vrefinv2/SQR(2);"(rms, 1-n
)"
4410 PRINT "Vconv1sat,Vconv2sat          ";Vconv1sat;Vconv2sat
4415 PRINT "Vset1gen,Vset2gen            ";Vset1gen;Vset2gen
4420 PRINT "Vset1hv,Vset2hv              ";Vset1hv*Nturns1tr;Vset2hv*Nturns2tr;"(vdc)
"
4425 PRINT "Fcent1,Fcent2                ";Fcent1;Fcent2;"(hz)"
4430 PRINT "Rpm1,Rpm2                    ";Rpm1;Rpm2;"                   Page 1 of
 2"
4435 IF Continuation=1 THEN 4450
4440 PRINT "Run Title:";Title$,"Date:";Date$,"I/C file:";Icfile$,"Program:";Pgm$
4445 GOTO 4455
4450 PRINT "Run Title:";Title$,"Date:";Date$,"I/C file:";Title2$,"Program:";Pgm$
4455 PRINT
4460 PRINT "* INITIAL CONDITIONS *****************************************************
***********"
4465 PRINT
4470 Plist_3:!
4475 PRINT "VSCF :"
4480 PRINT
4485 PRINT "Frequency: Ch1, Ch2, APU                    ";Fcent1+K11*Vvco1;Fcent2+
K12*Vvco2;Fapu
4490 PRINT
4495 PRINT "Delta angle:  Ch1-Ch2 (deg)                 ";Ang_err*360/2/PI
4500 PRINT "Delta angle:  APU-Ch1 (deg)                 ";Apu1err*360/2/PI
4505 PRINT "Delta angle:  APU-Ch2 (deg)                 ";Apu2err*360/2/PI
4510 PRINT "Real  watts: Ch1, Ch2, delta                ";Watts1*3;Watts2*3;(Watts
1-Watts2)*3
4515 PRINT
4520 PRINT "Thevenin voltage: Ch1, Ch2 (rms 1-n)        ";Vmag1/SQR(2);Vmag2/SQR(2
)
4525 PRINT "Delta Thevenin voltage: Ch1-Ch2 (rms 1-n) ";(Vmag1-Vmag2)/SQR(2)
4530 PRINT "Reactive Watts:  Ch1, Ch2, Ch1-Ch2          ";Iwatts1*3;Iwatts2*3;(Iwa
tts1-Iwatts2)*3
4535 PRINT
4540 PRINT "VSDC:"                          B-15
```

```
4545 PRINT
4550 PRINT "Generator Thevenin voltage: Ch1, Ch2         ";Vstator1;Vstator2;"(rms
 l-n)"
4555 PRINT "Generator terminal voltage: Ch1, Ch2         ";Vhv(1,1);Vhv(2,1);"(rms
 l-n)"
4560 PRINT "Generator RPM: Ch1, Ch2                       ";Rpm1;Rpm2
4565 PRINT
4570 PRINT "HVDC  POR voltage: Ch1,Ch2                    ";Vhv1;Vhv2;"(rms l-n)"
4575 PRINT "HVDC output watts: Ch1,Ch2, Ch1-Ch2          ";Watts1hv;Watts2hv;Watts1
hv-Watts2hv
4580 PRINT "HVDC bus Volts,Watts:                         ";Vhv(9,1)*Nturns1tr;(Vhv(
9,1)*Nturns1tr)^2/Rloadhv
4585 IF Final_cond=0 THEN 4635
4590 PRINT
4595 PRINT "* Plotter details ******************************************************
**********"
4600 PRINT
4605 PRINT "Full scale = +1                 Time = .005 sec./div."
4610 PRINT
4615 PRINT "Black = ";P1$;TAB(40);"Red   = ";P2$
4620 PRINT "Orange= ";P3$;TAB(40);"Yellow= ";P4$
4625 PRINT "Green = ";P5$;TAB(40);"Blue  = ";P6$
4630 PRINT "Violet= ";P7$;TAB(40);"Brown = ";P8$
4635 STANDARD
4640 RETURN
4645 Plist_2:PRINTER IS 7,1
4650 FLOAT 3
4655 Final_cond=1
4660 PRINT
4665 PRINT "* FINAL CONDITIONS ****************************************************
**********"
4670 PRINT
4675 GOSUB Plist_3
4680 PRINT LIN(2)
4685 PRINT "
Page 2 of 2"
4690 PRINT PAGE;
4695 PRINTER IS 16
4700 RETURN
4705 !
4710 ! CIRCUIT NETWORK MATRIX(S) ARE LOADED IN FOLLOWING SUBROUTINE:
4715 !
4720 Load_mtx:!
4725 G(1,1)=1/R11+1/R11c
4730 G(1,4)=-1/R11c
4735 G(2,2)=1/R12+1/R12c
4740 G(2,5)=-1/R12c
4745 G(3,3)=1/R1b+1/R1bc
4750 G(3,8)=-1/R1bc
4755 G(3,9)=-1/R1b
4760 G(4,1)=-1/R11c
4765 G(4,4)=1/Rcf1+1/R11c+1/R1feed1c
4770 G(4,6)=-1/R1feed1c
4775 G(5,2)=-1/R12c
4780 G(5,5)=1/Rcf2+1/R12c+1/R1feed2c
4785 G(5,7)=-1/R1feed2c
4790 G(6,4)=-1/R1feed1c
4795 G(6,6)=1/R1feed1+1/R1feed1c
4800 G(6,8)=-1/R1feed1
4805 G(7,5)=-1/R1feed2c
4810 G(7,7)=1/R1feed2+1/R1feed2c
4815 G(7,9)=-1/R1feed2
4820 G(8,3)=-1/R1bc
4825 G(8,6)=-1/R1feed1
4830 G(8,8)=1/R1feed1+1/R1d1+1/R11d1c+1/R1bc
4835 G(9,3)=-1/R1b
```

B-16

```
4840 G(9,7)=-1/R1feed2
4845 G(9,9)=1/R1feed2+1/R1d2+1/R11d2c+1/R1b
4850 MAT R=INV(G)
4855 !
4860 !
4865 Load_mtx2:!
4870 !
4875 Ghv(1,1)=1/Zstator1+1/Rloss1gen+1/Zfeed1inv+1/Zfeed1hv
4880 Ghv(1,3)=-1/Zfeed1hv
4885 Ghv(1,5)=-1/Zfeed1inv
4890 Ghv(2,2)=1/Zstator2+1/Rloss2gen+1/Zfeed2inv+1/Zfeed2hv
4895 Ghv(2,4)=-1/Zfeed2hv
4900 Ghv(2,6)=-1/Zfeed2inv
4905 Ghv(3,1)=-1/Zfeed1hv
4910 Ghv(3,3)=1/Zfeed1hv+1/Rloss1hv+Nturns1tr^2/Rhv1
4915 Ghv(3,7)=-Nturns1tr^2/Rhv1
4920 Ghv(4,2)=-1/Zfeed2hv
4925 Ghv(4,4)=1/Zfeed2hv+1/Rloss2hv+Nturns2tr^2/Rhv2
4930 Ghv(4,8)=-Nturns2tr^2/Rhv2
4935 Ghv(5,1)=-1/Zfeed1inv
4940 Ghv(5,5)=1/Zfeed1inv
4945 Ghv(6,2)=-1/Zfeed2inv
4950 Ghv(6,6)=1/Zfeed2inv
4955 Ghv(7,3)=-Nturns1tr^2/Rhv1
4960 Ghv(7,7)=Nturns1tr^2*(1/Rhv1+1/Rhv1tie)
4965 Ghv(7,9)=-Nturns1tr^2/Rhv1tie
4970 Ghv(8,4)=-Nturns2tr^2/Rhv2
4975 Ghv(8,8)=Nturns2tr^2*(1/Rhv2+1/Rhv2tie)
4980 Ghv(8,9)=-Nturns1tr^2/Rhv2tie
4985 Ghv(9,7)=-Nturns1tr^2/Rhv1tie
4990 Ghv(9,8)=-Nturns2tr^2/Rhv2tie
4995 Ghv(9,9)=Nturns1tr^2/Rhv1tie+Nturns2tr^2/Rhv2tie+Nturns1tr^2/Rloadhv
5000 MAT Rhv=INV(Ghv)
5005 Rhv_check=Rhv1
5010 Rhv_chk1=Rhv2
5015 RETURN
5020 !
5025 ! INITIAL CONDITION LOADING FOLLOWS:
5030 !
5035 Newic:!
5040 IF (Ic$<>"Y") AND (Ic$<>"y") THEN 5055
5045 Icfile$="25K-FL"
5050 GOTO 5070
5055 PRINT PAGE
5060 CAT
5065 LINPUT "NAME OF I C FILE",Icfile$
5070 ASSIGN #2 TO Icfile$
5075 READ #2;Ang1,Ang2,Ang_apu,I1,I2,I3,I4,I5,I6,I7,I8,I9,Vmag1,Vmag2
5080 READ #2;Vc11,Vc12,Vc21,Vc22,Vc51,Vc52,Flag1,Watts1,Watts2,Iwatts1,Iwatt
5085 READ #2;Duty1avg,Duty2avg,Rrect1,Rrect2,Vth1,Vth1a,Vth1c,Vth2, h2a,Vth
5090 READ #2;Vlink1f,Vlink2f,Vclink1,Vclink2,Ihv(*),Vhv1,Vhv2,Vhv1ub,Vhv2ub
5095 READ #2;Ifld1,Ifld2,Irotor1,Irotor2,Vhv(*),Ich1,Ich2,Ihv1ac,Ihv2ac
5100 READ #2;Vstator1,Vstator2,Rinv1loss,Rinv2loss,Apu1err,Apu2err, link1ma
nk2max
5105 READ #2;Vrotor1,Vrotor2,Vild1,Vild2,Vvco1,Vvco2,Ang_err,Vs(*),Va(*),Vc
5110 READ #2;I1a,I2a,I3a,I4a,I5a,I6a,I7a,I8a,I9a,I1c,I2c,I3c,I4c,I5c,I6c,I7
,I9c
5115 READ #2;Rhv1,Rhv2,Vhv1,Vhv2,Ihv1dc,Ihv2dc,Vcfb1,Vcfb2,Vpor1dc,Vpor2dc
5120 READ #2;Watts1hv,Watts2hv,Vfb1,Vfb2,Igen1,Igen2,Vgen1,Vgen2,Vc41,Vc42,V
5125 PRINT PAGE
5130 RETURN
5135 !                                    B-17
```

APPENDIX C

Example Computer Runs of Computer Simulation
of
Parallel Conditioned Power System

Steady State Operation

AC System, DC Link Voltage (50V/div)

HVDC Output (2500V/div)

Generator Field Amps(1 amp/div)

Generator Difference Angle (.01 radians/div)

AC System Output Volts (100V/div)

AC System Output Amps, Channel 1 (500 amp/div)

Generator Difference Volts (10V/div)

Generator Difference Current (2 amp/div)

HVDC Difference Current (2 amp/div)

(I/C=25K-FL)

25K_FL

C-2

Parameter Definition List for Hybrid VSCF/VSDC System Simulation, PROGRAM:WP-PAR

* Run Title: 25KFL2 Date: 8/13/83
   Synopsis: Steady state, full load on all systems.
      This is a continuation of run: 25K-FL
      Time frame for this run is: 0 TO .075 Secs.
      System rating, per channel, in KVA: VSCF=120, VSDC=270, Total=390

* CIRCUIT PARAMETERS OHMS, FARADS AND HENRYS (CH1,CH2):

C11,C12	3.646E-06	3.681E-06
C21,C22	5.422E-07	5.252E-07
C51,C52	9.799E-06	1.065E-05
Cf1,Cf2	5.664E-04	5.733E-04
Clink1,Clink2	6.183E-04	6.217E-04
Lf1,Lf2	1.560E-05	1.460E-05
Lb,Rlb	1.573E-06	2.778E-04
Lld1,Lld2	1.000E+00	1.000E+00
Lfeed1,Lfeed2	1.473E-06	1.470E-06
Lfld1,Lfld2	1.138E-01	1.037E-01
Lrotor1,Lrotor2	4.771E-02	5.962E-02
Zgen1,Zgen2	1.097E-01	1.055E-01 (ohms/phase at 18863 rpm)
Zfeed1inv,Zfeed2inv	6.693E-02	6.468E-02 (ohms/phase at 18863 rpm)
Zfeed1hv,Zfeed2hv	2.195E-02	2.362E-02 (ohms/phase at 18863 rpm)
Rld1,Rld2,Rloadhv	3.333E-01	3.333E-01 3.240E+02 <<<<<<<<<<System loads
R11,R12	7.425E+03	7.538E+03
R21,R22	2.950E+03	3.025E+03
R31,R32	4.405E+04	4.392E+04
R51,R52	9.826E+03	9.806E+03
R61,R62	2.870E+04	2.837E+04
Rcf1,Rcf2	1.103E-01	1.090E-01
Rlfeed1,Rlfeed2	2.979E-04	2.777E-04
Rl1,Rl2	9.693E-03	8.550E-03
Rfld1,Rfld2	3.820E+00	4.339E+00
Rrotor1,Rrotor2	1.814E+00	1.826E+00
Rloss1gen,Rloss2gen	2.940E+01	2.685E+01
Rloss1hv,Rloss2hv	4.079E+01	3.651E+01
Rhv1,Rhv2	3.230E+01	3.050E+01
Rhv1tie,Rhv2tie	1.050E+00	9.300E-01
Rburd1,Rburd2	1.990E+02	2.010E+02
Rburd1hv,Rburd2hv	1.208E+03	1.198E+03
Nturns1,Nturns2	3.616E+03	3.590E+03
Nturns1hv,Nturns2hv	2.970E+03	3.024E+03
Fcent1,Fcent2	4.015E+02	3.979E+02
VCO voltage input limit	± 5.000E+00	± 5.000E+00
Vild op amp sat. limit	± 1.500E+01	± 1.500E+01
Inverter current limit	1.257E+03	1.146E+03 (pole amps peak)
HVDC current limit	2.605E+02	2.481E+02 (generator phase amps, rms)
K11,K12	-7.795E+00	-7.916E+00 (hz/volt)
K21,K22	1.975E+00	2.079E+00 (volts/radian)
K31,K32	3.918E-03	3.854E-03 (volts/rpm)
K41,K42	2.302E+01	2.093E+01 (volts/amp)
K51,K52	4.987E-04	5.220E-04 (volts/amp/rpm)
K61,K62	3.340E-01	3.438E-01 (volts/volt)
K71,K72	9.839E+00	9.795E+00 (volts/amp)
K81,K82	5.180E-01	4.950E-01 (volts/volt)
K91,K92	2.455E-02	2.651E-02 (/amp)
K101,K102	2.010E+00	2.000E+00 (amps/amp)
K111,K112	8.900E-01	9.100E-01 (volts/amp)
Vrefinv1,Vrefinv2	1.141E+02	1.160E+02 (rms, 1-n)
Vconv1sat,Vconv2sat	3.240E+02	3.200E+02
Vset1gen,Vset2gen	2.170E+02	2.130E+02
Vset1hv,Vset2hv	1.299E+04	1.342E+04 (vdc)
Fcent1,Fcent2	4.015E+02	3.979E+02 (hz)
Rpm1,Rpm2	2.489E+04	2.510E+04

* INITIAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   3.997E+02 4.000E+02 4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.323E-01
Delta angle: APU-Ch1 (deg)   -1.523E-01
Delta angle: APU-Ch2 (deg)   2.740E-01
Real watts: Ch1, Ch2, delta   1.156E+05 1.198E+05 -4.192E+03

Thevenin voltage: Ch1, Ch2 (rms l-n)   1.137E+02 1.141E+02
Delta Thevenin voltage: Ch1-Ch2 (rms l-n)   -4.892E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.712E+04 -2.171E+04 4.584E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   .   2.872E+02 2.910E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.495E+02 2.510E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04 2.510E+04

HVDC POR voltage: Ch1,Ch2   1.317E+04 1.317E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.520E+05 2.823E+05 -3.027E+04
HVDC bus Volts,Watts: 1.315E+04 5.336E+05

* FINAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   3.997E+02 4.000E+02 4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.309E-01
Delta angle: APU-Ch1 (deg)   -1.512E-01
Delta angle: APU-Ch2 (deg)   2.737E-01
Real watts: Ch1, Ch2, delta   1.157E+05 1.200E+05 -4.237E+03

Thevenin voltage: Ch1, Ch2 (rms l-n)   1.137E+02 1.142E+02
Delta Thevenin voltage: Ch1-Ch2 (rms l-n)   -4.919E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.714E+04 -2.174E+04 4.607E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.871E+02 2.911E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.495E+02 2.511E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04 2.510E+04

HVDC POR voltage: Ch1,Ch2   1.317E+04 1.317E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.509E+05 2.834E+05 -3.256E+04
HVDC bus Volts,Watts: 1.315E+04 5.336E+05

* Plotter details **

Full scale = ±1   Time = .005 sec./div.

Black = V(6,1)/1000   Red   = Ich1/5000
Orange= Vlink1f/500   Yellow= Ang_err*10 (.1 radian f/s)
Green = (Vstator1-Vstator2)/100   Blue = (Ihv1dc-Ihv2dc)/20
Violet= Vhv1/25000   Brown = Ifld1/10

C-4

(I/C=25K-FL)   HVDUMP

C-5

Parameter Definition List for Hybrid VSCF/VSDC System Simulation, PROGRAM:WP-PAR

CIRCUIT PARAMETERS OHMS, FARADS AND HENRYS (CH1,CH2):

C11,C12	3.646E-06	3.681E-06
C21,C22	5.422E-07	5.252E-07
C51,C52	9.799E-06	1.065E-05
Cf1,Cf2	5.664E-04	5.733E-04
Clink1,Clink2	6.183E-04	6.217E-04
Lf1,Lf2	1.560E-05	1.460E-05
Lb,Rlb	1.573E-06	2.778E-04
Lld1,Lld2	1.000E+00	1.000E+00
Lfeed1,Lfeed2	1.473E-06	1.470E-06
Lfld1,Lfld2	1.138E-01	1.037E-01
Lrotor1,Lrotor2	4.771E-02	5.962E-02
Zgen1,Zgen2	1.097E-01	1.055E-01 (ohms/phase at 18863 rpm)
Zfeed1inv,Zfeed2inv	6.693E-02	6.468E-02 (ohms/phase at 18863 rpm)
Zfeed1hv,Zfeed2hv	2.195E-02	2.362E-02 (ohms/phase at 18863 rpm)
Rld1,Rld2,Rloadhv	3.333E-01	3.333E-01 3.240E+05 <<<<<<<<<System loads
R11,R12	7.425E+03	7.538E+03
R21,R22	2.950E+03	3.025E+03
R31,R32	4.405E+04	4.392E+04
R51,R52	9.826E+03	9.806E+03
R61,R62	2.870E+04	2.837E+04
Rcf1,Rcf2	1.103E-01	1.090E-01
Rlfeed1,Rlfeed2	2.979E-04	2.777E-04
Rl1,Rl2	9.693E-03	8.550E-03
Rfld1,Rfld2	3.820E+00	4.339E+00
Rrotor1,Rrotor2	1.814E+00	1.826E+00
Rloss1gen,Rloss2gen	2.940E+01	2.685E+01
Rloss1hv,Rloss2hv	4.079E+01	3.651E+01
Rhv1,Rhv2	3.230E+01	3.050E+01
Rhv1tie,Rhv2tie	1.050E+00	9.300E-01
Rburd1,Rburd2	1.990E+02	2.010E+02
Rburd1hv,Rburd2hv	1.208E+03	1.198E+03
Nturns1,Nturns2	3.616E+03	3.590E+03
Nturns1hv,Nturns2hv	2.970E+03	3.024E+03
Fcent1,Fcent2	4.015E+02	3.979E+02
VCO voltage input limit	± 5.000E+00	± 5.000E+00
Vild op amp sat. limit	± 1.500E+01	± 1.500E+01
Inverter current limit	1.257E+03	1.146E+03 (pole amps peak)
HVDC current limit	2.605E+02	2.481E+02 (generator phase amps, rms)
K11,K12	-7.795E+00	-7.916E+00 (hz/volt)
K21,K22	1.975E+00	2.079E+00 (volts/radian)
K31,K32	3.918E-03	3.854E-03 (volts/rpm)
K41,K42	2.302E+01	2.093E+01 (volts/amp)
K51,K52	4.987E-04	5.220E-04 (volts/amp/rpm)
K61,K62	3.340E-01	3.438E-01 (volts/volt)
K71,K72	9.839E+00	9.795E+00 (volts/amp)
K81,K82	5.180E-01	4.950E-01 (volts/volt)
K91,K92	2.455E-02	2.651E-02 (/amp)
K101,K102	2.010E+00	2.000E+00 (amps/amp)
K111,K112	8.900E-01	9.100E-01 (volts/amp)
Vrefinv1,Vrefinv2	1.141E+02	1.160E+02 (rms, l-n)
Vconv1sat,Vconv2sat	3.240E+02	3.200E+02
Vset1gen,Vset2gen	2.170E+02	2.130E+02
Vset1hv,Vset2hv	1.299E+04	1.342E+04 (vdc)
Fcent1,Fcent2	4.015E+02	3.979E+02 (hz)
Rpm1,Rpm2	2.489E+04	2.510E+04

Page 1 of 2

* INITIAL CONDITIONS ***

VSCF :

Frequency: Ch1, Ch2, APU   3.997E+02 4.000E+02 4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.323E-01
Delta angle: APU-Ch1 (deg)   -1.523E-01
Delta angle: APU-Ch2 (deg)   2.740E-01
Real watts: Ch1, Ch2, delta   1.156E+05 1.198E+05 -4.192E+03

Thevenin voltage: Ch1, Ch2 (rms 1-n)   1.137E+02 1.141E+02
Delta Thevenin voltage: Ch1-Ch2 (rms 1-n) -4.892E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.712E+04 -2.171E+04   4.584E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.872E+02 2.910E+02 (rms 1-n)
Generator terminal voltage: Ch1, Ch2   2.495E+02 2.510E+02 (rms 1-n)
Generator RPM: Ch1, Ch2   2.489E+04 2.510E+04

HVDC POR voltage: Ch1,Ch2   1.317E+04 1.317E+04 (rms 1-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.520E+05 2.823E+05 -3.027E+04
HVDC bus Volts,Watts: 1.315E+04 5.336E+02

* FINAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   3.997E+02 4.000E+02 4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.309E-01
Delta angle: APU-Ch1 (deg)   -1.512E-01
Delta angle: APU-Ch2 (deg)   2.737E-01
Real watts: Ch1, Ch2, delta   1.157E+05 1.200E+05 -4.237E+03

Thevenin voltage: Ch1, Ch2 (rms 1-n)   1.137E+02 1.142E+02
Delta Thevenin voltage: Ch1-Ch2 (rms 1-n) -4.919E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.714E+04 -2.174E+04   4.607E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.315E+02 2.566E+02 (rms 1-n)
Generator terminal voltage: Ch1, Ch2   2.197E+02 2.448E+02 (rms 1-n)
Generator RPM: Ch1, Ch2   2.489E+04 2.510E+04

HVDC POR voltage: Ch1,Ch2   1.374E+04 1.374E+04 (rms 1-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   7.588E+01 8.083E+02 -7.324E+02
HVDC bus Volts,Watts: 1.374E+04 5.825E+02

* Plotter details ***

Full scale = ±1   Time = .005 sec./div.

Black = V(6,1)/1000   Red   = Ich1/5000
Orange= Vlink1f/500   Yellow= Ang_err*10 (.1 radian f/s)
Green = (Vstator1-Vstator2)/100 Blue   = (Ihv1dc-Ihv2dc)/20
Violet= Vhv1/25000   Brown = Ifld1/10

C-7

HVAPP

(I/C=HVDUMP)

C-8

* Run Title: HVAPP   Date: 9/13/83
   Synopsis: Application of full load to HVDC system.
       This is a continuation of run: HVDUMP
       Time frame for this run is: 0 TO .075 Secs.
       System rating, per channel, in KVA: VSCF=120, VSDC=270, Total=390

* CIRCUIT PARAMETERS OHMS, FARADS AND HENRYS (CH1,CH2):

C11,C12	3.646E-06	3.681E-06
C21,C22	5.422E-07	5.252E-07
C51,C52	9.799E-06	1.065E-05
Cf1,Cf2	5.664E-04	5.733E-04
Clink1,Clink2	6.183E-04	6.217E-04
Lf1,Lf2	1.560E-05	1.460E-05
Lb,Rlb	1.573E-06	2.778E-04
Lld1,Lld2	1.000E+00	1.000E+00
Lfeed1,Lfeed2	1.473E-06	1.470E-06
Lfld1,Lfld2	1.138E-01	1.037E-01
Lrotor1,Lrotor2	4.771E-02	5.962E-02
Zgen1,Zgen2	1.097E-01	1.055E-01	(ohms/phase at 18863 rpm)
Zfeed1inv,Zfeed2inv	6.693E-02	6.468E-02	(ohms/phase at 18863 rpm)
Zfeed1hv,Zfeed2hv	2.195E-02	2.362E-02	(ohms/phase at 18863 rpm)
Rld1,Rld2,Rloadhv	3.333E-01	3.333E-01	3.240E+02 <<<<<<<<<System load=
R11,R12	7.425E+03	7.538E+03
R21,R22	2.950E+03	3.025E+03
R31,R32	4.405E+04	4.392E+04
R51,R52	9.826E+03	9.866E+03
R61,R62	2.870E+04	2.837E+04
Rcf1,Rcf2	1.103E-01	1.090E-01
Rlfeed1,Rlfeed2	2.979E-04	2.777E-04
Rl1,Rl2	9.693E-03	8.550E-03
Rfld1,Rfld2	3.820E+00	4.339E+00
Rrotor1,Rrotor2	1.814E+00	1.826E+00
Rloss1gen,Rloss2gen	2.940E+01	2.685E+01
Rloss1hv,Rloss2hv	4.079E+01	3.651E+01
Rhv1,Rhv2	3.230E+01	3.050E+01
Rhv1tie,Rhv2tie	1.050E+00	9.300E-01
Rburd1,Rburd2	1.990E+02	2.010E+02
Rburd1hv,Rburd2hv	1.208E+03	1.198E+03
Nturns1,Nturns2	3.616E+03	3.590E+03
Nturns1hv,Nturns2hv	2.970E+03	3.024E+03
Fcent1,Fcent2	4.015E+02	3.979E+02
VCO voltage input limit	± 5.000E+00	± 5.000E+00
Vild op amp sat. limit	± 1.500E+01	± 1.500E+01
Inverter current limit	1.257E+03	1.146E+03	(pole amps peak)
HVDC current limit	2.605E+02	2.481E+02	(generator phase amps, rms)
K11,K12	-7.795E+00	-7.916E+00	(hz/volt)
K21,K22	1.975E+00	2.079E+00	(volts/radian)
K31,K32	3.918E-03	3.854E-03	(volts/rpm)
K41,K42	2.302E+01	2.093E+01	(volts/amp)
K51,K52	4.987E-04	5.220E-04	(volts/amp/rpm)
K61,K62	3.340E-01	3.438E-01	(volts/volt)
K71,K72	9.839E+00	9.795E+00	(volts/amp)
K81,K82	5.180E-01	4.950E-01	(volts/volt)
K91,K92	2.455E-02	2.651E-02	(/amp)
K101,K102	2.010E+00	2.000E+00	(amps/amp)
K111,K112	8.900E-01	9.100E-01	(volts/amp)
Vrefinv1,Vrefinv2	1.141E+02	1.160E+02	(rms, l-n)
Vconv1sat,Vconv2sat	3.240E+02	3.200E+02
Vset1gen,Vset2gen	2.170E+02	2.130E+02
Vset1hv,Vset2hv	1.299E+04	1.342E+04	(vdc)
Fcent1,Fcent2	4.015E+02	3.979E+02	(hz)
Rpm1,Rpm2	2.489E+04	2.510E+04

* INITIAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   3.997E+02   4.000E+02   4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.309E-01
Delta angle: APU-Ch1 (deg)   -1.512E-01
Delta angle: APU-Ch2 (deg)   2.737E-01
Real watts: Ch1, Ch2, delta   1.157E+05   1.200E+05 -4.237E+03

Thevenin voltage: Ch1, Ch2 (rms l-n)   1.137E+02   1.142E+02
Delta Thevenin voltage: Ch1-Ch2 (rms l-n)   -4.919E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.714E+04 -2.174E+04   4.607E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.315E+02   2.566E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.197E+02   2.448E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04   2.510E+04

HVDC POR voltage: Ch1,Ch2   1.374E+04   1.374E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   7.588E+01   8.083E+02 -7.324E+02
HVDC bus Volts,Watts: 1.374E+04   5.825E+05

* FINAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   3.997E+02   4.000E+02   4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.309E-01
Delta angle: APU-Ch1 (deg)   -1.510E-01
Delta angle: APU-Ch2 (deg)   2.738E-01
Real watts: Ch1, Ch2, delta   1.159E+05   1.201E+05 -4.250E+03

Thevenin voltage: Ch1, Ch2 (rms l-n)   1.138E+02   1.143E+02
Delta Thevenin voltage: Ch1-Ch2 (rms l-n)   -4.938E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.715E+04 -2.177E+04   4.624E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.815E+02   2.841E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.440E+02   2.451E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04   2.510E+04

HVDC POR voltage: Ch1,Ch2   1.287E+04   1.287E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.401E+05   2.613E+05 -2.122E+04
HVDC bus Volts,Watts: 1.285E+04   5.095E+05

* Plotter details **

Full scale = ±1   Time = .005 sec./div.

Black = V(6,1)/1000   Red   = Ich1/5000
Orange= Vlink1f/500   Yellow= Ang_err+10 (.1 radian f/s)
Green = (Vstator1-Vstator2)/100   Blue   = (Ihv1dc-Ihv2dc)/20
Violet= Vhv1/25000   Brown = Ifld1/10

(I/C=25K-FL)   AC1FLT

C-11

Parameter Definition List for Hybrid VSCF/VSDC System Simulation, PPOGRAM:WP-PAR

* Run Title: AC1FLT Date: 9/13/83
  Synopsis: Fault on channel 1 of AC system
      This is a continuation of run: 25K-FL
      Time frame for this run is: 0 TO .075 Secs.
      System rating, per channel, in KVA: VSCF=120, VSDC=270, Total=390

* CIRCUIT PARAMETERS OHMS, FARADS AND HENRYS (CH1,CH2):

C11,C12	3.646E-06	3.681E-06	
C21,C22	5.422E-07	5.252E-07	
C51,C52	9.799E-06	1.065E-05	
Cf1,Cf2	5.664E-04	5.733E-04	
Clink1,Clink2	6.183E-04	6.217E-04	
Lf1,Lf2	1.560E-05	1.460E-05	
Lb,R1b	1.573E-06	2.778E-04	
L1d1,L1d2	1.000E+00	1.000E+00	
Lfeed1,Lfeed2	1.473E-06	1.470E-06	
Lf1d1,Lf1d2	1.138E-01	1.037E-01	
Lrotor1,Lrotor2	4.771E-02	5.962E-02	
Zgen1,Zgen2	1.097E-01	1.055E-01	(ohms/phase at 18863 rpm)
Zfeed1inv,Zfeed2inv	6.693E-02	6.468E-02	(ohms/phase at 18863 rpm)
Zfeed1hv,Zfeed2hv	2.195E-02	2.362E-02	(ohms/phase at 18863 rpm)
R1d1,R1d2,Rloadhv	3.333E-04	3.333E-04	3.240E+02 <<<<<<<<<System load:
R11,R12	7.425E+03	7.538E+03	
R21,R22	2.950E+03	3.025E+03	
R31,R32	4.405E+04	4.392E+04	
R51,R52	9.826E+03	9.806E+03	
R61,R62	2.870E+04	2.837E+04	
Rcf1,Rcf2	1.103E-01	1.090E-01	
R1feed1,R1feed2	2.979E-04	2.777E-04	
R11,R12	9.693E-03	8.550E-03	
Rf1d1,Rf1d2	3.820E+00	4.339E+00	
Rrotor1,Rrotor2	1.814E+00	1.826E+00	
Rloss1gen,Rloss2gen	2.940E+01	2.685E+01	
Rloss1hv,Rloss2hv	4.079E+01	3.651E+01	
Rhv1,Rhv2	3.230E+01	3.050E+01	
Rhv1tie,Rhv2tie	1.050E+00	9.300E-01	
Rburd1,Rburd2	1.990E+02	2.010E+02	
Rburd1hv,Rburd2hv	1.200E+03	1.198E+03	
Nturns1,Nturns2	3.616E+03	3.590E+03	
Nturns1hv,Nturns2hv	2.970E+03	3.024E+03	
Fcent1,Fcent2	4.015E+02	3.979E+02	
VCO voltage input limit±	5.000E+00	± 5.000E+00	
Vild op amp sat. limit ±	1.500E+01	± 1.500E+01	
Inverter current limit	1.257E+03	1.146E+03	(pole amps peak)
HVDC current limit	2.605E+02	2.481E+02	(generator phase amps, rms)
K11,K12	-7.795E+00	-7.916E+00	(hz/volt)
K21,K22	1.975E+00	2.079E+00	(volts/radian)
K31,K32	3.918E-03	3.854E-03	(volts/rpm)
K41,K42	2.302E+01	2.093E+01	(volts/amp)
K51,K52	4.987E-04	5.220E-04	(volts/amp/rpm)
K61,K62	3.340E-01	3.438E-01	(volts/volt)
K71,K72	9.839E+00	9.795E+00	(volts/amp)
K81,K82	5.190E-01	4.950E-01	(volts/volt)
K91,K92	2.455E-02	2.651E-02	(/amp)
K101,K102	2.010E+00	2.000E+00	(amps/amp)
K111,K112	8.900E-01	9.100E-01	(volts/amp)
Vrefinv1,Vrefinv2	1.141E+02	1.160E+02	(rms, 1-n)
Vconv1sat,Vconv2sat	3.240E+02	3.200E+02	
Vset1gen,Vset2gen	2.170E+02	2.130E+02	
Vset1hv,Vset2hv	1.299E+04	1.342E+04	(vdc)
Fcent1,Fcent2	4.015E+02	3.979E+02	(hz)
Rpm1,Rpm2	2.489E+04	2.510E+04	

* INITIAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   3.997E+02   4.000E+02   4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.323E-01
Delta angle: APU-Ch1 (deg)   -1.523E-01
Delta angle: APU-Ch2 (deg)   2.740E-01
Real watts: Ch1, Ch2, delta   1.156E+05   1.198E+05 -4.192E+03

Thevenin voltage: Ch1, Ch2 (rms l-n)   1.137E+02   1.141E+02
Delta Thevenin voltage: Ch1-Ch2 (rms l-n) -4.892E-01
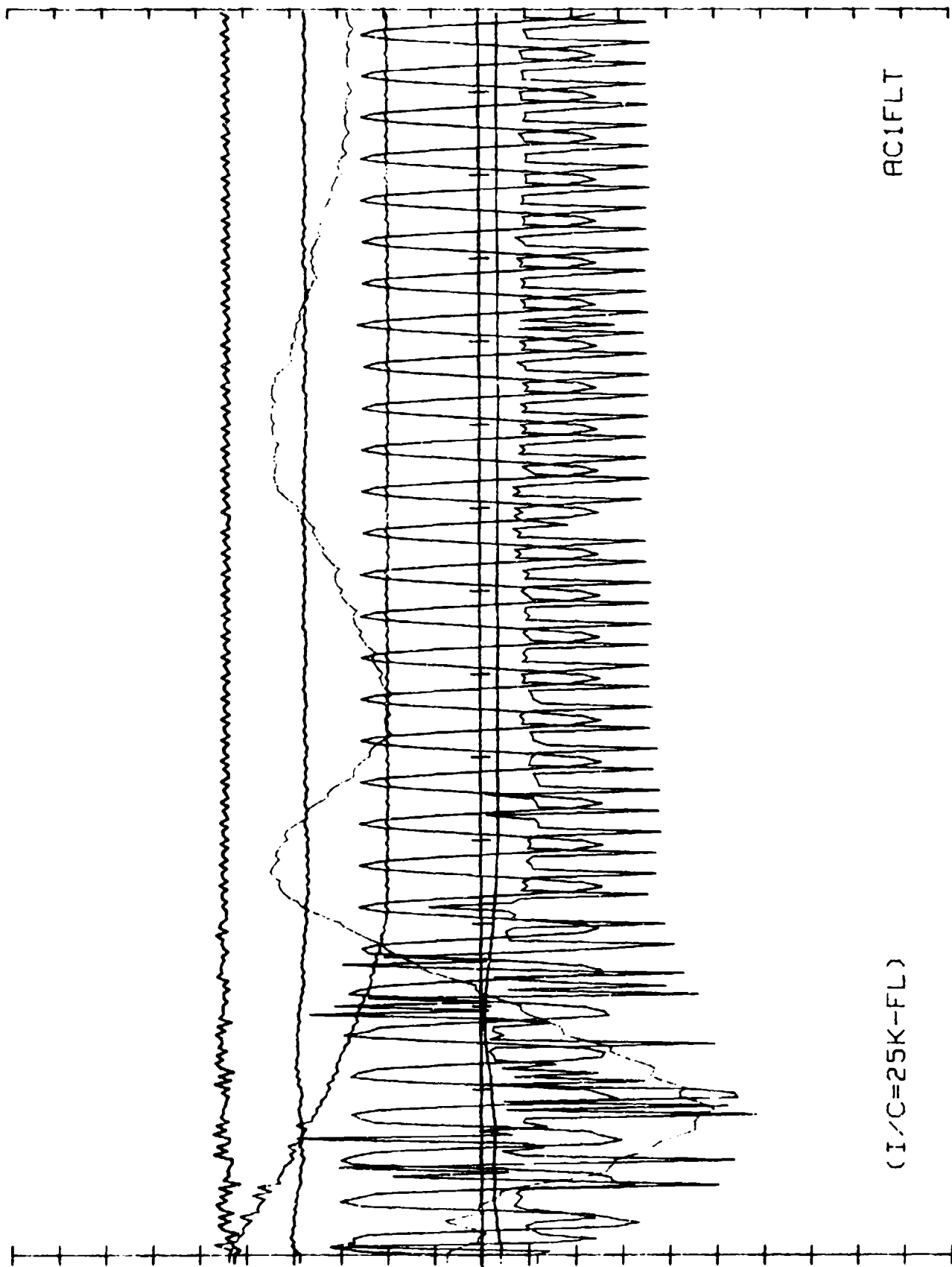Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.712E+04 -2.171E+04   4.584E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.872E+02   2.910E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.495E+02   2.510E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04   2.510E+04

HVDC POR voltage: Ch1,Ch2   1.317E+04   1.317E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.520E+05   2.823E+05 -3.027E+04
HVDC bus Volts,Watts: 1.315E+04   5.336E+05

* FINAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   4.004E+02   4.000E+02   4.000E+02

Delta angle: Ch1-Ch2 (deg)   1.568E+00
Delta angle: APU-Ch1 (deg)   -9.457E-01
Delta angle: APU-Ch2 (deg)   6.271E-01
Real watts: Ch1, Ch2, delta   3.244E+03   4.600E+03 -1.355E+03

Thevenin voltage: Ch1, Ch2 (rms l-n)   4.081E+01   4.131E+01
Delta Thevenin voltage: Ch1-Ch2 (rms l-n) -5.001E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.072E+05 -1.033E+05 -3.897E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.877E+02   2.916E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.513E+02   2.525E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04   2.510E+04

HVDC POR voltage: Ch1,Ch2   1.325E+04   1.325E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.564E+05   2.962E+05 -3.981E+04
HVDC bus Volts,Watts: 1.323E+04   5.406E+05

* Plotter details **

Full scale = ±1   Time = .005 sec./div.

Black = V(6,1)/1000   Red   = Ich1/5000
Orange= Vlink1f/500   Yellow= Ang_err*10 (.1 radian f/s)
Green = (Vstator1-Vstator2)/100   Blue = (Ihv1dc-Ihv2dc)/20
Violet= Vhv1/25000   Brown = Ifld1/10

C-13

(I/C=ACIFLT)   ACFCLR

C-14

* Run Title: ACfCLR Date: 9/14/83
  Synopsis: Fault removed from one channel of the AC system.
      This is a continuation of run: AC1FLT
      Time frame for this run is: 0 TO .075 Secs.
      System rating, per channel, in KVA: VSCF=120, VSDC=270, Total=390

* CIRCUIT PARAMETERS OHMS, FARADS AND HENRYS (CH1,CH2):

C11,C12	3.646E-06	3.681E-06
C21,C22	5.422E-07	5.252E-07
C51,C52	9.799E-06	1.065E-05
Cf1,Cf2	5.664E-04	5.733E-04
Clink1,Clink2	6.183E-04	6.217E-04
Lf1,Lf2	1.560E-05	1.460E-05
Lb,R1b	1.573E-06	2.778E-04
L1d1,L1d2	1.000E+00	1.000E+00
Lfeed1,Lfeed2	1.473E-06	1.470E-06
Lfld1,Lfld2	1.138E-01	1.037E-01
Lrotor1,Lrotor2	4.771E-02	5.962E-02
Zgen1,Zgen2	1.097E-01	1.055E-01 (ohms/phase at 18863 rpm)
Zfeed1inv,Zfeed2inv	6.693E-02	6.468E-02 (ohms/phase at 18863 rpm)
Zfeed1hv,Zfeed2hv	2.195E-02	2.362E-02 (ohms/phase at 18863 rpm)
R1d1,R1d2,Rloadhv	3.333E-01	3.333E-01 3.240E+02 <<<<<<<<<System loads
R11,R12	7.425E+03	7.538E+03
R21,R22	2.950E+03	3.025E+03
R31,R32	4.405E+04	4.392E+04
R51,R52	9.826E+03	9.806E+03
R61,R62	2.870E+04	2.837E+04
Rcf1,Rcf2	1.103E-01	1.090E-01
Rlfeed1,Rlfeed2	2.979E-04	2.777E-04
Rl1,Rl2	9.693E-03	8.550E-03
Rfld1,Rfld2	3.820E+00	4.339E+00
Rrotor1,Rrotor2	1.814E+00	1.826E+00
Rloss1gen,Rloss2gen	2.940E+01	2.685E+01
Rloss1hv,Rloss2hv	4.079E+01	3.651E+01
Rhv1,Rhv2	3.230E+01	3.050E+01
Rhv1tie,Rhv2tie	1.050E+00	9.300E-01
Rburd1,Rburd2	1.990E+02	2.010E+02
Rburd1hv,Rburd2hv	1.208E+03	1.198E+03
Nturns1,Nturns2	3.616E+03	3.590E+03
Nturns1hv,Nturns2hv	2.970E+03	3.024E+03
Fcent1,Fcent2	4.015E+02	3.979E+02
VCO voltage input limit	± 5.000E+00	± 5.000E+00
Vild op amp sat. limit	± 1.500E+01	± 1.500E+01
Inverter current limit	1.257E+03	1.146E+03 (pole amps peak)
HVDC current limit	2.605E+02	2.481E+02 (generator phase amps, rms)
K11,K12	-7.795E+00	-7.916E+00 (hz/volt)
K21,K22	1.975E+00	2.079E+00 (volts/radian)
K31,K32	3.918E-03	3.854E-03 (volts/rpm)
K41,K42	2.302E+01	2.093E+01 (volts/amp)
K51,K52	4.987E-04	5.220E-04 (volts/amp/rpm)
K61,K62	3.340E-01	3.438E-01 (volts/volt)
K71,K72	9.839E+00	9.795E+00 (volts/amp)
K81,K82	5.180E-01	4.950E-01 (volts/volt)
K91,K92	2.455E-02	2.651E-02 (/amp)
K101,K102	2.010E+00	2.000E+00 (amps/amp)
K111,K112	8.900E-01	9.100E-01 (volts/amp)
Vrefinv1,Vrefinv2	1.141E+02	1.160E+02 (rms, l-n)
Vconv1sat,Vconv2sat	3.240E+02	3.200E+02
Vset1gen,Vset2gen	2.170E+02	2.130E+02
Vset1hv,Vset2hv	1.299E+04	1.342E+04 (vdc)
Fcent1,Fcent2	4.015E+02	3.979E+02 (hz)
Rpm1,Rpm2	2.489E+04	2.510E+04

* INITIAL CONDITIONS ***

VSCF :

Frequency: Ch1, Ch2, APU   4.004E+02   4.000E+02   4.000E+02

Delta angle: Ch1-Ch2 (deg)   1.568E+00
Delta angle: APU-Ch1 (deg)   -9.457E-01
Delta angle: APU-Ch2 (deg)   6.271E-01
Real watts: Ch1, Ch2, delta   3.244E+03   4.600E+03 -1.355E+03

Thevenin voltage: Ch1, Ch2 (rms l-n)   4.081E+01   4.131E+01
Delta Thevenin voltage: Ch1-Ch2 (rms l-n) -5.001E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.072E+05 -1.033E+05 -3.897E+03

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.877E+02   2.916E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.513E+02   2.525E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04   2.510E+04

HVDC POR voltage: Ch1,Ch2   1.325E+04   1.325E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.564E+05   2.962E+05 -3.981E+04
HVDC bus Volts,Watts: 1.323E+04   5.406E+05

* FINAL CONDITIONS **

VSCF :

Frequency: Ch1, Ch2, APU   3.999E+02   4.000E+02   4.000E+02

Delta angle: Ch1-Ch2 (deg)   4.231E-01
Delta angle: APU-Ch1 (deg)   -8.739E-02
Delta angle: APU-Ch2 (deg)   3.337E-01
Real watts: Ch1, Ch2, delta   1.126E+05   1.228E+05 -1.028E+04

Thevenin voltage: Ch1, Ch2 (rms l-n)   1.141E+02   1.140E+02
Delta Thevenin voltage: Ch1-Ch2 (rms l-n) 1.030E-01
Reactive Watts: Ch1, Ch2, Ch1-Ch2   -1.155E+04 -2.764E+04   1.609E+04

VSDC:

Generator Thevenin voltage: Ch1, Ch2   2.857E+02   2.898E+02 (rms l-n)
Generator terminal voltage: Ch1, Ch2   2.482E+02   2.493E+02 (rms l-n)
Generator RPM: Ch1, Ch2   2.489E+04   2.510E+04

HVDC POR voltage: Ch1,Ch2   1.310E+04   1.310E+04 (rms l-n)
HVDC output watts: Ch1,Ch2, Ch1-Ch2   2.479E+05   2.792E+05 -3.133E+04
HVDC bus Volts,Watts: 1.308E+04   5.283E+05

* Plotter details ***

Full scale = ±1   Time = .005 sec./div.

Black = V(6,1)/1000   Red   = Ich1/5000
Orange= Vlink1f/500   Yellow= Ang_err*10 (.1 radian f/s)
Green = (Vstator1-Vstator2)/100   Blue = (Ihv1dc-Ihv2dc)/20
Violet= Vhv1/25000   Brown = Ifld1/10

C-16